SY28810A

5.5V 10A Load Switch with Ultra low $R_{DS(ON)}$

General Description

The SY28810A is a 2.8mΩ, single-channel load switch with a controlled and adjustable turn-on and integrated Power Good (PG) indicator.

The device contains an N-channel MOSFET that can operate over an input voltage range of 0.6V to 5.5V and can support a maximum continuous current of 10A. The wide input voltage range and high current capability enable the device to be used in various applications. The low ON resistance of 2.8mΩ minimizes the voltage drop across the load switch, effectively reducing power loss.

The device's controlled rise time can help mitigate the inrush current associated with large bulk load capacitances, effectively minimizing or eliminating power supply droop. The design flexibility is enhanced through the adjustable slew rate which can be configured using an external capacitor, CSST, allowing for a trade-off between inrush current and power-up timing requirements. Additionally, the integrated PG indicator informs the system of the load switch status, aiding in seamless power sequencing.

The SY28810A is available in a compact DFN 2mm×3mm-10pin package with an integrated thermal pad, enabling efficient dissipation of high power. The device is designed for operation across a wide temperature range, from -40°C to +105°C in free-air conditions.

Features

- Integrated Single Channel Load Switch
- V_{BIAS} Voltage Range: 2.5V to 5.5V
- V_{IN} Voltage Range: 0.6V to V_{BIAS}
- On-Resistance: 2.8mΩ@V_{IN}=3.3V, V_{BIAS}=3.3V
- 10A Maximum Continuous Switch Current
- Shutdown Current
  - I_{SD_VBIAS} = 5.5μA at V_{BIAS} = 5V
  - I_{SD_VIN} = 4nA at V_{BIAS} = 5V, V_{IN} = 5V
- Controlled and Adjustable Slew Rate through C_{SST}
- Power Good (PG) Indicator
- Compact DFN2×3-10 Package

Applications

- Servers
- Telecom systems

Typical Application

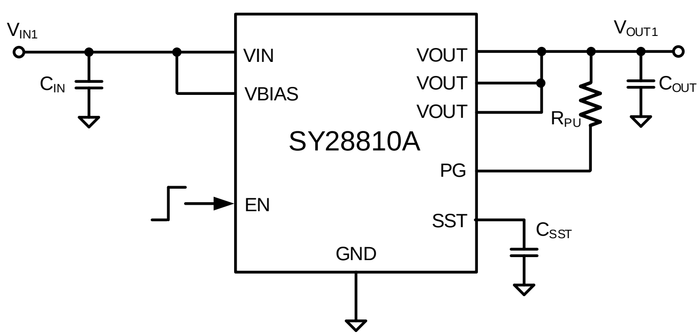


Figure 1. Schematic Diagram

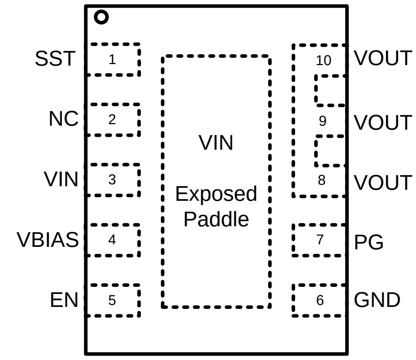
Ordering Information

Ordering Number	Package Type	Top Mark
SY28810ADHC	DFN2×3-10 RoHS Compliant and Halogen Free	***7Qxyz***

Device code: 7Q

x=year code, y=week code, z= lot number code

Pinout (Top View)



(DFN2×3-10)

Pin Number	Pin Name	Pin Description
1	SST	VOUT slew rate control.
2	NC	No connection.
3	VIN	Switch input. Bypass this input with a 10μF ceramic capacitor to GND.
4	VBIAS	Bias voltage. Internal power supply, connect a 0.1μF ceramic capacitor to GND.
5	EN	Active high switch control input. Do not leave floating.
6	GND	Ground.
7	PG	Power good indicator. Active high, Open drain output. Tie to GND if not used.
8,9,10	VOUT	Switch output. Connect a 10μF ceramic capacitor to GND.
Exposed Pad	VIN	Switch input. Connected to a wide and thick power trace to achieve the best thermal and electrical performance.

Block Diagram

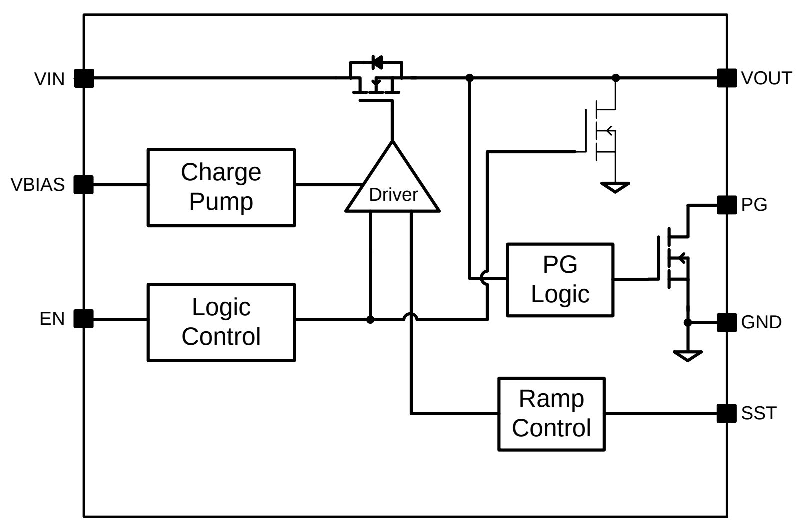


Figure 2. Block Diagram

Absolute Maximum Ratings

Parameter (Note 1)	Min	Max	Unit
VIN, VBIAS, VOUT, EN, PG	-0.3	6	V
SST	-0.3	V_{OUT}+6	
Lead Temperature (Soldering, 10s)		260	°C
Junction Temperature, Operating	-40	150	
Storage Temperature	-65	150	

Thermal Information

Parameter (Note 2)	Typ	Unit
θ_{JA} Junction-to-Ambient Thermal Resistance	51.4	°C/W
θ_{JC} Junction-to-Case Thermal Resistance	65	
P_D Power Dissipation T_A = 25°C	2.43	W

Recommended Operating Conditions

Parameter (Note 3)	Min	Max	Unit
VIN	0.6	VBIAS	V
VBAIS	2.5	5.5	
VOUT	0	VIN	
EN, PG	0	5.5	
Junction Temperature, Operating	-40	125	°C
Ambient Temperature	-40	105	

Electrical Characteristics

(-40°C≤T_J≤+105°C (full) and V_{BIAS} = 5V. Typical values are at T_A = 25°C, unless otherwise specified. The values are guaranteed by test, design or statistical correlation.)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Voltage Range for V_{IN}	V_{IN}		0.6		5.5	V
Voltage Range for V_{BUS}	V_{BUS}		2.5		5.5	V
VBIAS UVLO	V_{BIAS_UVLO}				2.4	V
VBIAS UVLO Hysteresis	V_{BIAS_HYS}			0.1		V
VBIAS Quiescent Current	I_{Q_BIAS}	V_{BIAS}=5V, V_{IN}=EN=5V, -40°C to 85°C		75	98	μA
		V_{BIAS}=3.3V, V_{IN}=EN=3.3V, -40°C to 85°C		66	86	μA
		V_{BIAS}=5V, V_{IN}=EN=5V, -40°C to 105°C		75	100	μA
		V_{BIAS}=3.3V, V_{IN}=EN=3.3V, -40°C to 105°C		66	88	μA
VBIAS Shutdown Current	I_{SHDN_BIAS}	V_{BIAS}=5V, V_{IN}=5V, EN=0V, V_{OUT}=0V, -40°C to 85°C		8	12	μA
		V_{BIAS}=5V, V_{IN}=5V, EN=0V, V_{OUT}=0V, -40°C to 105°C			12	μA
VIN Shutdown Current	I_{SHDN_VIN}	V_{IN}=5V, EN=0V, V_{OUT}=0V, -40°C to 85°C		0.004	10	uA
		V_{IN}=5V, EN=0V, V_{OUT}=0V, -40°C to105°C			20	μA
		V_{IN}=3.3V, EN=0V, V_{OUT}=0V, -40°C to 85°C		0.003	7	μA
		V_{IN}=3.3V, EN=0V, V_{OUT}=0V, -40°C to105°C			14	μA
		V_{IN}=2.5V, EN=0V, V_{OUT}=0V, -40°C to 85°C		0.002	6	μA
		V_{IN}=2.5V, EN=0V, V_{OUT}=0V, -40°C to105°C			12	μA
		V_{IN}=1.8V, EN=0V, V_{OUT}=0V, -40°C to 85°C		0.002	6	μA
		V_{IN}=1.8V, EN=0V, V_{OUT}=0V, -40°C to105°C			10	μA
		V_{IN}=1.05V, EN=0V, V_{OUT}=0V, -40°C to 85°C		0.001	4	μA
		V_{IN}=1.05V, EN=0V, V_{OUT}=0V, -40°C to105°C			8	μA
		V_{IN}=0.6V, EN=0V, V_{OUT}=0V, -40°C to 85°C		0.001	4	μA
		V_{IN}=0.6V, EN=0V, V_{OUT}=0V, -40°C to105°C			7	μA
EN Leakage Current	I_{EN_LKG}	V_{EN}=5.5V, -40°C to105°C			0.1	μA
EN Turn-on Threshold	V_{EN_ON}	T_A=25°C	1.2			V
EN Turn-off Threshold	V_{EN_OFF}	T_A=25°C			0.4	V
PG Leakage Current	I_{PG_LKG}	V_{PG}=5.0V, -40°C to105°C			0.5	μA
PG Output Low Voltage	V_{PG_LOW}	V_{EN}=0V, I_{PG}=1mA			0.2	V
Integrate FET RON	$R_{DS(ON)}$	V_{BIAS}=EN=5V, I_{OUT}=1A: V_{IN}=5V, -40°C to 85°C		2.8	5.7	mΩ
		V_{BIAS}=EN=5V, I_{OUT}=1A: V_{IN}=5V, -40°C to 105°C			6	mΩ
		V_{BIAS}=EN=5V, I_{OUT}=1A: V_{IN}=3.3V, -40°C to 85°C		2.8	5.7	mΩ
		V_{BIAS}=EN=5V, I_{OUT}=1A: V_{IN}=3.3V, -40°C to 85°C			6	mΩ
		V_{BIAS}=EN=5V, I_{OUT}=1A: V_{IN}=0.6V, -40°C to 85°C		2.8	5.7	mΩ
		V_{BIAS}=EN=5V, I_{OUT}=1A: V_{IN}=0.6V, -40°C to 85°C			6	mΩ
		V_{BIAS}=EN=3.3V, I_{OUT}=1A: V_{IN}=3.3V, -40°C to 85°C		2.8	5.7	mΩ
		V_{BIAS}=EN=3.3V, I_{OUT}=1A: V_{IN}=3.3V, -40°C to 105°C			6	mΩ
		V_{BIAS}=EN=3.3V, I_{OUT}=1A: V_{IN}=2.5V, -40°C to 85°C		2.8	5.7	mΩ
		V_{BIAS}=EN=3.3V, I_{OUT}=1A: V_{IN}=2.5V, -40°C to 85°C			6	mΩ
		V_{BIAS}=EN=3.3V, I_{OUT}=1A: V_{IN}=0.6V, -40°C to 85°C		2.8	5.7	mΩ
		V_{BIAS}=EN=3.3V, I_{OUT}=1A: V_{IN}=0.6V, -40°C to 85°C			6	mΩ
Discharge Resistance	R_{DIS}	V_{IN}=5V		200		Ω
Switching Characteristics						
VOUT Rise Time	t_{rise}	R_L=10Ω, C_L=0.1μF, C_{SST}=0pF, V_{BIAS}=EN=5V: V_{IN} =5V		31		μs
		R_L=10Ω, C_L=0.1μF, C_{SST}=0pF, V_{BIAS}=EN=5V: V_{IN} =1.05V		13		μs
		R_L=10Ω, C_L=0.1μF, C_{SST}=0pF, V_{BIAS}=EN=5V: V_{IN} =0.6V		10		μs

Parameter	Symbol	Test Conditions		Min	Typ	Max	Unit
		R_L=10Ω, C_L=0.1μF, C_{SST}=0pF, V_{BIAS}=EN=3.3V	V_{IN} =3.3V		24		μs
			V_{IN} =1.05V		12		μs
			V_{IN} =0.6V		9		μs
Turn On Delay	t_{d_ON}	R_L=10Ω, C_L=0.1μF, C_{SST}=0pF, V_{BIAS}=EN=5V	V_{IN} =5V		26		μs
			V_{IN} =1.05V		26		μs
			V_{IN} =0.6V		27		μs
		R_L=10Ω, C_L=0.1μF, C_{SST}=0pF, V_{BIAS}=EN=3.3V	V_{IN} =3.3V		26		μs
			V_{IN} =1.05V		26		μs
			V_{IN} =0.6V		27		μs
VOUT Fall Time	t_{fall}	R_L=10Ω, C_L=0.1μF, C_{SST}=0pF, V_{BIAS}=EN=5V	V_{IN} =5V		2.3		μs
			V_{IN} =1.05V		2.2		μs
			V_{IN} =0.6V		2.2		μs
		R_L=10Ω, C_L=0.1μF, C_{SST}=0pF, V_{BIAS}=EN=3.3V	V_{IN} =3.3V		2.4		μs
			V_{IN} =1.05V		2.3		μs
			V_{IN} =0.6V		2.3		μs
PG Turn On Time	t_{PG_ON}	R_L=10Ω, C_L=0.1μF, C_{SST}=0pF, V_{BIAS}=EN=5V	V_{IN} =5V		192		μs
			V_{IN} =1.05V		134		μs
			V_{IN} =0.6V		131		μs
		R_L=10Ω, C_L=0.1μF, C_{SST}=0pF, V_{BIAS}=EN=3.3V	V_{IN} =3.3V		132		μs
			V_{IN} =1.05V		122		μs
			V_{IN} =0.6V		119		μs
PG Turn Off Time	t_{PG_OFF}	R_L=10Ω, C_L=0.1μF, C_{SST}=0pF, V_{BIAS}=EN=5V	V_{IN} =5V		1.3		μs
			V_{IN} =1.05V		1.3		μs
			V_{IN} =0.6V		1.3		μs
		R_L=10Ω, C_L=0.1μF, C_{SST}=0pF, V_{BIAS}=EN=3.3V	V_{IN} =3.3V		1.5		μs
			V_{IN} =1.05V		1.5		μs
			V_{IN} =0.6V		1.5		μs

Note 1: Stresses beyond the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: θ_{JA} is measured in the natural convection at T_A = 25°C on a high effective 4-layer thermal conductivity test board of JEDEC 51-7 thermal measurement standard. V_{OUT} of DFN2×3-10 package is the case position for θ_{JC} measurement.

Note 3: The device is not guaranteed to function outside its operating conditions.

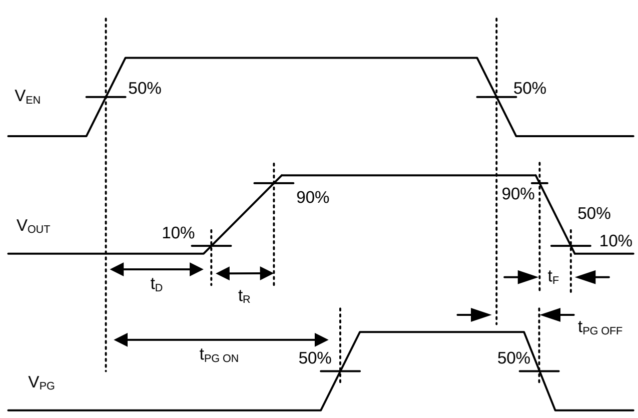
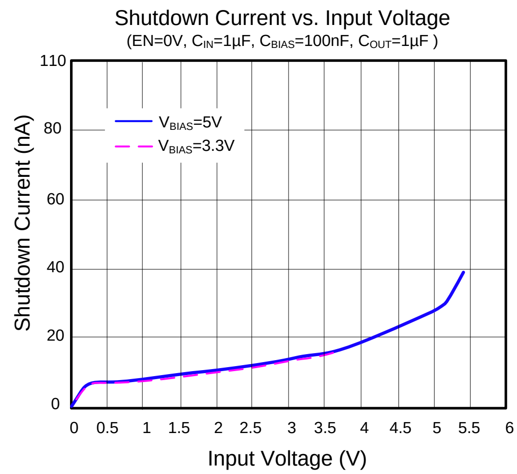
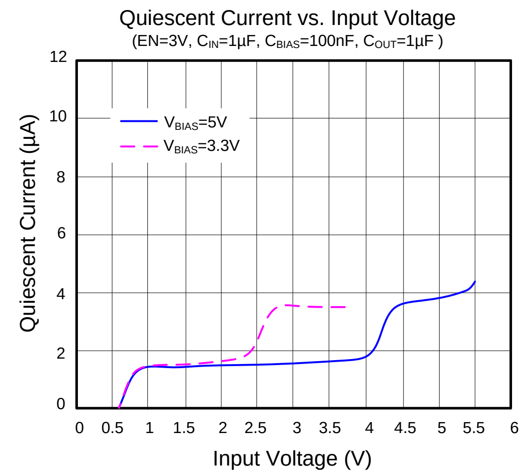
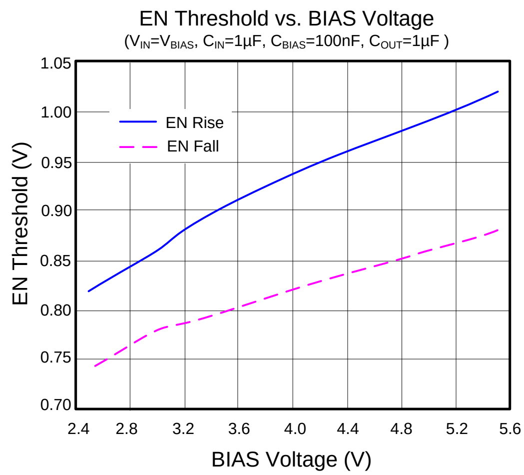


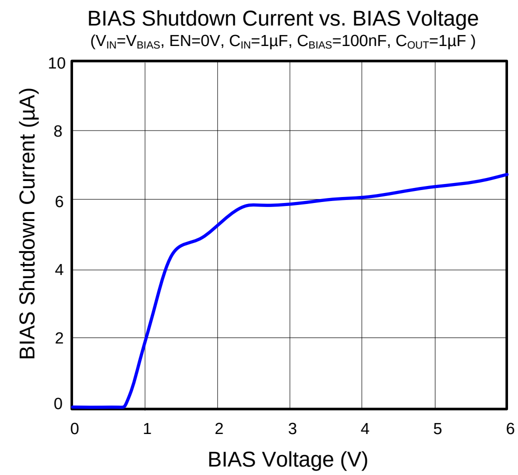
Figure 3. Timing Waveform

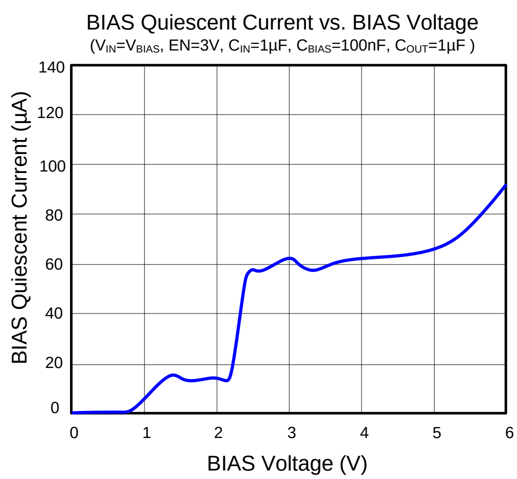
Typical Performance Characteristics

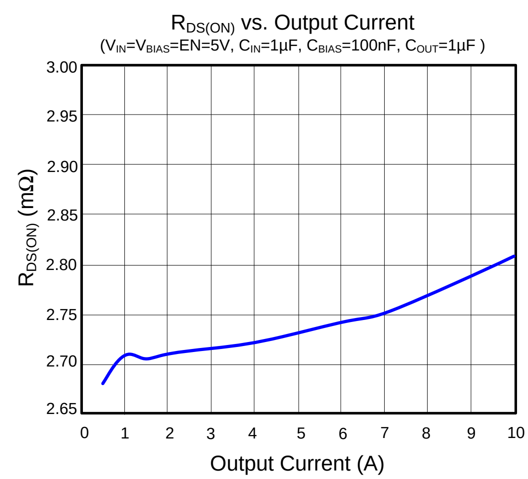




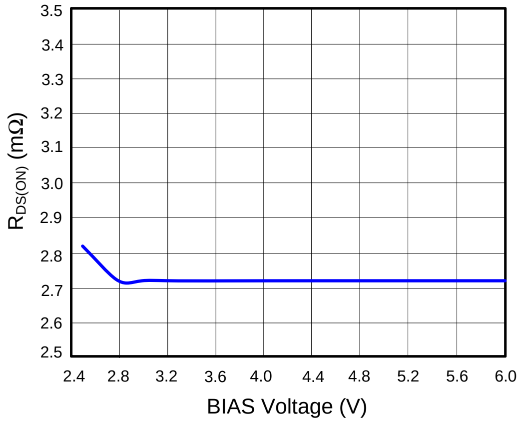




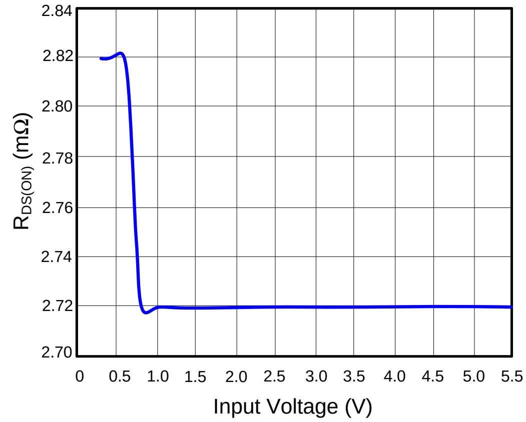




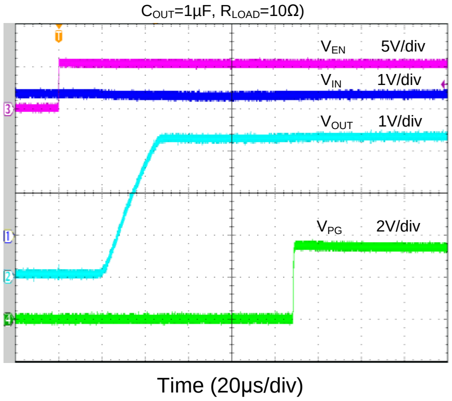
$R_{DS(ON)}$ vs. BIAS Voltage
(V_{IN}=V_{BIAS}=EN=5V, C_{IN}=1µF, C_{BIAS}=100nF, C_{OUT}=1µF)



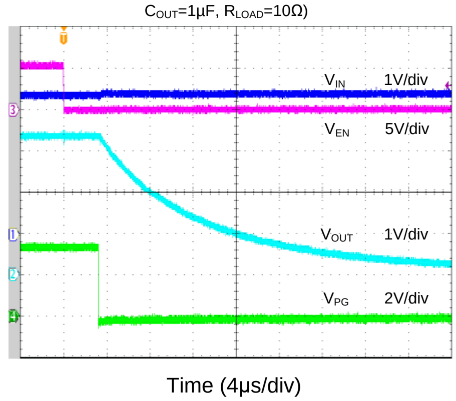
$R_{DS(ON)}$ vs. Input Voltage
(V_{IN}=V_{BIAS}=EN=5V, C_{IN}=1µF, C_{BIAS}=100nF, C_{OUT}=1µF)



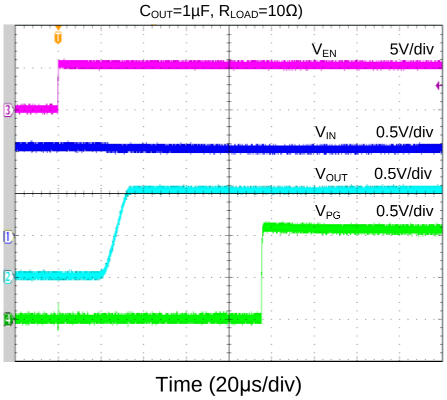
EN ON
(V_{BIAS}=3.3V, V_{IN}=3.3V, EN=0V to 5V, C_{IN}=1µF, C_{BIAS}=0.1µF, C_{OUT}=1µF, R_{LOAD}=10Ω)



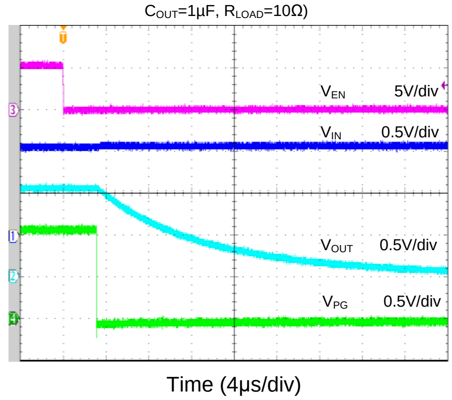
EN OFF
(V_{BIAS}=3.3V, V_{IN}=3.3V, EN=5V to 0V, C_{IN}=1µF, C_{BIAS}=0.1µF, C_{OUT}=1µF, R_{LOAD}=10Ω)



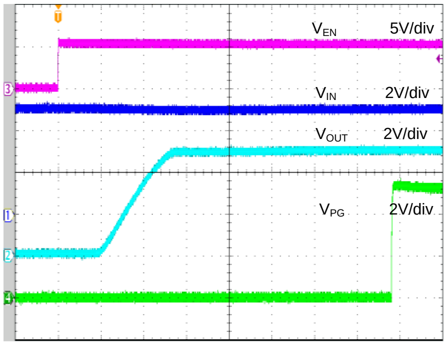
EN ON
(V_{BIAS}=3.3V, V_{IN}=1.05V, EN=0V to 5V, C_{IN}=1µF, C_{BIAS}=0.1µF, C_{OUT}=1µF, R_{LOAD}=10Ω)



EN OFF
(V_{BIAS}=3.3V, V_{IN}=1.05V, EN=5V to 0V, C_{IN}=1µF, C_{BIAS}=0.1µF, C_{OUT}=1µF, R_{LOAD}=10Ω)

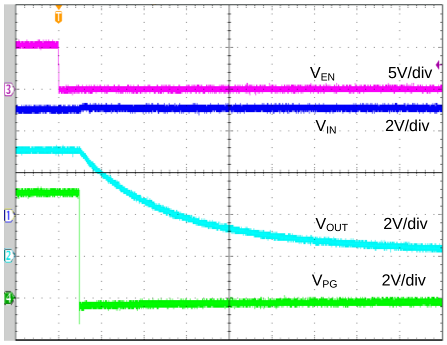


EN ON
(V_{BIAS}=5V, V_{IN}=5V, EN=0V to 5V, C_{IN}=1μF, C_{BIAS}=0.1μF, C_{OUT}=1μF, R_{LOAD}=10Ω)



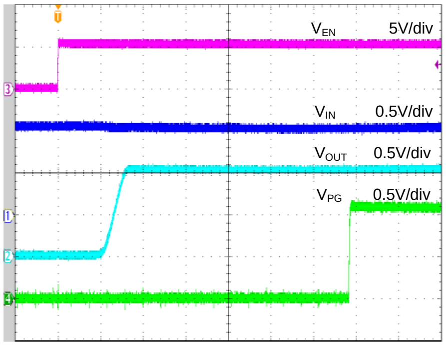
Time (20μs/div)

EN OFF
(V_{BIAS}=5V, V_{IN}=5V, EN=5V to 0V, C_{IN}=1μF, C_{BIAS}=0.1μF, C_{OUT}=1μF, R_{LOAD}=10Ω)



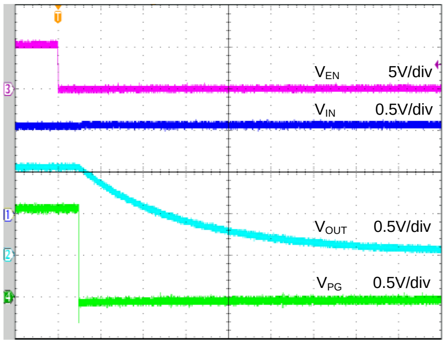
Time (4μs/div)

EN ON
(V_{BIAS}=5V, V_{IN}=1.05V, EN=0V to 5V, C_{IN}=1μF, C_{BIAS}=0.1μF, C_{OUT}=1μF, R_{LOAD}=10Ω)



Time (20μs/div)

EN OFF
(V_{BIAS}=5V, V_{IN}=1.05V, EN=5V to 0V, C_{IN}=1μF, C_{BIAS}=0.1μF, C_{OUT}=1μF, R_{LOAD}=10Ω)



Time (4μs/div)

Application Information

The SY28810A is a 2.8mΩ, single-channel load switch with a controlled and adjustable turn-on and integrated PG indicator.

The device contains an N-channel MOSFET that can operate over an input voltage range of 0.6V to 5.5V and can support a maximum continuous current of 10A. The wide input voltage range and high current capability enable the device to be used in various applications. The low ON resistance of 2.8mΩ minimizes the voltage drop across the load switch, effectively reducing power loss.

The device's controlled rise time can help mitigate the inrush current associated with large bulk load capacitances, effectively minimizing or eliminating power supply droop. The design flexibility is enhanced through the adjustable slew rate which can be configured using an external capacitor, CSST, allowing for a trade-off between inrush current and power-up timing requirements. Additionally, the integrated PG indicator informs the system of the load switch status, aiding in seamless power sequencing.

During shutdown, the device offers a very low leakage current, thereby reducing unnecessary leakage for downstream modules during standby. The SY28810A has an optional 200Ω on-chip resistor for quick discharge of the output when the switch is disabled.

Input Pin:
It is recommended to connect a capacitor between VIN and GND close to the device pins. This helps limit the voltage drop on the input supply induced by transient inrush currents when the switch is activated into a discharged capacitor at the load. Typically, a 1μF ceramic capacitor, CIN, is deemed sufficient. Higher values of CIN can be used to further reduce the voltage drop. A CIN to CL (load capacitance) ratio of 1 to 1 is recommended for minimizing VIN dip caused by inrush currents during startup.

Bias Capacitor:
For optimal decoupling performance, it is strongly recommended to include a decoupling capacitor of at least 0.1μF between the VBIAS pin and the GND. This capacitor should be placed as close to the device as possible.

EN Pin:
The EN pin controls the state of the load switch. Asserting the pin high enables the switch. The minimum voltage that guarantees a logic high is 1.2V. This pin cannot be left floating and must be tied driven high or low for proper functionality.

Output Delay Time (SST):
The SY28810A features controlled rise time for effective inrush current control. The rise time is adjusted by connecting a capacitor to GND on the SST pin. Without any capacitor on SST, the rise time is at its minimum for the fastest timing. Equation 1 provides an approximate relationship between SST, VIN, and rise time when VBIAS is set to 5V. Rise time, as illustrated in Figure 3, is defined from the 10% to 90% measurement on VOUT.

$$t_R=(0.009\times V_{IN}+0.002)\times C_{SST}+4.3\times V_{IN}+6 \qquad (1)$$

Where:
- t_R is the rise time (in μs)
- V_{IN} is the input voltage (in V)
- C_{SST} is the capacitance value on the SST pin (in pF)

Table 1 contains rise time values measured on a typical device. Rise times shown below are only valid for the power-up sequence where VIN and VBIAS are already in a steady state condition before the ON pin is asserted high.

Table 1. Rise Time vs. SST Capacitor

C_{SST} (pF)	Rise Time (μs) at 25°C C_L =1μF, C_{IN} =1μF, R_L=10Ω, V_{BIAS}=5V				
	V_{IN}= 5V	V_{IN}= 3.3V	V_{IN}= 1.8V	V_{IN}= 1.05V	V_{IN}= 0.8V
0	27.2	20.1	13.32	9.28	8.16
220	37.6	26.8	17.3	11.76	10.04
470	48.1	34	21.4	14.2	12.2
1000	74	51.4	31.1	20.4	17.2
2200	134.8	92.4	55	35.1	28.5
4700	274.6	167.2	98.4	62	50.2
10000	485	324	186.8	117.6	95.2

Power Good (PG):
The SY28810A provides a Power Good (PG) output signal indicating that the pass MOSFET gate is driven high, and the switch is on, with the On-resistance close to its final value (full load ready). The open-drain output is high-impedance in its active state. The required pull-up resistor can be connected to a voltage source compatible with the interface to the host controller. It is important to note that a valid PG output requires VBIAS to be present. Equation 2 outlines the approximate relationship between CSST, VIN, and PG turn-on time ($t_{PG,ON}$) when VBIAS is set to 5V:

$$t_{PG,ON}=(0.0107\times V_{IN}+0.04)\times C_{SST}+4.3\times V_{IN}+134 \qquad (2)$$

Where:

- $t_{PG,ON}$ is the PG turn-on time (in µs)
- V_{IN} is the input voltage (in V)
- C_{SST} is the capacitance value on the CT pin (in pF)

Table 2 contains the PG turn-on time values measured on a typical device.

Table 2. PG Turn on Time vs. CT Capacitor

SST (pF)	Typical PG turn on time (µs) at 25°C C_L=1µF, C_{IN}=1µF, R_L=10Ω, V_{BIAS}=5V, R_{PU}=10kΩ				
	VIN= 5V	VIN= 3.3V	VIN= 1.8V	VIN= 1.05V	VIN= 0.8V
0	155.4	148	140.2	137.2	137
220	178.2	166.4	155.2	150.4	150.2
470	201.2	185.2	170	163.4	163.0
1000	258	231.6	207.2	196.2	194.4
2200	395.2	343.6	295.6	273.6	268
4700	641	545	457	415	405
10000	1166	971	795	709	688

Power Supply Recommendations:

The device is designed to operate with a VBIAS range of 2.5V to 5.5V, and a VIN range of 0.6V to VBIAS. The supply must be well-regulated and placed as close to the device terminal as possible with the recommended 1µF bypass capacitor. If the supply is located more than a few inches from the device terminals, additional bulk capacitance may be required in addition to the ceramic bypass capacitors. In the case where the power supply is slow to respond to a large load current step, additional bulk capacitance may also be required. If additional bulk capacitance is required, an electrolytic, tantalum, or ceramic capacitor of 10µF may be sufficient.

PCB Layout Guide:

For best performance of the SY28810A, the following guidelines must be strictly followed:

1. Keep all power traces as short and wide as possible and use at least 2 ounce copper for all power traces.
2. Input and output capacitors should be placed close to the SY28810A and connected to the ground plane to reduce noise coupling and parasitic trace inductance.
3. The SST trace must be as short as possible to reduce parasitic capacitance.

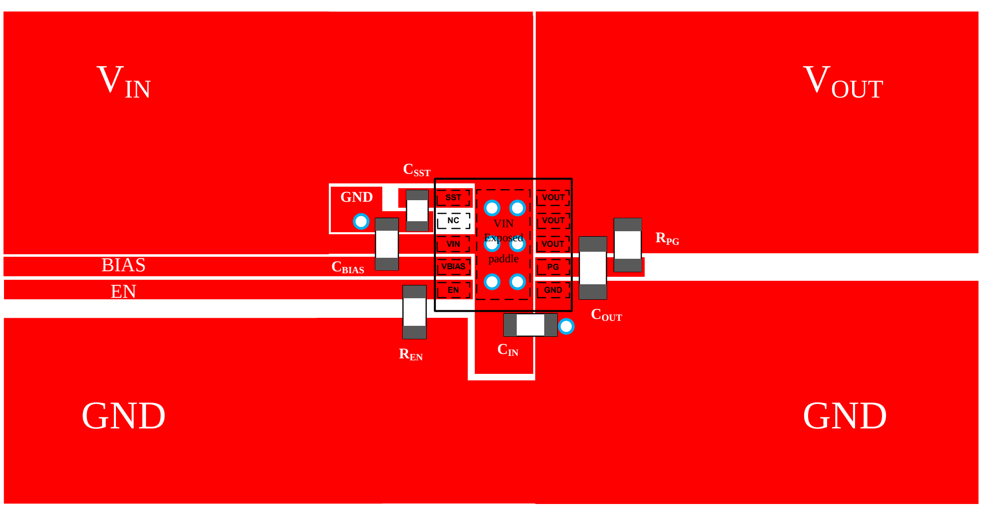
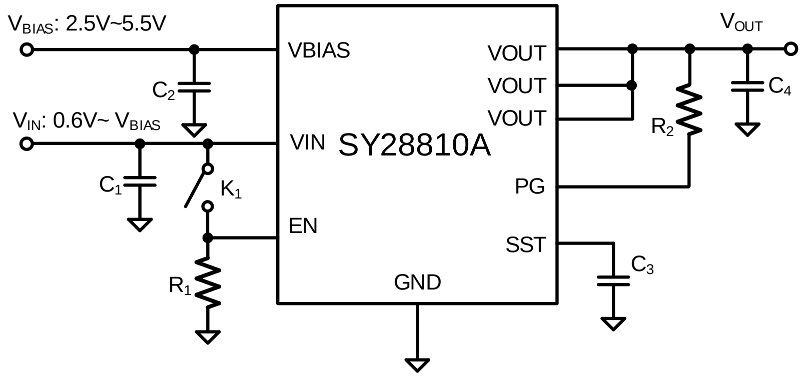


Figure 4. PCB Layout Suggestion

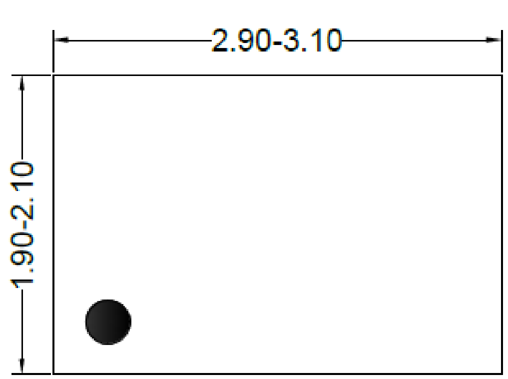
Schematic



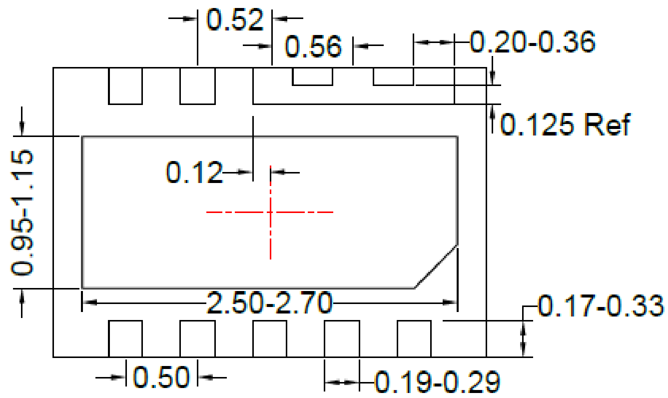
BOM List

Reference Designator	Description	Part Number	Manufacturer
U_1		SY28810ADHC	Silergy
C_1, C_4	10μF/10V, 0805, X7R	GRM21BR71A106K	Murata
C_2	0.1μF/50V, 0603, X5R	GRM188R61H104K	Murata
C_3	Null		
R_1	1MΩ, 0603		
R_2	10KΩ, 0603		

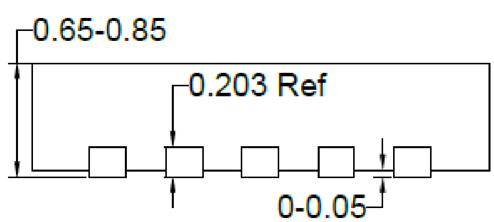
Package Outline Drawing



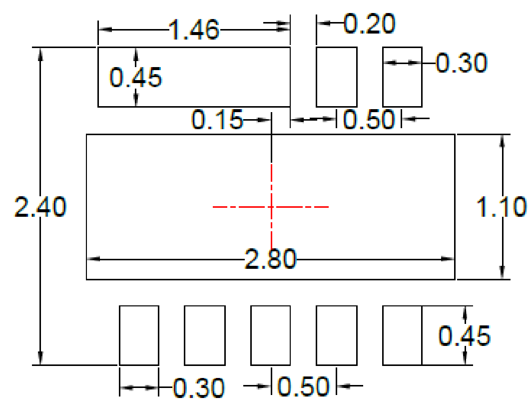
Top View



Bottom View



Front View

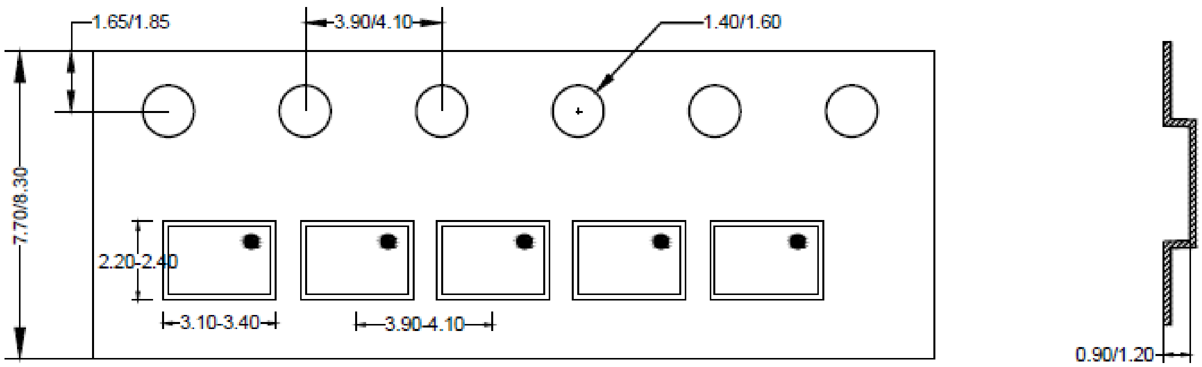


Recommended PCB Layout (Reference Only)

Notes: 1. All dimensions are in millimeters and exclude mold flash and metal burr.
2: The center of the PCB diagram refers to the chip center.

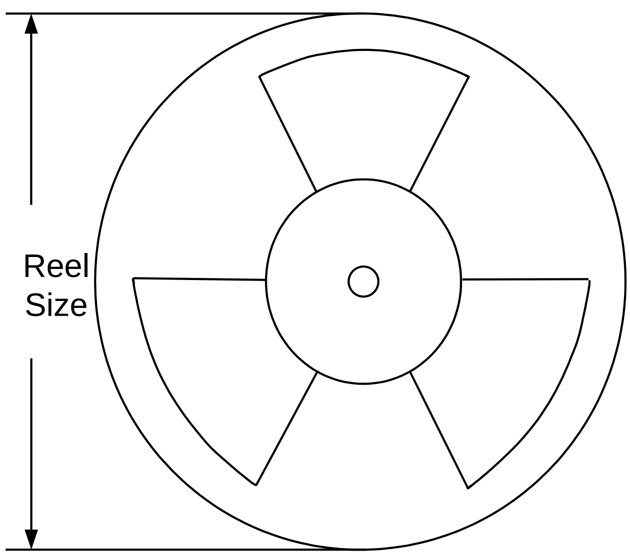
Taping & Reel Specification

DFN2×3 Taping Orientation



Feeding direction →

Carrier Tape & Reel Specification for Packages



Package type	Tape width (mm)	Pocket pitch (mm)	Reel size (Inch)	Trailer length (mm)	Leader length (mm)	Qty per reel (pcs)
DFN2×3-10	8	4	7"	400	160	3000

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, however, not warrantied. Please make sure that you have the latest revision.

Date	Revision	Change
Jan.05, 2024	Revision 1.0	Language improvements for clarity.
Dec.17, 2021	Revision 0.9	Initial Release

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