SY2A55105

High- or Low-Side, Bidirectional, High Accuracy Current-Sense Amplifier

General Description

SY2A55105 is a 100V/V fixed Gain, high-precision, High or Low Side, voltage output current-sense amplifier, suitable for bidirectional (charge/discharge) or unidirectional current measurements.

The SY2A55105 has a low offset zero-drift architecture across the -0.3V to 26V input common-mode voltage range, which is independent of supply voltage. The precise input offset voltage (V_{OS}) allows the device to function very well in measuring the low voltage drop in the power management unit.

The SY2A55105 is designed to operate from a 3V to 5.5V supply, and draws just 80μA (typ) quiescent current. The device is provided in a SOT363 package, and specified over the extended automotive temperature range of -40°C to 125°C. The device is AEC−Q100 Qualified.

Features

- Voltage-output, Current-sense amplifier
- Wide Common Mode Operation Range: -0.3V~26V
- Gain=100V/V
- Amplifier's Output Referenced to VREF input
- Shunt Drop Range:
  - -20mV to 20mV (VCC=5V，REF=2.5V)
  - 1mV to 45mV (VCC=5V，REF=0V)
- Low Offset Voltage: ±50μV (Maximum)
- 0.5μV/°C Offset Drift (Maximum)
- Accuracy: ±0.5% Gain Error (Maximum)
- 10ppm/°C Gain Drift (Maximum)
- Quiescent Current: 100μA (Maximum)
- AEC-Q100 Qualified
- Packages: SOT363

Applications

- On-Board Charge (OBC)
- Battery Management System (BMS)
- Body Control Modules
- Over-current Detection
- Wireless Charging

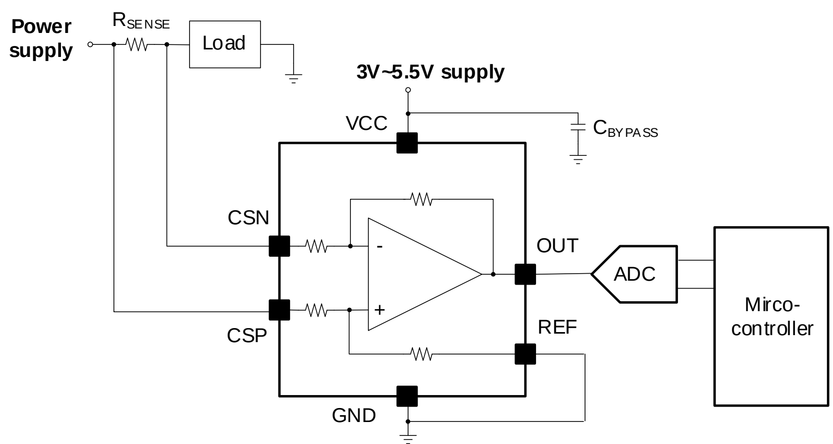


Figure 1. Typical application

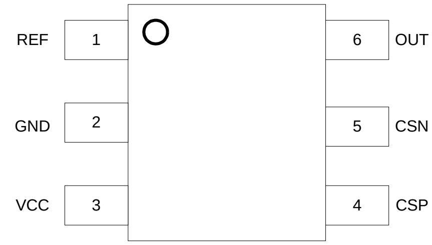
Figure. 1 shows the basic connections of the SY2A55105. The two-input pin CSN and CSP should be connected to the shunt resistor as closely as possible to minimize any resistance in series with the sense resistor. A bypass capacitor connected to the power-supply is required for stability concern.

Ordering Information

Ordering Part Number	Package type	Top Mark
SY2A55105AHT	SOT363 RoHS Compliant and Halogen Free	***b**xyz*

x=year code, y=week code, z= lot number code

Pinout (Top View)



(SOT363)

Pin Description

Pin No	Pin Name	Pin Description
1	REF	Reference voltage input, 0V to VCC.
2	GND	Ground.
3	VCC	Power supply, 3V to 5.5V.
4	CSP	Connect to supply side of shunt resistor.
5	CSN	Connect to load side of shunt resistor.
6	OUT	Amplifier Output.

Block Diagram

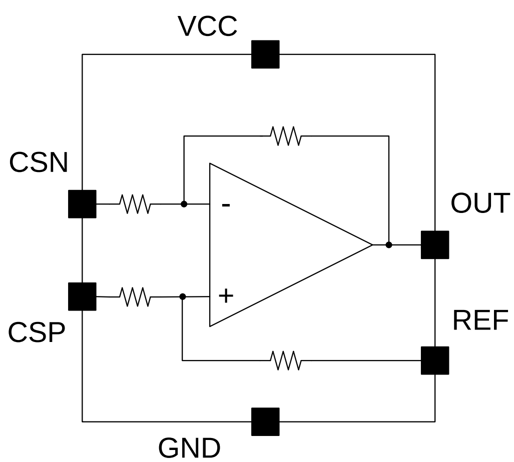


Figure 2. Block Diagram

Absolute Maximum Ratings

Parameter (Note 1)	Min	Max	Unit
VCC	-0.3	6	V
CSP, CSN(Common-mode)	-0.3	29	
CSP, CSN(Differential)	-29	29	
REF	-0.3	VCC	
OUT	-0.3	VCC	
Junction Temperature, Operating	-40	150	°C
Storage Temperature	-65	150	
ESD: HBM (Human Body Model)	± 4000		V
ESD: CDM (Charged Device Model)	± 1000		V

Thermal Information

Parameter (Note 2)	Max	Unit
θ_{JA} Junction-to-ambient Thermal Resistance	321	°C/W
θ_{JC} Junction-to-case Thermal Resistance	60	
P_D Power Dissipation T_A = 25°C	0.31	W

Recommended Operating Conditions

Parameter (Note 3)	Min	Max	Unit
CSP, CSN (Differential)	-20	20	mV
VCC	3	5.5	V
REF	GND	VCC	
Junction Temperature Range	-40	125	°C

Electrical Characteristics

T_A = -40°C to 125°C, VCC = 5V, V_{SENSE} = CSP-CSN = 0mV, CSP = 12V, and VREF = 2.5V, unless otherwise noted.

Parameter		Symbol	Test condition	Min	Typ	Max	Unit
Input	Common-mode Input	V_{CM}		-0.3		26	V
	Common-mode Rejection Ratio	CMRR	CSP=CSN=0 V to 26 V, V_{SENSE} = 0mV	105	125		dB
	Offset Voltage, RTI (Note 4)	V_{OS}	V_{SENSE} = 0 mV, T_A = 25°C		±1	±50	μV
	Offset Voltage vs Temperature	dV_{OS}/dT			0.1	0.5	μV/°C
	Offset Voltage vs Power Supply	PSR	VCC = 3 V to 5.5V, CSP = 12 V, V_{SENSE} = 0 mV, T_A = 25°C		±0.1	±6	μV/V
	Input Bias Current	I_B	V_{SENSE} = 0 mV, T_A = 25°C	30	38	45	μA
	Input Offset Current	I_{OS}	V_{SENSE} = 0 mV, T_A = 25°C		±0.02		μA
Output	Gain				100		V/V
	Gain Error		V_{SENSE} = -20 mV to 20 mV		±0.02%	±0.5%	
	Gain Error vs Temperature				3	10	ppm/°C
	Nonlinearity Error		T_A = 25°C		±0.01%		
	Maximum Capacitive Load		No sustained oscillation, T_A = 25°C		1		nF
Voltage Output	Output Voltage Swing to V_{CC} Power-supply Rail		R_{LOAD} = 10kΩ to GND		(V_{CC}) - 0.05	(V_{CC})- 0.2	V
	Output Voltage Swing to GND		R_{LOAD} = 10kΩ to GND		(V_{GND})+ 0.005	(V_{GND})+ 0.05	V
Frequency Response	Bandwidth	BW	C_{LOAD} = 10pF, T_A = 25°C		28		kHz
	Slew Rate	SR	T_A = 25°C		0.4		V/μs
Power Supply	Operation Voltage	V_{CC}		3		5.5	V
	Quiescent Current	I_Q	V_{SENSE} = 0 mV, T_A = 25°C		80	100	μA
			V_{SENSE} = 0 mV			100	μA

Note 1: Stresses beyond the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: Package thermal resistance is measured in the natural convection at T_A=25˚C on an 8.5cm×8.5cm size single-layer Silergy Evaluation Board.

Note 3: The device is not guaranteed to function outside its operating conditions.

Note 4: RTI = Referred to Input.

Applications Information

The SY2A55105 is a 100V/V fixed Gain, zero-drift current-sense amplifier that can monitors current by amplifying the differential voltage across an external shunt resistor to create an output voltage.

The SY2A55104 has -0.3V to 26V input common-mode voltage range, which is independent of supply voltage. This ability allows the current to be monitored during short-circuit conditions, while also enabling high-side current sensing above the supply voltage. This device is intended to operate as Analog Front END (AFE) for ADC or microcontroller requiring high-common mode signal translation to low-side referenced inputs. It is commonly used for over-current detection, voltage feedback control loops, or as a power monitor.

REF Input

The SY2A55105 device will measure the voltage developed across a current-sense resistor when current passes through the device. The transfer function of SY2A55105 is

$$OUT=100\times V_{SENSE}+V_{REF} \qquad (V_{SENSE}=V_{CSP}-V_{CSN})$$

This ability allows the SY2A55105 applicable to unidirectional and bidirectional current sensing.

It should be noted that the linear output range of the SY2A55105 is 0.05V to VCC-0.2V, it means the output will saturate low condition with small input signal when the REF pin is connected to ground and output will saturate high condition with small input signal when the REF pin is connected to VCC. In order to achieve ideal linear amplification, it is necessary to ensure that the output voltage is between 0.05V and VCC-0.2V.

For unidirectional current-sense application, the REF pin can be connected to ground directly as Figure 3 shown. When the input signal increases, the output voltage will increase. When very low input currents need to be measured, the REF pin needs to be biased to a convenient value above 50 mV to bring the output into the linear range of the device.

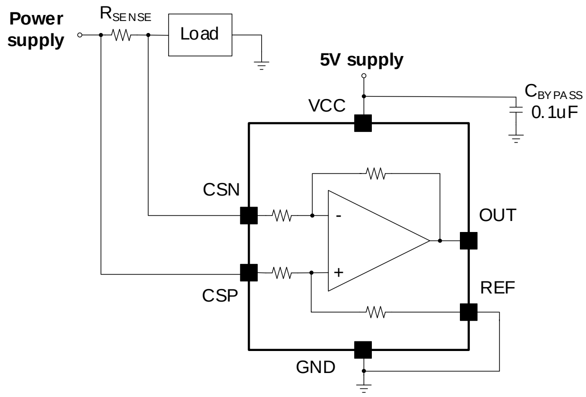


Figure 3. Unidirectional Current-sense Application

For bidirectional current-sense application, the REF pin can be connected to a reference voltage (for example 0.5×VCC) as Figure 4 shown. The output rises above the reference voltage for positive differential input signals and falls below the reference voltage for negative differential input signals linearly.

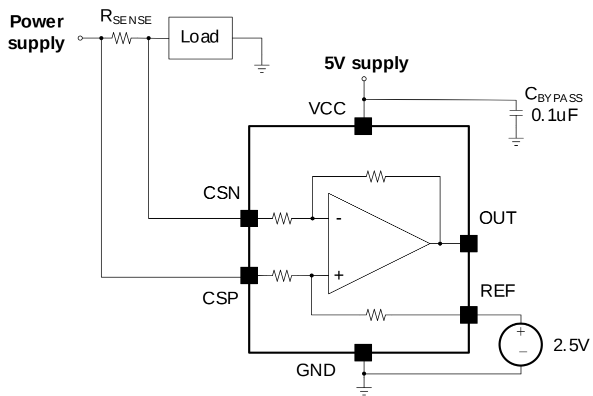


Figure 4. Bidirectional Current-sense Application

Like any differential amplifier, the common mode rejection ratio of the SY2A55105 is affected by any impedance present at the REF input. This problem will not exist when the REF pin is connected directly to most reference or power supplies. When using a resistor divider from the power supply or a reference voltage, the REF pin must be buffered by an OP AMP as Figure 5 shown.

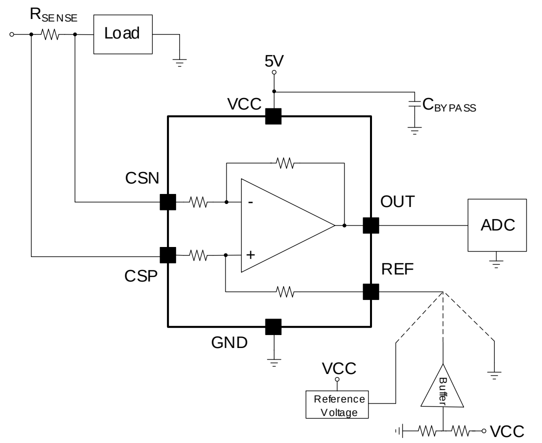


Figure 5. REF Pin Drive

In the system where using a differential input analog-to-digital converter (ADC) or using two separate single-ended input ADCs, the differential voltage of the OUT pin and the REF pin of the SY2A55105 can be directly collected. This detection method can eliminate the influence of external impedance on the REF input, where the REF pin can be driven directly with a divider resistor without going through the buffer. As shown in Figure 6.

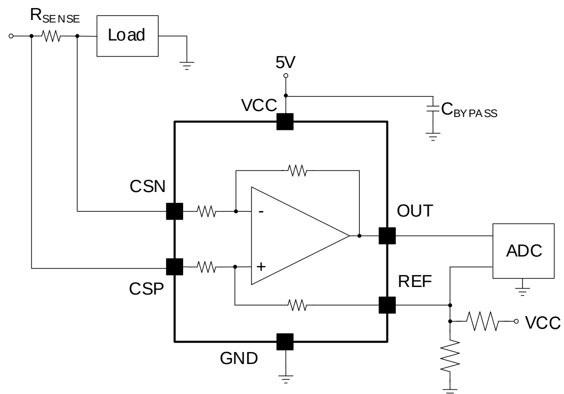


Figure 6. Sensing the SY2A55105 to Cancel the Effects of Impedance on the REF Input

Input Filtering

To improve the de-glitch ability and the system SNR (Signal to Noise Ratio), It's recommended to place a RC filter at the inputs pins is as below shows.

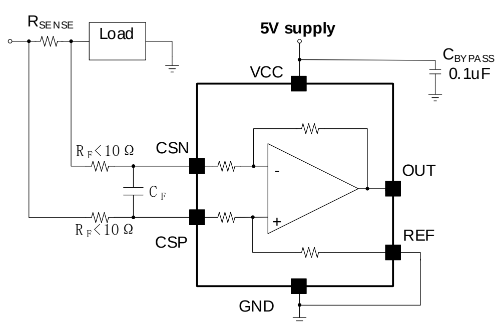


Figure 7. Filter at Input Pins

However, adding external series resistors creates additional errors in the measurement. When differential voltages are applied between the input pins of the SY2A55105, there will be a mismatch in the input bias current, resulting in an internal bias network. When additional external series filter resistors are added to the circuit, a mismatch in the bias current will result in a mismatch of the voltage drop across the filter resistors. This mismatch produces a differential error voltage that is subtracted from the voltage generated at the shunt resistor. This error results in the voltage at the input pin of the device is different than the voltage generated across the shunt resistor. Without additional series resistance, the mismatch of input bias current has little effect on device operation. To reduce the impact on the accuracy, the value of these series resistors should be less than 10 Ω.

The amount of error that these external filter resistors add to the measurement can be calculated using Equation 1.

$$GainError=\left(\frac{10000}{6.88\times R_F+10000}-1\right)\times 100\%$$

For example, using R_F =10Ω for external series resistance will results in a Gain error = -0.68%.

Selecting R_{SENSE}

The design of the current-sense resistor R_{SENSE} is dependent of the measured current, the maximum current-sense voltage range between CSP and CSN, the reference voltage VREF and the power voltage VCC.

For the unidirectional current application, assuming the measured current range is 0A ~ I_{maxP}, because the maximum current-sense voltage range of the CSP pin and the CSN pin are 1mV ~ 45mV, the maximum current-sense resistor R_{max1} for the input limit is 45mV/I_{maxP}.

But because pin OUT output voltage is clamped between GND and VCC-0.2V, the maximum current-sense resistor R_{max2} for the output limit is (VCC-0.2V-V_{REF})/100/I_{maxP}.

So the smaller value of R_{max1} and R_{max2} can be chosen as the maximum available current-sense resistor value.

Unidirectional Application R_{SENSE} Design Table

1.Measured current range	0A ~ I_{maxP}
2.Maximum current-sense voltage range	1mV ~ 45mV
3.Maximum sensing resistor for input limit	R_{max1}=45mV/I_{maxP}
4.Maximum OUT pin output range	GND ~ VCC-0.2V
5.Maximum sensing resistor for output limit	R_{max2}= (VCC-0.2V -V_{REF})/100/I_{maxP}
6.Maximum available current-sense resistor	$R_{SENSE,max}$=MIN[R_{max1}, R_{max2}]

For the bidirectional current application, assuming the measured current range is -I_{maxN} ~ I_{maxP}, the maximum current-sense resistor R_{max1} for the input limit is the smaller value of 20mV/I_{maxN} and 20mV/I_{maxP}.

But because pin OUT output voltage is clamped between GND and VCC-0.2V, the maximum current-sense resistor R_{max2} for the output limit is the smaller value of V_{REF}/100/I_{maxN} and (VCC-0.2V-V_{REF})/100/I_{maxP}.

So the smaller value of R_{max1} and R_{max2} can be chosen as the maximum available current-sense resistor value.

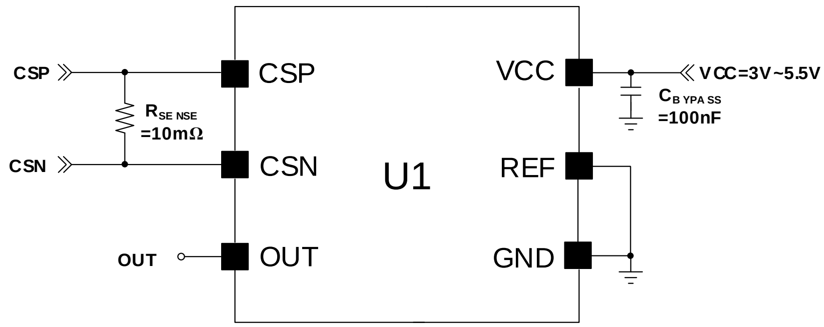
Bidirectional Application R_{SENSE} Design Table

1.Measured current range	-I_{maxN} ~ I_{maxP}
2.Maximum current-sense voltage range	-20mV ~ 20mV
3.Maximum sensing resistor for input limit	R_{max1}=MIN[20mV/I_{maxN}, 20mV/I_{maxP}]
4.Maximum OUT pin output range	GND ~ VCC-0.2V
5.Maximum sensing resistor for output limit	R_{max2}= MIN[V_{REF}/100/I_{maxN}, (VCC-0.2V-V_{REF})/100/I_{maxP}]
6.Maximum available current-sense resistor	$R_{SENSE,max}$=MIN[R_{max1}, R_{max2}]

A quick design table are shown as below:

Unidirectional Application (V_{REF}=0V)			**Bidirectional Application (V_{REF}=0.5×VCC)**		
I_{SENSE} Range	Recommended R_{SENSE}		I_{SENSE} Range	Recommended R_{SENSE}	
	VCC=5V	VCC=3.3V		VCC=5V	VCC=3.3V
0A ~ 1A	45mΩ	30mΩ	-1A ~ 1A	20mΩ	14mΩ
0A ~ 2A	22.5mΩ	15mΩ	-2A ~ 2A	10mΩ	7mΩ
0A ~ 3A	15mΩ	10mΩ	-4A ~ 4A	5mΩ	3.5mΩ
0A ~ 5A	9mΩ	6mΩ	-5A ~ 5A	4mΩ	2.5mΩ
0A ~ 10A	4.5mΩ	3mΩ	-10A ~ 10A	2mΩ	1.4mΩ

Application Schematic



BOM List

Designator	Description	Part Number	MFR
C_{BYPASS}	100nF/50V/X7R, 0603	GCJ188R71H104KA12D	muRata
R_{SENSE}	10mΩ/1W, 2512, 1%	RL2512FK-070R01L	YAGEO

Layout Guidelines

Using a Kelvin connection to connect the input pins to the current-sense resistor RSENSE. Due to the low resistance values of RSENSE, poor PCB routing often leads to additional parasitic resistance between input pins, resulting in additional errors that cannot be ignored, this connection technique ensures that only RSENSE impedance is detected between the input pins. Minimizing the loop formed by these connections.

Place the bypass capacitor (a 0.1μF MLCC is recommended) very near VCC and GND.

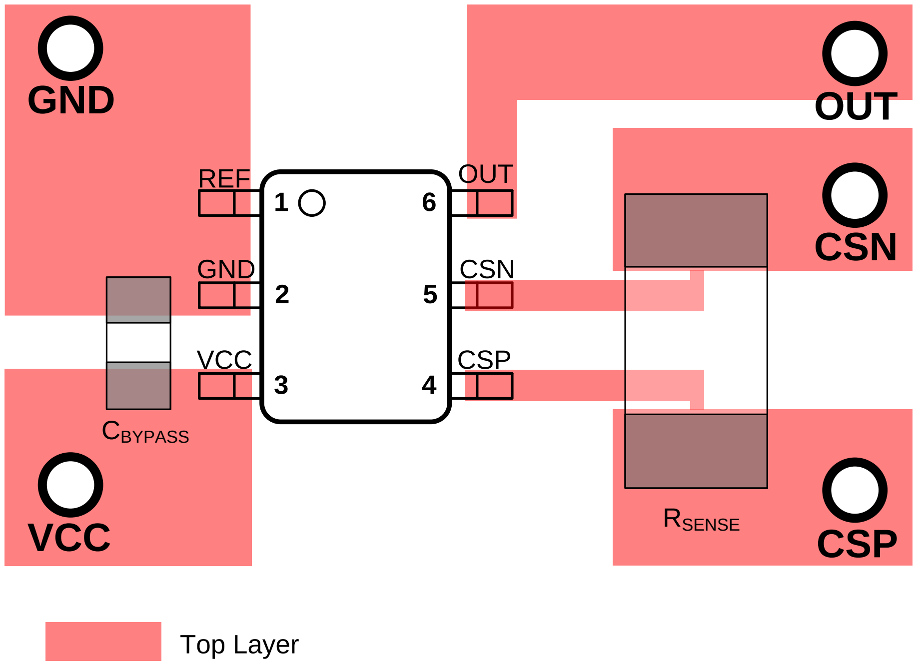
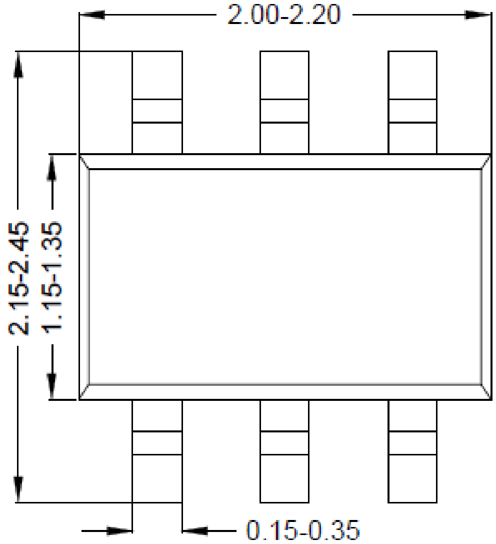
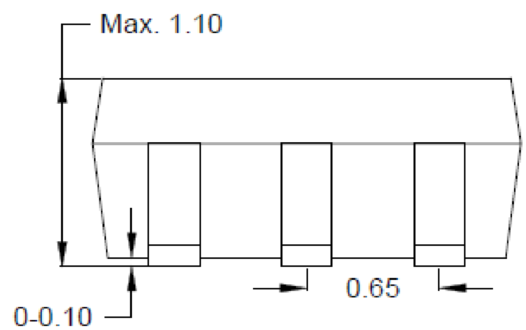


Figure 8. Recommended Layout

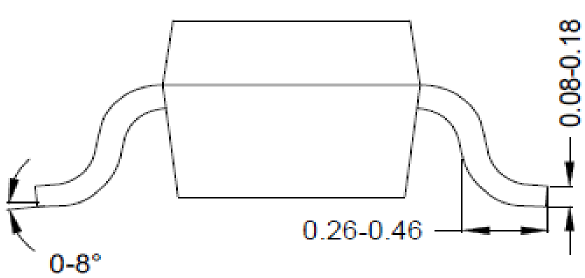
SOT363 Package Outline Drawing



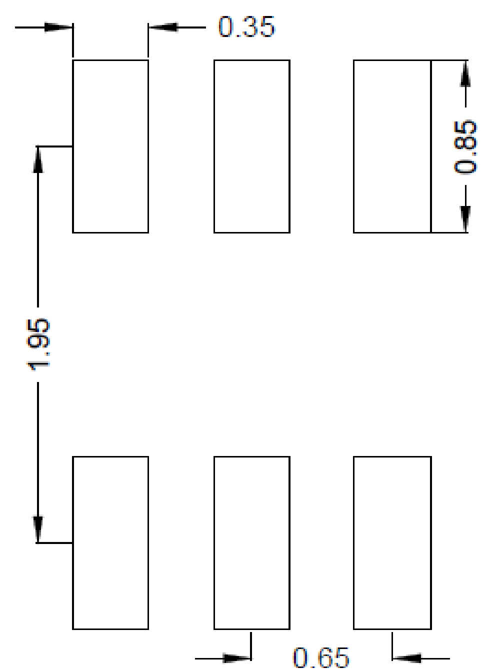
Top view



Side view A



Side view B

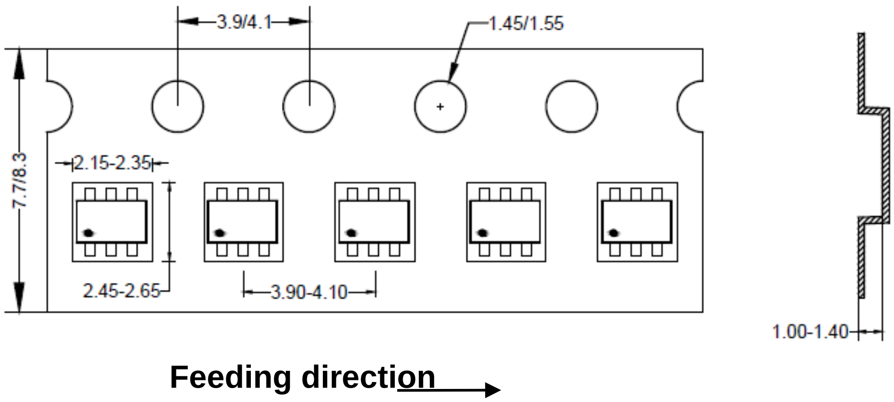


Recommended PCB layout
(Reference only)

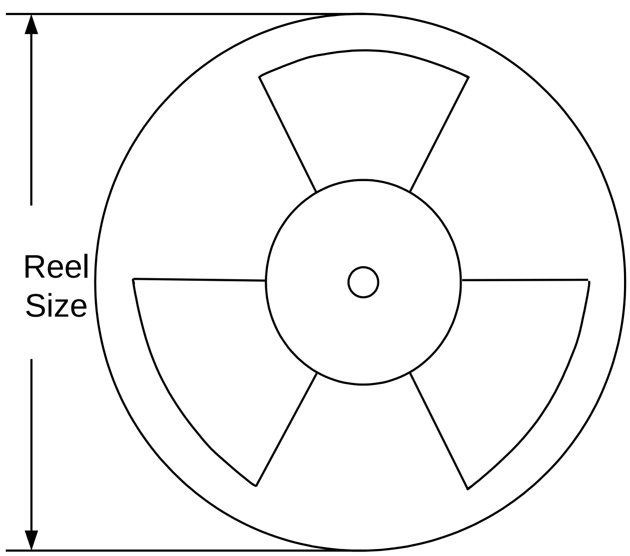
Notes: All dimension in millimeter and exclude mold flash & metal burr.

Taping & Reel Specification

1. Package Orientation



2. Carrier Tape & Reel Specification for Packages



Package types	Tape width (mm)	Pocket pitch(mm)	Reel size (Inch)	Trailer length(mm)	Leader length (mm)	Qty per reel
SOT363	8	4	7"	280	160	3000

3. Others: NA

Revision History

The revision history provided is for informational purpose only and is believed to be accurate, however, not warranted. Please make sure that you have the latest revision.

Date	Revision	Change
Nov. 20, 2020	Revision 0.9	Initial Release.
Nov. 20, 2021	Revision 1.0	Production Release.

IMPORTANT NOTICE

1. **Right to make changes.** Silergy and its subsidiaries (hereafter Silergy) reserve the right to change any information published in this document, including but not limited to circuitry, specification and/or product design, manufacturing or descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products are sold subject to Silergy's standard terms and conditions of sale.

2. **Applications.** Application examples that are described herein for any of these products are for illustrative purposes only. Silergy makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification. Buyers are responsible for the design and operation of their applications and products using Silergy products. Silergy or its subsidiaries assume no liability for any application assistance or designs of customer products. It is customer's sole responsibility to determine whether the Silergy product is suitable and fit for the customer's applications and products planned. To minimize the risks associated with customer's products and applications, customer should provide adequate design and operating safeguards. Customer represents and agrees that it has all the necessary expertise to create and implement safeguards which anticipate dangerous consequences of failures, monitor failures and their consequences, lessen the likelihood of failures that might cause harm and take appropriate remedial actions. Silergy assumes no liability related to any default, damage, costs or problem in the customer's applications or products, or the application or use by customer's third-party buyers. Customer will fully indemnify Silergy, its subsidiaries, and their representatives against any damages arising out of the use of any Silergy components in safety-critical applications. It is also buyers' sole responsibility to warrant and guarantee that any intellectual property rights of a third party are not infringed upon when integrating Silergy products into any application. Silergy assumes no responsibility for any said applications or for any use of any circuitry other than circuitry entirely embodied in a Silergy product.

3. **Limited warranty and liability.** Information furnished by Silergy in this document is believed to be accurate and reliable. However, Silergy makes no representation or warranty, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information. In no event shall Silergy be liable for any indirect, incidental, punitive, special or consequential damages, including but not limited to lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges, whether or not such damages are based on tort or negligence, warranty, breach of contract or any other legal theory. Notwithstanding any damages that customer might incur for any reason whatsoever, Silergy' aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the Standard Terms and Conditions of Sale of Silergy.

4. **Suitability for use.** Customer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of Silergy components in its applications, notwithstanding any applications-related information or support that may be provided by Silergy. Silergy products are not designed, authorized or warranted to be suitable for use in life support, life-critical or safety-critical systems or equipment, nor in applications where failure or malfunction of a Silergy product can reasonably be expected to result in personal injury, death or severe property or environmental damage. Silergy assumes no liability for inclusion and/or use of Silergy products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

5. **Terms and conditions of commercial sale**. Silergy products are sold subject to the standard terms and conditions of commercial sale, as published at http://www.silergy.com/stdterms, unless otherwise agreed in a valid written individual agreement specifically agreed to in writing by an authorized officer of Silergy. In case an individual agreement is concluded only the terms and conditions of the respective agreement shall apply. Silergy hereby expressly objects to and denies the application of any customer's general terms and conditions with regard to the purchase of Silergy products by the customer.

6. **No offer to sell or license**. Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights. Silergy makes no representation or warranty that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right. Information published by Silergy regarding third-party products or services does not constitute a license to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from Silergy under the patents or other intellectual property of Silergy.

For more information, please visit: www.silergy.com