SY24655QDQ

High- and Low-Side, Bidirectional, Zero-Drift, High-accuracy Current/Power Monitor with Accumulator and Programmable Alert

General Description

The SY24655 uses a 16-bit ADC (Analog to Digital Converter) along with a dedicated analog front-end to enable precise monitoring of current, voltage, and power of a separate rail. 16 addresses, configurable using two dedicated pins, enable multiple devices connected with application processor on the same I²C or SMBUS-compatible interface.

An integrated power accumulator can be used for average power calculations. Programmable calibration value, conversion times, and averaging when combined with an internal multiplier enable direct readouts of current in amperes and power in watts.

A flexible interrupt generation scheme enables alerting the host when the voltage, current or power levels on the monitored rail are below or above the configured thresholds.

The SY24655 can be used to monitor bus voltages that can vary from 0V to 36V, independent of the supply voltage.

Features

- Senses Bus Voltages from 0V to 36V
- High-Side or Low-Side Sensing
- Embedded 16bit ADC
- Reports Current, Voltage, and Power
- Integrated Power Accumulator for Average Power Monitoring
- High Accuracy:
  - 0.25% Gain Error (Max)
  - ±10μV Shunt Offset (Max)
- Low I_B: 1nA (Max)
- Configurable Averaging Options
- Abundant Alert Sources Setting
- 1.8V I²C, SMBus Compliant Interface
- 16 Programmable Addresses
- Operates from 2.7V to 5.5V Power Supply
- Industrial Temperature: –40°C~125°C
- Package: QFN3×3-16

Application

- Servers
- Telecom Equipment
- Computing
- Power Management
- Battery Chargers
- Power Supplies
- Test Equipment

Typical Application

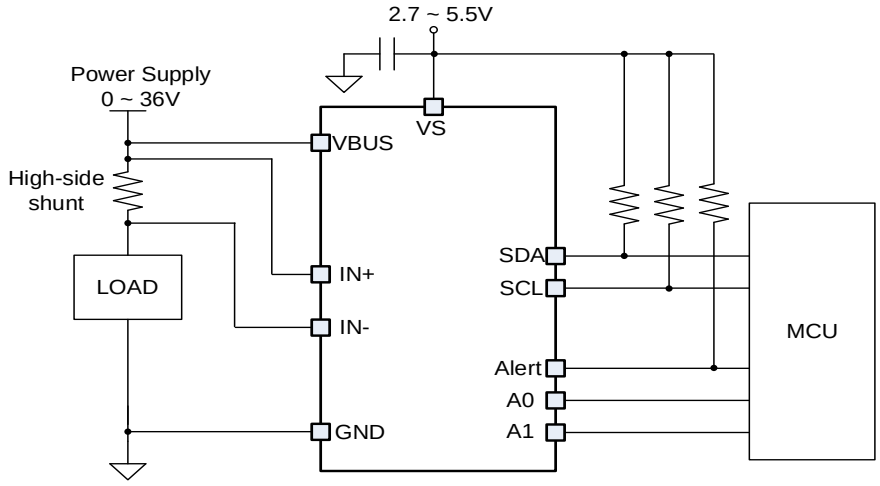

Figure 1. Typical Application Circuit

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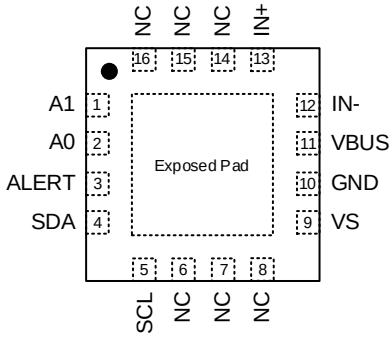
Ordering Information

Ordering Part Number	Package Type	Top Mark
SY24655QDQ	QFN3×3-16	**FYA*xyz***

x = year code, y = week code, z = lot number code.

Pinout (Top View)



(QFN3×3-16)

Pin Description

Pin No	Pin Name	Pin Description
1	A1	Address pin. Connect to GND, SCL, SDA, or VS.
2	A0	Address pin. Connect to GND, SCL, SDA, or VS.
3	ALERT	Multi-functional alert, open-drain output.
4	SDA	Serial bus data line, open-drain input/output.
5	SCL	Serial bus clock line, open-drain input.
6, 7, 8, 14, 15, 16	NC	No internal connection
9	VS	Power supply, 2.7 V to 5.5 V.
10	GND	Ground.
11	VBUS	Bus voltage input.
12	IN–	Negative differential voltage input. Connect to load side of shunt resistor.
13	IN+	Positive differential voltage input. Connect to supply side of shunt resistor.
	Thermal Pad	This pad can be connected to ground or left floating.

Block Diagram

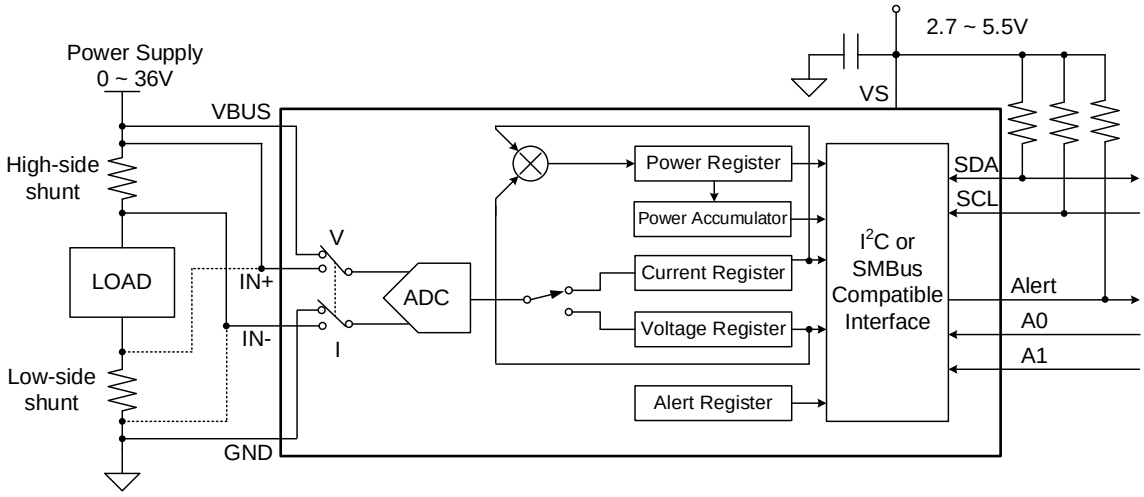


Figure 2. Block Diagram

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Absolute Maximum Ratings

Parameter (Note 1)	**Min**	**Max**	**Unit**
V_S	-0.3	6	V
V_{IN+} - V_{IN} (Differential)	-40	40	
(V_{IN+} + V_{IN-}) / 2 (Common-Mode)	-0.3	40	
VBUS	-0.3	40	
V_{SDA}, V_{SCL}, V_{A0}, V_{A1}	-0.3	6	
Input Current into any Pin		5	mA
Open-drain Digital Output Current		10	
Maximum Junction Temperature		150	°C
Storage Temperature Range	-65	150	
ESD: HBM (Human Body Model)	± 2000		V
ESD: CDM (Charged Device Model)	± 1000		V

Thermal Information

Parameter (Note 2)	**Max**	**Unit**
θ_{JA} Junction-to-Ambient Thermal Resistance	42	°C/W
θ_{JC} Junction-to-Case Thermal Resistance (top)	38	

Recommended Operating Conditions

Parameter (Note 3)	**Min**	**Max**	**Unit**
V_S		3.3	V
Common-mode, V_{IN+}, V_{IN-}		12	
Operation Temperature	-40	125	°C

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Electrical Characteristics

T_A = 25°C, VS = 3.3V, V_{IN+} = 12V, V_{SENSE} = (V_{IN+} – $V_{IN–}$) = 0mV and V_{VBUS} = 12V, unless otherwise specified.

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Input						
Shunt Voltage Input Range			-81.92		+81.9175	mV
Bus Voltage Input Range (Note 4)			0		36	V
Common-mode Rejection	CMRR	0V≤V_{IN+}≤36V	130	140		dB
Shunt Offset Voltage, RTI (Note 5)	V_{OS}			±2.5	±10	μV
Shunt Offset Voltage, RTI vs. Temperature		–40°C≤T_A≤125°C		0.02	0.1	μV/°C
Shunt Offset Voltage, RTI vs. Power Supply	PSRR	2.7≤VS≤5.5V		2.5		μV/V
Bus Offset Voltage, RTI	V_{OS}			±1.25	±10	mV
Bus Offset Voltage, RTI vs. Temperature		–40°C≤T_A≤125°C		10	40	μV/°C
Bus Offset Voltage, RTI vs. Power Supply	PSRR			0.5		mV/V
Input Bias Current (I_{IN+}, $I_{IN–}$ pins)	I_B				1	nA
VBUS Input Impedance				830		kΩ
DC Accuracy						
ADC Native Resolution				16		Bits
1 LSB Step Size		Shunt voltage		2.5		μV
		Bus voltage		1.25		mV
Shunt Voltage Gain Error				0.02	0.25	%
Shunt Voltage Gain Error vs. Temperature		–40°C≤T_A≤125°C		10	50	ppm/°C
Bus Voltage Gain Error				0.02	0.25	%
Bus Voltage Gain Error vs. Temperature		–40°C≤T_A≤125°C		10	50	ppm/°C
Power Gain Error		V_{BUS}=12V, V_{IN+} - V_{IN-}= -80~80mV		0.05	0.5	%
Power Gain Error vs. Temperature		–40°C≤T_A≤125°C		10	50	ppm/°C
Differential Nonlinearity				±0.1		LSB
ADC Conversion Time	t_{CT}	CT bit = 000		140	147	μs
		CT bit = 001		204	215	
		CT bit = 010		332	349	
		CT bit = 011		588	618	
		CT bit = 100		1.1	1.155	ms
		CT bit = 101		2.116	2.222	
		CT bit = 110		4.156	4.364	
		CT bit = 111		8.244	8.657	
SMBus						
SMBus Timeout (Note 6)				28	35	ms
Digital Input/Output						
Input Capacitance				3		pF
Leakage Input Current		0V≤V_{SCL}≤VS, 0V≤V_{SDA}≤VS, 0V≤V_{Alert}≤VS		0.1	1	μA
Address Pin(A0/A1) Bias Current		V_{A0}=VS, V_{A1}=VS		5.5	7	μA
High Level Input Voltage	V_{IH}		1.4		6	V
Low Level Input Voltage	V_{IL}		-0.5		0.4	V
Low Level Output Voltage, SDA, Alert	V_{OL}	I_{OL}=3mA	0		0.4	V
Hysteresis				200		mV
Power Supply						
Operating Supply Range			2.7		5.5	V
Quiescent Current (Note 7)	I_Q			320	370	μA
		Power down (Shutdown) Mode		3.7	5	
Power-on Reset Threshold	V_{POR}			2		V

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Note 1: Stresses beyond the “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: Package thermal resistance is measured in the natural convection at TA = 25˚C on an 8.5cm × 8.5cm two-layer Silergy Evaluation Board. θ_{JC} top is measured in accordance with JESD51-14.

Note 3: The device is not guaranteed to function outside its operating conditions.

Note 4: While the input range is 36V, the full-scale range of the ADC scaling is 40.96V. Do not apply more than 36V.

Note 5: RTI = Referred-to-input.

Note 6: SMBus timeout in the SY24655 resets the interface any time SCL is low for more than 28ms.

Note 7: A0=A1=GND or floating.

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Detailed Description

The SY24655 is a current, voltage, and power monitor which can be used to continuously monitor an independent power rail with a voltage between 0V and 36V. The SY24655 measures the differential voltage across a shunt resistor installed in series with a load, and the voltage of the rail. Based on the measured values reports values for current, voltage and power. The integrated power accumulator can be used for average power calculations. Programmable calibration values, conversion times, and averaging combined with the built-in multiplier enable direct readouts of current in amperes and power in watts.

A programmable interrupt function provides a flexible method to alert a host in the event of changes on the multiple monitored resources.

The functionality of the SY24655 can be roughly divided into three parts: ADC, Power Accumulator and Interrupt generation. The ADC operation is configured using the Configuration Register. The function of the Accumulator can be configured using the ACCUM_CONFIG Register. The Interrupt is configured using the Mask/Enable Register. Each block is described in more detail below.

ADC

The SY24655 integrates a highly accurate, 16-bit ADC. The SY24655 can convert the measurements to current, based on the calibration register value, and then calculate power.

The internal ADC has two operating modes, continuous and triggered, that determine how the ADC operates following shunt voltage and bus voltage conversions. When the device is in normal operating mode, the SY24655 will continuously convert a shunt voltage reading followed by a bus voltage reading. After the shunt voltage reading, the current value will be calculated. This current value is then used for calculating the power. These values are subsequently stored in an accumulator, and the measurement and calculation sequence repeats until the number of averages set in the configuration register is reached. Following every sequence, the present set of values measured and calculated are appended to previously collected values. After the averaging processing completes, the final values for the shunt voltage, bus voltage, current, and power will be updated in the corresponding registers that can then be read by a host using the I^2C bus.

In addition to the two operating modes (continuous and triggered), the internal ADC also has a power-down mode that reduces the quiescent current and turns off the current flowing into the device inputs, reducing the current consumption when the device is not being used.

The SY24655 offers programmable conversion times for both the shunt voltage and bus voltage measurements. The conversion times for these measurements can be programmed between 140μs and 8.244ms. A greater number of samples in the average or a longer conversion time enables the device to be more effective in reducing the effects of system noise affecting the measurements.

Power Accumulator

The SY24655 has an integrated power accumulator that records the total accumulated power, the corresponding sample count and rollover count. The accumulated power and sample count are accessible by reading the EIN Register and can be used for both energy metering and on-demand average power calculations.

The accumulator has two modes of operation, continuous and counting, which is determined and configured using the ACCUM_CONFIG Register. When the accumulator is in continuous mode, the power will continuously accumulate until the accumulated power overflows. In counting mode, the power continuously accumulates until the countdown set in the TIMER bits of ACCUM_CONFIG Register is reached, or the EIN Register overflows, and the accumulator re-starts at 0.

All powers, only positive powers, or only negative powers can be accumulated by setting the ACCUM_CONFIG Register. If the EIN accumulator encountered a value inconsistent with the selected mode of operation, the corresponding flag will become ‘1’.

If the accumulation function is expected to be restarted, the EIN Register can be cleared and then the accumulation function will be restored by setting the CLEAR_EIN bit of the ACCUM_CONFIG Register.

The energy accumulator can be configured using the ACCUM_CONFIG Register command to automatically clear with each READ_EIN command. The ability to clear the accumulator on read, switch ADC conversion mode or switch accumulation mode permits the device to be easily synchronized to an external timer, and allows the accumulator to always start at 0, thus eliminating the need to subtract the initial accumulated values and sample counts.

The EIN Register can also be cleared by setting the RST bit of Configuration Register to ‘0’. This method of clearing EIN Register is not recommended because this command also clears the Calibration Register used for scaling the accumulated power.

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Interrupt Generation

The SY24655 uses the Alert Limit Register in conjunction with the Mask/Enable Register to allow the Alert pin to be programmed to respond to a single user-defined event (Alert Function), or to other defined device notifications like: Conversion Ready, Accumulation Ready or EIN Overflow. Based on the function selected using the Mask/Enable register, the value written into the Alert Limit Register sets the corresponding threshold value that asserts the Alert pin.

The Alert pin allows for one of several available user-programmable thresholds to be monitored:

- Current Over-Limit (COL)
- Current Under-Limit (CUL)
- Bus Over-Voltage (BOV)
- Bus Under-Voltage (BUV)
- Power Over-Limit (POL)

The Alert pin is an open-drain output. This pin will be asserted when the function selected in the Mask/Enable Register meets the trigger criteria programmed into the Alert Limit Register. Only one of these alert functions can be enabled and monitored at a time. If multiple Alert Functions are enabled, the selected function in the highest significant bit position will take priority and determine the behavior of the Alert pin.

The Conversion Ready state of the device can be monitored using the Alert pin to inform the host when SY24655 has completed the current conversion cycle and is ready to begin initiate a new one. The Conversion Ready can be monitored along with one of the Alert Functions.

In accumulator counting mode, the Accumulation Ready Flag bit will be set after the times of accumulations is reached. The accumulation Ready Flag can be monitored using the Alert pin along with one of the Alert Functions.

The EIN Overflow Flag bit will be set after the EIN Register overflows, which includes accumulated power and sample count overflows. The EIN Overflow Flag can be monitored using the Alert pin along with one of the Alert Functions.

If an alert function is not used, the Alert pin can be left floating without impacting the operation of the device. If an alert function like the Conversion Ready, the Accumulation Ready or the EIN Overflow Flag will be enabled, after the Alert pin is asserted, the Mask/Enable Register must be read following the alert to determine the source of the alert.

If the Device Notifications are not needed, the Alert pin will only respond to an alert limit being triggered based on the Alert Function being enabled.

When the value in the Alert Limit Register is compared to the corresponding converted value, for example, if the alert function that is enabled is Current Over-Limit (COL), following every shunt voltage conversion, the value in the Alert Limit Register will be compared to the measured shunt voltage to determine if the measurement has exceeded the programmed limit, which translates to the current through the shunt exceeding the target threshold. The Alert Function Flag (AFF) asserts high any time the measured voltage exceeds the value programmed into the Alert Limit Register. In addition to the AFF being asserted, the Alert pin is asserted based on the configuration bits.

The Bus Voltage alert functions compare the measured bus voltage to the Alert Limit Register following every bus voltage conversion and assert the AFF bit and Alert pin if the condition is met.

The Power Over-Limit alert function is compared to the calculated power value following every bus voltage measurement conversion, and asserts the AFF bit and Alert pin if the programmed threshold is exceeded.

The polarity of the Alert pin and behavior can be controlled using the Alert Polarity Bit (APOL bit of the Mask/Enable Register).

If the Alert Latch is enabled, the AFF and Alert pin will remain asserted until either the Configuration Register is written to or the Mask/Enable Register is read.

If the Alert pin is not used in a design, it can be left floating.

Device Configuration

In order to report the current and power values properly, several registers should be configured using the following steps:

Step1: select the resolution of the Current Register (04h): Current_LSB.

The highest resolution for the Current Register (04h) can be obtained by using the smallest allowable Current_LSB based on the maximum expected current I_{MAX} as shown in Equation (1). Select a value for the Current_LSB to the nearest round number above this value to obtain the conversion of the Current Register (04h) and Power Register (03h) to amperes and watts respectively.

$$Current_LSB = \frac{I_{MAX}}{2^{15}} \qquad (1)$$

Where Current_LSB is the resolution of the Current Register (04h); I_{MAX} is the maximum expected monitored current.

In addition, the value of the shunt resistor is selected based on the shunt voltage measurement range and I_{MAX} with the intent to maximize the dynamic range.

Step2: Calibration Register (05h) Configuration

The Calibration Register enables the user to scale the Current Register (04h) and Power Register (03h) values.

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With the correct configuration of the Calibration Register (05h), the current flowing through the shunt resistor can be read out by simply multiply the Current Register and Current_LSB. The value of the Calibration Register (05h), CAL[R], can be calculated using the equation (2) below:

$$CAL[R] = \frac{2048 \times Shunt_LSB}{Current_LSB \times R_{Shunt}} \quad (2)$$

Where CAL[R] is the value of the Calibration Register (05h); Shunt_LSB is the resolution of the Shunt Voltage Register (01h), Shunt_LSB is 2.5μV/LSB; Current_LSB is the resolution of the Current Register (04h); R_{Shunt} is the shunt resistor.

After programming the Calibration Register, the Current Register (04h) and Power Register (03h) update accordingly based on the corresponding shunt voltage and bus voltage measurements on every measurement cycle. Until the Calibration Register is programmed, the Current Register (04h) and Power Register (03h) values will be zero.

Step3: Current Register (04h)

The value of the Shunt Register (01h) can be calculated using the equation (3)

$$Shunt[R] = \frac{Current \times R_{Shunt}}{Shunt_LSB} \quad (3)$$

In the device, the Current Register value is calculated based on the value of the Shunt Voltage Register (01h) and the Calibration Register(05h).

$$Current[R] = \frac{Shunt[R] \times CAL[R]}{2048} \quad (4)$$

Where Current[R] is the value of the Current Register (04h); Shunt[R] is the value of the Shunt Register (01h); CAL[R] is the value of the Calibration Register (05h)

The Current Register value represents the current in Amperes as described by the equation (5)

$$Current = Current[R] \times Current_LSB \quad (5)$$

Step4: Bus Voltage Register

The Bus Voltage is represented using equation (6)

$$Bus = Bus[R] \times Bus_LSB \quad (6)$$

Where Bus_LSB is the resolution of the Bus Voltage Register(02h), which is a fixed 1.25mV/LSB.

Step5: Power Register

The value of the Power Register (03h) is calculated based on the equation (7)

$$Power[R] = \frac{Current[R] \times Bus[R]}{20000} \quad (7)$$

Where Current[R] is the value of the Current Register (04h); Bus[R] is the value of the Bus Voltage Register (02h); Power[R] is the value of the Power Register(03h).

Based on equations (1)~(7), the resolution of the Power Register is fixed as 25 times of the resolution of the Current Register. The resulting power value obtained based on equation (8)

$$Power = Power[R] \times Power_LSB \quad (8)$$

Configuration Example

In Figure 3, a nominal 10A load creates a differential voltage of 20mV across a 2mΩ shunt resistor. The Bus Voltage for The SY24655 is measured at the external VBUS input pin, which in this example is connected to the IN– pin to measure the voltage level delivered to the load. In this example, the VBUS pin measures less than 12V because the voltage at the IN– pin is 11.98V as a result of the voltage drop across the shunt resistor.

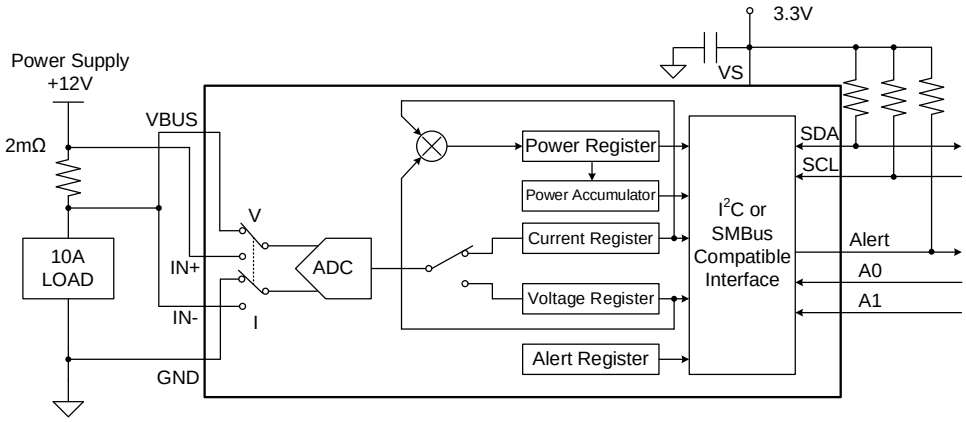

Figure 3. High-Side Sensing Circuit Application Example

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Assuming a maximum expected current of 15A, the Current_LSB is calculated to be 457.7μA/bit using Equation (1). The Current_LSB value could be rounded up to 500μA/Bit or 1mA/Bit, to simplify the conversion from the Current Register (04h) and Power Register (03h) to amperes and watts. For this example, a value of 1mA/bit was chosen for the Current_LSB. Using this value for the Current_LSB does trade a small amount of resolution for having a simpler conversion process. Using the equation (2) with a Current_LSB value of 1mA/bit and a shunt resistor value of 2mΩ results in a Calibration Register value of 2560 (A00h).

The Current Register (04h) is then calculated by multiplying the decimal value of the Shunt Voltage Register (01h) content by the decimal value of the Calibration Register and then dividing by 2048, as shown in Equation (4). For this example, the Shunt Voltage Register contains a value of 8,000 (representing 20mV), which is multiplied by the Calibration Register value of 2560 and then divided by 2048 to yield a decimal value for the Current Register (04h) of 10000 (2710h). Multiplying this value by 1mA/bit results in the original 10A current level to be measured.

The LSB for the Bus Voltage Register (02h) is a fixed 1.25mV/bit, which means that the 11.98V present at the VBUS pin results in a register value of 9584 (2570h). Note that the MSB of the Bus Voltage Register (02h) is always zero because the VBUS pin is only able to measure positive voltages.

The Power Register (03h) is calculated by multiplying the decimal value of the Current Register, 10000, by the decimal value of the Bus Voltage Register (02h), 9584, and then dividing by 20,000, as defined in Equation (7). For this example, the result for the Power Register (03h) is 4792 (12B8h). Multiplying this result by the power LSB (25 times Current_LSB) results in a power calculation of (4792 × 25mW/bit), or 119.82W. The power LSB has a fixed ratio to the Current_LSB of 25. For this example, 1mA/bit Current_LSB results in a power LSB of 25mW/bit. This ratio is internally programmed to ensure that the scaling of the power calculation is within an acceptable range. A manual calculation for the power being delivered to the load would use a bus voltage of 11.98V multiplied by the load current of 10A to give a result of 119.8W.

The following table lists the results for used for the register configuration, including measuring and calculating the values for current and power for a 10A load, V_{CM}=12V, R_{SHUNT}=2mΩ, and V_{VBUS}=12V.

Table 1. Calculating Current and Power

Register Name	Address	Contents	DEC	LSB	Value
Configuration Register	00h	4127h			
Shunt Register	01h	1F40h	8000	2.5μV	20mV
Bus Voltage Register	02h	2570h	9584	1.25mV	11.98V
Calibration Register	05h	0A00h	2560		
Current Register	04h	2710h	10000	1mA	10A
Power Register	03h	12B8h	4792	25mW	119.82W

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Programming

Serial Bus Address

To communicate with SY24655, the master must first address slave devices via a slave address byte. The slave address byte consists of seven address bits, and a direction bit that indicates whether the action is a read or write operation.

The device has two address pins, A0 and A1, which can be used to select between 16 possible addresses. The device samples the state of pins A0 and A1 on every bus communication. The state of the address pins has to be stable before any activity on the serial interface occurs.

A1	A0	Slave Address
GND	GND	1000000
GND	VS	1000001
GND	SDA	1000010
GND	SCL	1000011
VS	GND	1000100
VS	VS	1000101
VS	SDA	1000110
VS	SCL	1000111
SDA	GND	1001000
SDA	VS	1001001
SDA	SDA	1001010
SDA	SCL	1001011
SCL	GND	1001100
SCL	VS	1001101
SCL	SDA	1001110
SCL	SCL	1001111

Writing Command

Accessing a specific register on SY24655 is accomplished by writing the appropriate value to the register pointer. The value for the register pointer is the first byte to be transferred after the slave address byte with the R/W bit low. Every write operation to the device requires a value for the register pointer.

Writing to a register begins with the first byte transmitted by the master. This byte is the slave address, with the R/W bit low. The device then acknowledges receipt of a valid address. The next byte transmitted by the master is the address of the register which data is written to. This register address value updates the register pointer to the desired register. The next two bytes are written to the register addressed by the register pointer. The device acknowledges receipt of each data byte. The master may terminate data transfer by generating a start or stop condition.

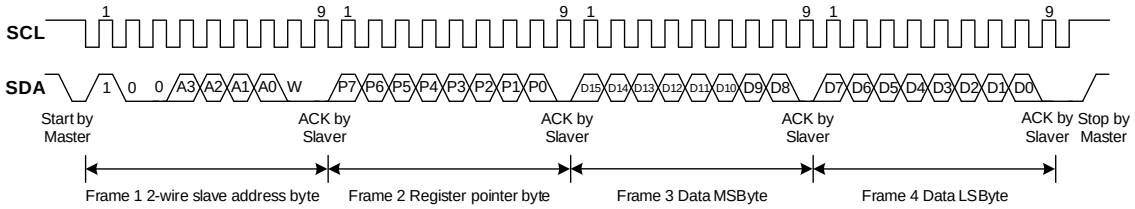

Figure 4. Timing Diagram for Write Word Format

Read Command

When reading from SY24655, a new value must be written to the register pointer, as shown in Figure 5. This write is accomplished by issuing the slaver address byte with the R/W bit low, followed by the register pointer byte. No additional data are required.

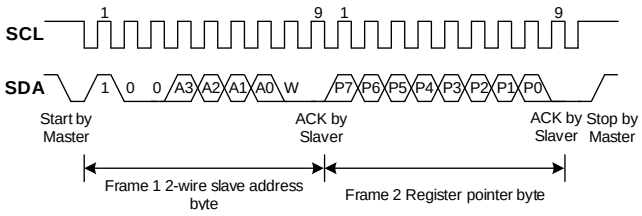

Figure 5. Typical Register Pointer Set

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The master then generates a start condition and sends the slave address byte with the R/W bit high to initiate the read command. The next byte is transmitted by the slave and is the most significant byte of the register indicated by the register pointer. This byte is followed by an Acknowledge from the master; then the slave transmits the least significant byte. The master acknowledges receipt of the data byte. The master may terminate data transfer by generating a Not-Acknowledge after receiving any data byte, or generating a start or stop condition.

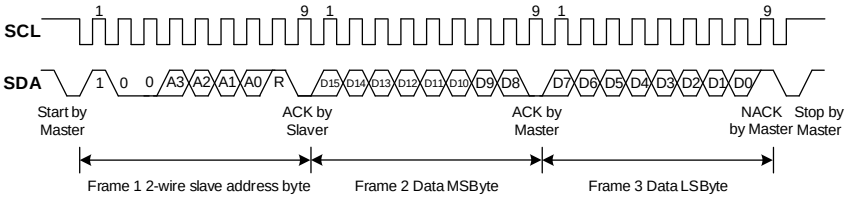

Figure 6. Timing Diagram for Read Word Format

High-Speed I²C Mode

When the bus is idle, both the SDA and SCL lines will be pulled high by the pull-up resistors. The master generates a start condition followed by a valid serial byte containing high-speed (HS) master code 00001XXX. This transmission is made in fast (400kHz) or standard (100kHz) (F/S) mode at no more than 400kHz. The device does not acknowledge the HS master code, but does recognize it and switches its internal filters to support 3.4MHz operation.

The master then generates a repeated start condition (a repeated start condition has the same timing as the start condition). After this repeated start condition, the protocol will be the same as F/S mode, except that transmission speeds up to 3.4MHz are allowed. Instead of using a stop condition, use repeated start conditions to secure the bus in HS-mode. A stop condition ends the HS-mode and switches all the internal filters of the device to support the F/S mode.

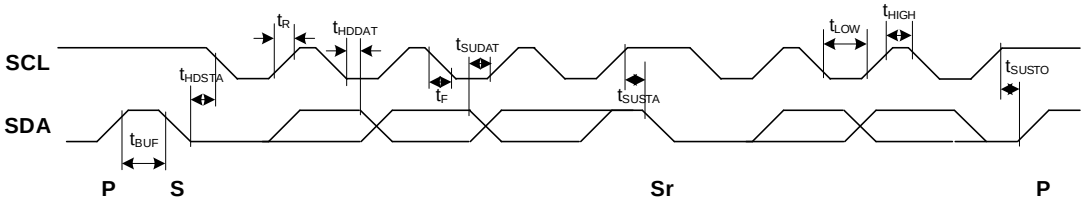

Figure 7. Bus Timing Diagram

Table 2. Bus Timing Diagram Definitions

Parameters	Symbol	Fast Mode		High-Speed Mode		Units
		Min	Max	Min	Max	
SCL operating frequency	f_{SCL}	0.005	0.4	0.005	3.4	MHz
Bus free time between stop and start conditions	t_{BUF}	600		160		ns
Hold time after repeated START condition. After this period, the first clock is generated.	t_{HDSTA}	100		100		ns
Repeated start condition setup time	t_{SUSTA}	100		100		ns
STOP condition setup time	t_{SUSTO}	100		100		ns
Data hold time	t_{HDDAT}	10	900	10	100	ns
Data setup time	t_{SUDAT}	100		20		ns
SCL clock low period	t_{LOW}	1300		200		ns
SCL clock high period	t_{HIGH}	600		60		ns
Data fall time	t_F		300		80	ns
Clock fall time	t_F		300		40	ns
Clock rise time	t_R		300		40	ns
Clock/data rise time for SCLK≤100kHz	t_R		1000			ns

SMBus Alert Response

The SY24655 can respond to the SMBus Alert Response address, which provides a quick fault identification for simple slave devices. When an Alert occurs, the master can broadcast the Alert Response slave address (0001 100) with the Read/Write bit set high. Following this Alert Response, any slave device that generates an alert identifies itself by acknowledging the Alert Response and sending its address on the bus.

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The Alert Response can activate several different slave devices simultaneously, similar to the I²C General Call. If more than one slave attempts to respond, bus arbitration rules apply. The losing device does not generate an Acknowledge and continues to hold the Alert line low until the interrupt is cleared.

The timing diagram for the SMBus Alert response operation is shown below.

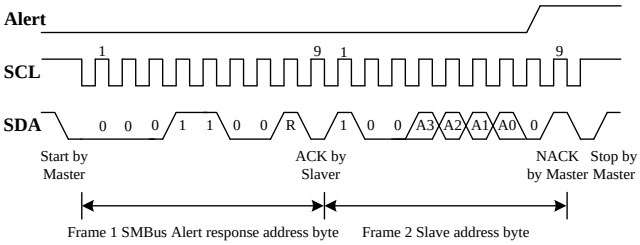

Figure 8. Timing Diagram for SMBus Alert

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Register Maps

SY24655 uses a bank of registers for holding configuration settings, status information and storing measurement and internal calculation results.
The following table summarizes the device registers. All 16-bit device registers can be accessed using two 8-bit bytes via the I²C interface.

Register Address (Hex)	Register Name	Function	Power-On Reset (Hex)	Type
00h	Configuration Register	All-register reset, shunt voltage and bus voltage ADC conversion times and averaging, operating mode.	4127h	R/W
01h	Shunt Voltage Register	Shunt voltage measurement data.	0000h	R
02h	Bus Voltage Register	Bus voltage measurement data.	0000h	R
03h	Power Register	Contains the value of the calculated power being delivered to the load.	0000h	R
04h	Current Register	Contains the value of the calculated current flowing through the shunt resistor.	0000h	R
05h	Calibration Register	Sets full-scale range and LSB of current and power measurements. Overall system calibration.	0000h	R/W
06h	Mask/Enable Register	Alert configuration and Conversion Ready flag.	0000h	R/W
07h	Alert Limit Register	Contains the limit value to compare to the selected Alert function.	0000h	R/W
0Ah	EIN Register	Retrieves the energy reading measurement.	00h, 00h, 00h, 00h, 00h, 00h	Block read
0Dh	ACCUM_CONFIG Register	Configures Control register for the accumulator function.	004Ch	R/W

Configuration Register (00h) (Read/Write)

The Configuration Register settings control the operating modes for the device. This register controls the conversion time settings for the shunt and bus voltage measurements as well as the averaging mode used. The operating mode that controls what signals are selected to be measured is also programmed in the Configuration Register.

The Configuration Register can be read from at any time without impacting or affecting the device settings or a conversion in progress. Writing to the Configuration Register halts any conversion in progress until the write sequence is completed resulting in a new conversion starting based on the new contents of the Configuration Register (00h). This halt prevents any uncertainty in the conditions used for the next completed conversion.

<table>
<tr><th>Bit No.</th><th>Bit Name</th><th>Por Value</th><th>Description</th></tr>
<tr><td>D15</td><td>RST</td><td>0</td><td>Reset Bit
Setting this bit to '1' generates a system reset that is the same as power-on reset. Reset all registers to default values; this bit self-clears.</td></tr>
<tr><td>D14</td><td></td><td>1</td><td></td></tr>
<tr><td>D13</td><td></td><td>0</td><td></td></tr>
<tr><td>D12</td><td></td><td>0</td><td></td></tr>
<tr><td>D11</td><td>AVG2</td><td>0</td><td rowspan="3">Averaging Mode
Determines the number of samples that are collected and averaged. The following table shows all the AVG bit settings and related number of averages for each bit setting. Shaded values are default.
<table>
<tr><th>AVG[2:0]</th><th>Number of Averages</th></tr>
<tr><td>000</td><td>1</td></tr>
<tr><td>001</td><td>4</td></tr>
<tr><td>010</td><td>16</td></tr>
<tr><td>011</td><td>64</td></tr>
<tr><td>100</td><td>128</td></tr>
<tr><td>101</td><td>256</td></tr>
<tr><td>110</td><td>512</td></tr>
<tr><td>111</td><td>1024</td></tr>
</table></td></tr>
<tr><td>D10</td><td>AVG1</td><td>0</td></tr>
<tr><td>D9</td><td>AVG0</td><td>0</td></tr>
<tr><td>D8</td><td>VBUSCT2</td><td>1</td><td rowspan="2">Bus Voltage Conversion Time
Sets the conversion time for the bus voltage measurement. The following table shows the VBUSCT bit options and related conversion times for each bit setting. Shaded values are default.
<table>
<tr><th>VBUSCT[2:0]</th><th>Conversion Time</th></tr>
<tr><td>000</td><td>140us</td></tr>
<tr><td>001</td><td>204us</td></tr>
</table></td></tr>
<tr><td>D7</td><td>VBUSCT1</td><td>0</td></tr>
</table>

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<table>
<tr><td>D6</td><td>VBUSCT0</td><td>0</td><td>
<table>
<tr><td>010</td><td>332us</td></tr>
<tr><td>011</td><td>588us</td></tr>
<tr><td>100</td><td>1.1ms</td></tr>
<tr><td>101</td><td>2.116ms</td></tr>
<tr><td>110</td><td>4.156ms</td></tr>
<tr><td>111</td><td>8.244ms</td></tr>
</table>
</td></tr>
<tr><td>D5</td><td>VSHCT2</td><td>1</td><td rowspan="3">Shunt Voltage Conversion Time
Sets the conversion time for the shunt voltage measurement. The following table shows the VSHCT bit options and related conversion times for each bit setting. Shaded values are default.
<table>
<tr><th>VSHCT[2:0]</th><th>Conversion Time</th></tr>
<tr><td>000</td><td>140us</td></tr>
<tr><td>001</td><td>204us</td></tr>
<tr><td>010</td><td>332us</td></tr>
<tr><td>011</td><td>588us</td></tr>
<tr><td>100</td><td>1.1ms</td></tr>
<tr><td>101</td><td>2.116ms</td></tr>
<tr><td>110</td><td>4.156ms</td></tr>
<tr><td>111</td><td>8.244ms</td></tr>
</table>
</td></tr>
<tr><td>D4</td><td>VSHCT1</td><td>0</td></tr>
<tr><td>D3</td><td>VSHCT0</td><td>0</td></tr>
<tr><td>D2</td><td>MODE2</td><td>1</td><td rowspan="3">Operating Mode
Selects continuous, triggered, or power-down mode of operation. These bits default to continuous shunt and bus measurement mode. The mode settings are shown as below. Shaded values are default.
<table>
<tr><th>MODE[2:0]</th><th>Mode</th></tr>
<tr><td>000</td><td>Power-Down (or Shutdown)</td></tr>
<tr><td>001</td><td>Shunt Voltage, Triggered</td></tr>
<tr><td>010</td><td>Bus Voltage, Triggered</td></tr>
<tr><td>011</td><td>Shunt and Bus, Triggered</td></tr>
<tr><td>100</td><td>Power-Down (or Shutdown)</td></tr>
<tr><td>101</td><td>Shunt Voltage, Continuous</td></tr>
<tr><td>110</td><td>Bus Voltage, Continuous</td></tr>
<tr><td>111</td><td>Shunt and Bus, Continuous</td></tr>
</table>
</td></tr>
<tr><td>D1</td><td>MODE1</td><td>1</td></tr>
<tr><td>D0</td><td>MODE0</td><td>1</td></tr>
</table>

Shunt Voltage Register (01h) (Read-Only)

The Shunt Voltage Register stores the current shunt voltage reading, V_{SHUNT}. Negative numbers are represented in two's complement format. Generate the two's complement of a negative number by complementing the absolute value binary number and adding 1. An MSB = '1' denotes a negative number.

If averaging is enabled, this register displays the averaged value.

Full-scale range = 81.92mV (decimal = 7FFF); LSB= 2.5μV.

Bit No.	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Bit Name	SIGN	SD14	SD13	SD12	SD11	SD10	SD9	SD8	SD7	SD6	SD5	SD4	SD3	SD2	SD1	SD0
POR Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bus Voltage Register (02h) (Read-Only)

The Bus Voltage Register stores the most recent bus voltage reading, VBUS. If averaging is enabled, this register displays the averaged value.

Full-scale range = 40.96V (decimal = 7FFF); LSB = 1.25mV.

Bit No.	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Bit Name	-	BD14	BD13	BD12	BD11	BD10	BD9	BD8	BD7	BD6	BD5	BD4	BD3	BD2	BD1	BD0
POR Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

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Power Register (03h) (Read-Only)

If averaging is enabled, this register displays the averaged value.

The Power Register LSB is internally programmed to equal 25 times the programmed value of the Current_LSB.

Bit No.	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Bit Name	PD15	PD14	PD13	PD12	PD11	PD10	PD9	PD8	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0
POR Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Current Register (04h) (Read-Only)

If averaging is enabled, this register displays the averaged value.

Bit No.	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Bit Name	CSIGN	CD14	CD13	CD12	CD11	CD10	CD9	CD8	CD7	CD6	CD5	CD4	CD3	CD2	CD1	CD0
POR Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Calibration Register (05h) (Read/Write)

This register provides the device with the value of the shunt resistor that is used to create the measured differential voltage. It also sets the resolution of the Current Register. Programming this register sets the Current_LSB and the Power_LSB. This register is also suitable to be used in system calibration.

Bit No.	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Bit Name	-	FS14	FS13	FS12	FS11	FS10	FS9	FS8	FS7	FS6	FS5	FS4	FS3	FS2	FS1	FS0
POR Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Mask/Enable Register (06h) (Read/Write)

The Mask/Enable Register selects the function that is enabled to control the Alert pin as well as how that pin functions. If multiple functions are enabled, the highest significant bit position Alert Function (D15-D11) takes priority and responds to the Alert Limit Register.

Bit No.	Bit Name	Por Value	Description
D15	COL	0	**Current Over-Limit** Setting this bit high configures the Alert pin to be asserted if the shunt voltage measurement following a conversion exceeds the value programmed in the Alert Limit Register.
D14	CUL	0	**Current Under-Limit** Setting this bit high configures the Alert pin to be asserted if the shunt voltage measurement following a conversion drops below the value programmed in the Alert Limit Register.
D13	BOL	0	**Bus Voltage Over-Voltage** Setting this bit high configures the Alert pin to be asserted if the bus voltage measurement following a conversion exceeds the value programmed in the Alert Limit Register.
D12	BUL	0	**Bus Voltage Under-Voltage** Setting this bit high configures the Alert pin to be asserted if the bus voltage measurement following a conversion drops below the value programmed in the Alert Limit Register.
D11	POL	0	**Power Over-Limit** Setting this bit high configures the Alert pin to be asserted if the Power calculation made following a bus voltage measurement exceeds the value programmed in the Alert Limit Register.
D10	CNVR	0	**Conversion Ready** Setting this bit high configures the Alert pin to be asserted when the Conversion Ready Flag, Bit 3, is asserted indicating that the device is ready for the next conversion.
D9	ACCUMR	0	**Accumulation Ready** Setting this bit high configures the Alert pin to be asserted when the Accumulation Ready Flag, Bit 5, is asserted indicating that the time of accumulations is reached in Accumulator Counting mode.
D8	EOF	0	**EIN Overflow** Setting this bit high configures the Alert pin to be asserted when the Accumulation Ready Flag, Bit 6, is asserted indicating that the EIN Register overflows.

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D7	-	0	
D6	EOFF	0	**EIN Overflow Flag** The EIN Overflow Flag bit is set after the EIN Register overflows. When the Alert Latch Enable bit is set to Latch mode, the EIN Overflow Flag bit clears only when the Mask/Enable, Register is read. When the Alert Latch Enable bit is set to Transparent mode, the EIN Overflow Flag bit is cleared, following the next conversion that does not result in an Alert condition.
D5	ACCUMRF	0	**Accumulation Ready Flag** The Accumulation Ready Flag bit is set after the times of accumulations is reached in Accumulator Counting mode. When the Alert Latch Enable bit is set to Latch mode, the Accumulation Ready Flag bit clears only when the Mask/Enable Register is read. When the Alert Latch Enable bit is set to Transparent mode, the Accumulation Ready Flag bit is cleared following the next conversion that does not result in an Alert condition.
D4	AFF	0	**Alert Function Flag** While only one Alert Function can be monitored at the Alert pin at a time, the Conversion Ready can also be enabled to assert the Alert pin. Reading the Alert Function Flag following an alert allows the user to determine if the Alert Function was the source of the Alert. When the Alert Latch Enable bit is set to Latch mode, the Alert Function Flag bit clears only when the Mask/Enable Register is read. When the Alert Latch Enable bit is set to Transparent mode, the Alert Function Flag bit is cleared following the next conversion that does not result in an Alert condition.
D3	CVRF	0	**Conversion Ready Flag** Although the device can be read at any time, and the data from the last conversion is available, the Conversion Ready Flag bit is provided to help coordinate one-shot or triggered conversions. The Conversion Ready Flag bit is set after all conversions, averaging, and multiplications are complete. Conversion Ready Flag bit clears under the following conditions: 1.) Writing to the Configuration Register (except for Power-Down selection) 2.) Reading the Mask/Enable Register
D2	OVF	0	**Math Overflow Flag** This bit is set to '1' if an arithmetic operation resulted in an overflow error. It indicates that current and power data may be invalid.
D1	APOL	0	**Alert Polarity bit; sets the Alert pin polarity.** 1 = Inverted (active-high open collector) 0 = Normal (active-low open collector) (default)
D0	LEN	0	**Alert Latch Enable** Configures the latching feature of the Alert pin and Alert Flag bits. 1 = Latch enabled 0 = Transparent (default) When the Alert Latch Enable bit is set to Transparent mode, the Alert pin and Flag bit resets to the idle states when the fault has been cleared. When the Alert Latch Enable bit is set to Latch mode, the Alert pin and Alert Flag bit remains active following a fault until the Mask/Enable Register has been read.

Alert Limit Register (07h) (Read/Write)

The Alert Limit Register contains the value used to compare to the register selected in the Mask/Enable Register to determine if a limit has been exceeded.

Bit No.	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Bit Name	AUL15	AUL14	AUL13	AUL12	AUL11	AUL10	AUL9	AUL8	AUL7	AUL6	AUL5	AUL4	AUL3	AUL2	AUL1	AUL0
POR Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

EIN Register (0Ah) (Read)

EIN Register is a command that returns information that the host can use to calculate energy or to average input power consumption. Six bytes of data are returned by this command. The first two bytes are the 16-bit, unsigned output of the internal accumulator that continuously sums samples of the instantaneous input power. The third data byte is a count of the rollover events for the accumulator. This byte is an unsigned integer indicating the number of times that the accumulator has rolled over from the maximum positive value (FFFFh) to zero. The last three data bytes are a 24-bit unsigned integer that counts the number of samples of the instantaneous input power accumulated.

The combination of the accumulator and the rollover count can overflow within a few seconds depending on the ADC conversion time. The host software must detect and appropriately handle this overflow. Similarly, the sample count value overflows, but this event only occurs one time every few hours, when using 1ms ADC conversion time.

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To convert the data obtained in the EIN Register command to average power, first convert the accumulator and rollover count to an unsigned integer.
Total Accumulated Unscaled Power (Accumulator_24) = (rollover_count × 2^{16}) + Accumulator
The overflow detection and handling is done using the 24 bits of accumulator data and the sample count. As shown in the following formula, data from the previous calculation must be saved and used in this calculation to obtain the unscaled average power. The following table lists the definitions for this command.

$$\frac{\text{Accumulator_24[n]} - \text{Accumulator_24[n-1]}}{\text{Sample_count [n]} - \text{Sample_count[n-1]}}$$

Where

- accumulator_24 [n] = Overflow corrected, 24-bit accumulator data from this read
- Sample_count [n] = Sample count data from this read
- accumulator_24[n-1] = Overflow corrected 24-bit accumulator data from the previous read
- Sample_count [n-1] = Sample count data from the previous read
- Unscaled average power is now in the same units as the data from the READ_PIN command

EIN Register Definitions

Byte	Meaning	Default
6	Sample count high byte	0
5	Sample count mid byte	0
4	Sample count low byte	0
3	Power accumulator rollover count	0
2	Power accumulator high byte	0
1	Power accumulator low byte	0

When the average power is calculated over a known number of samples, energy can be calculated by taking the product of the average power and the time interval for that average. The time interval can be externally measured or calculated by multiplying the number of samples reported by the ADC conversion time, inclusive of any device averaging modes. Calculating the energy consumption using the ADC conversion time can result in a 10% error in the energy reading because of the variations of the internal sampling oscillator frequency. For increased energy measurement precision, using a higher accuracy external time measurement method is recommended.
The energy accumulator can be configured using the ACCUM_CONFIG Register command to automatically clear on each READ_EIN(D1-D0,0Dh) command. The ability to clear the accumulator on a read permits the device to be easily synchronized to an external timer and allows the accumulator to always start at 0, thus eliminating the need to subtract the initial accumulated values and sample counts.
The READ_EIN(D1-D0,0Dh) power accumulator can also be cleared by issuing a CLEAR_EIN(D0,0Dh) command or RST(D15,00h) command. Clearing the power accumulator with the RST(D15,00h) command is not recommended because this command also clears the calibration register used to scale the accumulated power.

ACCUM_CONFIG Register (0Dh) (Read/Write)

This register configures various behaviors of the device in regards to data communications and alerts.

Bit No.	Bit Name	POR Value	Description
D15	EIN_Status	0	0 = All values added to the EIN accumulator match the setting of EIN_ACCUM 1 = The EIN accumulator encountered a value inconsistent with the selected mode of operation.
D14	ACCUM_MODE	0	1 = Accumulator Counting mode 0 = Accumulator Continuous mode
D13	EIN_ACCUM	00	00 = All powers are accumulated. 01 = All the positive powers are accumulated.the sample count continues to increment for negative values. 10 = All the negative powers are accumulated.the sample count continues to increment for positive values. 11 = All signed powers are accumulated.
D12			

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D11	Switch_ADC_ Mode auto clear	0	Set the mode of switching the ADC conversion mode. 0 = Clear the EIN Register and then start the accumlation function after switching the ADC conversion mode. 1 = Not clear the EIN Register and then continue to accumlate after switching the ADC conversion mode.
D10	READ_EIN auto clear	0	0 = Does not clear the sample count and accumulator after read. 1 = Clear the sample count and accumulator after read.
D9	TIMER	000	Set the times of accumulations in Accumulator Counting mode. 000 = 16 001 = 64 010 = 128 011 = 256 100 = 512 101 = 1024 110 = 2048 111 = 4096
D8			
D7			
D6-D2	MID	10011	The Manufacturer ID Register stores a unique identification number for the manufacturer.
D1	Switch_EIN_M ode auto clear	0	Set the mode of switching the EIN_ACCUM. 0 = Clear the EIN Register and then start the accumulation function after switching the EIN_ACCUM. 1 = Not clear the EIN Register and then continue to accumulate after switching the EIN_ACCUM.
D0	CLEAR_EIN	0	Set the mode of clearing the EIN Register. 0 = Do nothing. 1 = Clear the EIN Register and then start the accumulation function. When CLEAR_EIN bits are written to 1, this bit returns to 0 after the corresponding operation is finished.

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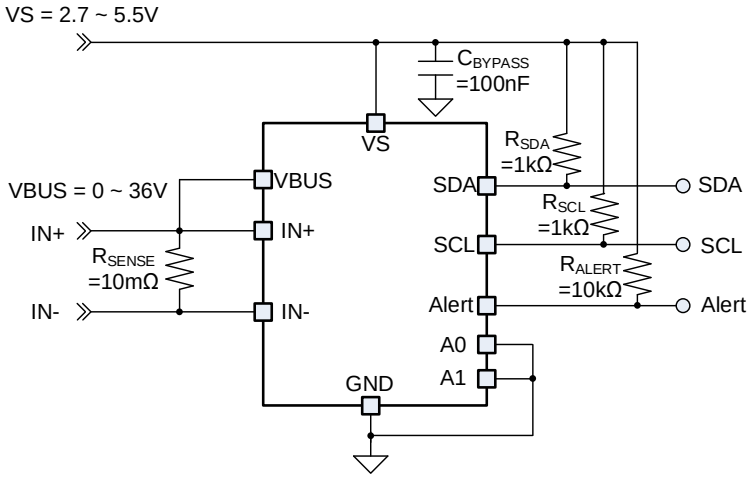
Application Schematic



BOM List

Designator	Description	Part Number	MFR
C_{BYPASS}	100nF/50V/X7R, 0603	GCJ188R71H104KA12D	muRata
R_{SENSE}	10mΩ/1W, 1%, 2512	RL2512FK-070R01L	YAGEO
R_{SDA}, R_{SCL}	1kΩ, 1%, 0603		
R_{ALERT}	10kΩ, 1%, 0603		

Layout Guidelines

Using a Kelvin connection to connect the input pins to the current-sensing resistor R_{SENSE}. Due to the low resistance values of R_{SENSE}, poor PCB routing often leads to additional parasitic resistance between input pins, resulting in additional errors that cannot be ignored, this connection technique ensures that only R_{SENSE} impedance is detected between the input pins. Minimizing the loop formed by these connections.

Place the bypass capacitor (a 0.1μF MLCC is recommended) very near VCC and GND.

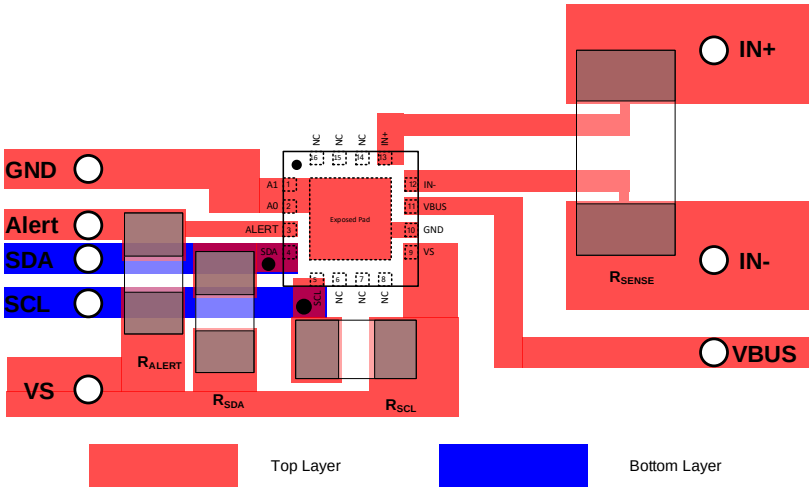


Figure 9. Recommended Layout

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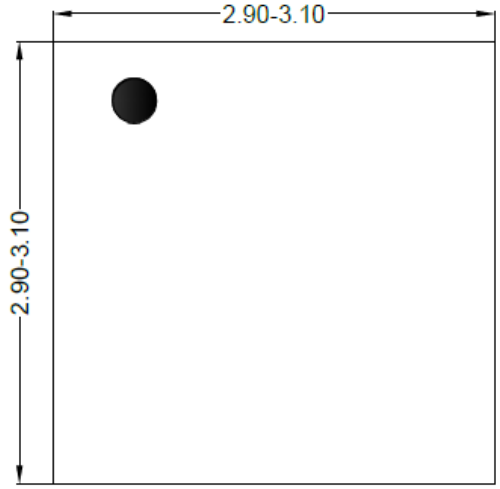
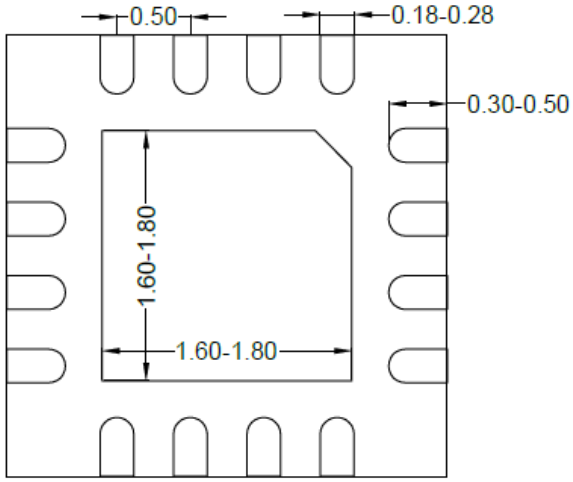
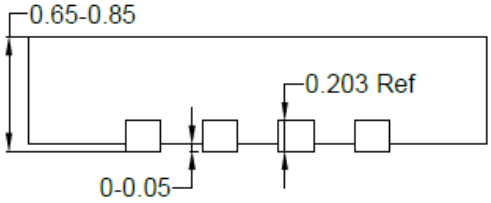
QFN3x3-16 Package outline & PCB Layout



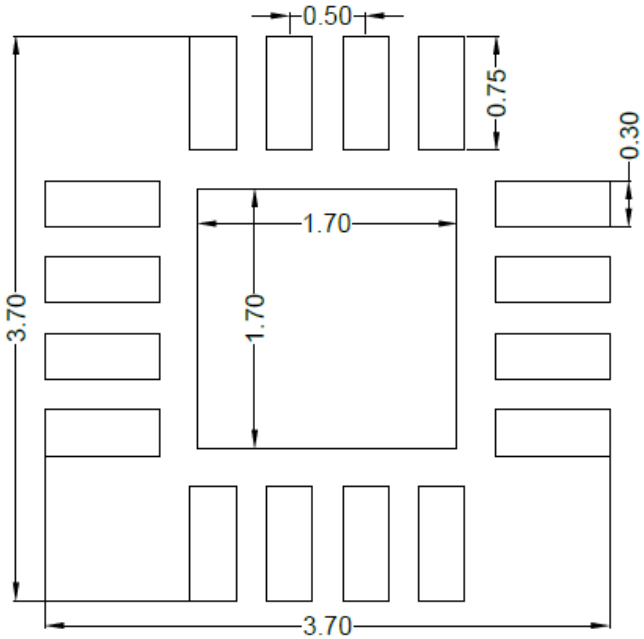
Top View



Bottom View



Side View



PCB layout (Recommended)

Notes: **All dimension in millimeter and exclude mold flash & metal burr.**

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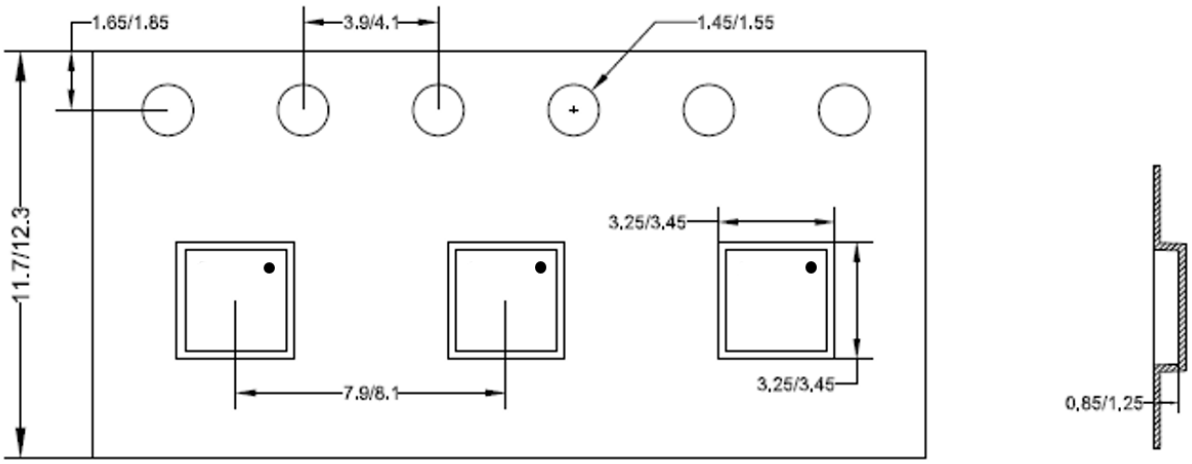
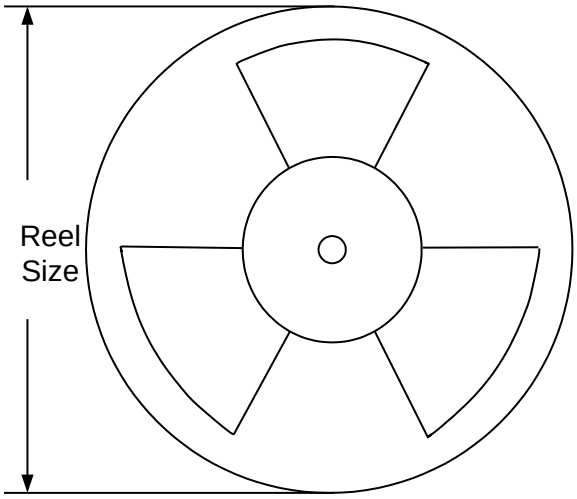
Taping & Reel Specification

1. QFN3×3-16 Taping Orientation



Feeding direction ⟶

2. Carrier Tape & Reel Specification for Packages



Package types	Tape width (mm)	Pocket pitch(mm)	Reel size (Inch)	Trailer length(mm)	Leader length (mm)	Qty per reel
QFN3×3	12	8	13"	400	400	5000

3. Others: NA

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Revision History

The revision history provided is for informational purpose only and is believed to be accurate, however, not warranted. Please make sure that you have the latest revision.

Date	Revision	Change
Nov. 21, 2022	Revision 0.9	Initial Release.
Aug.17, 2023	Revision 0.9A	Language improvements for clarity.
Nov.27, 2023	Revision 1.0	1.Add [Writing Command], [Read Command], [High-Speed I2C Mode], [SMBus Alert Response] above the chapter[Register Maps] 2. Update the Detailed Description: change "Step5" to "Step4" and "Step6" to "Step5" in chapter [Configuration for the Readouts]. 3. Change the test condition of Leakage Input Current in Electrical Characteristics from "$0V \le V_{SCL} \le VS$, $0V \le V_{SDA} \le VS$, $0V \le V_{Alert} \le VS$, $0V \le V_{A0} \le VS$, $0\ V \le V_{A1} \le VS$" to "$0V \le V_{SCL} \le VS$, $0V \le V_{SDA} \le VS$, $0V \le V_{Alert} \le VS$" 4. Add item "Address pin(A0/A1) Bias Current" in Electrical Characteristics

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