SY28637E

Single-channel, Adjustable Voltage Monitor in Ultra-small Package

General Description

The SY28637E device a very small supervisory circuit that monitor voltage greater than 500mV with a 1% threshold accuracy and offer adjustable delay time using external capacitor. The SY28637E has a logic enable pin to power on and off the output.

The SY28637E operates from 1.7V to 6.5V and has a typical quiescent current of 9μA with an open drain output rated at 18V. The SY28637E is available in an ultra-small DFN package and is fully specified over the temperature range of T_J=-40°C to 125°C.

Ordering Information

SY28637□(□□□)
- Package Code
- Optional Spec Code

Ordering Number	Package type	Note
SY28637EDTD	DFN1.45×1-6	--

Features

- Adjustable Threshold Down to 500mV
- Threshold Accuracy: 1% Over temperature
- Capacitor-adjustable Delay Time
- Low Quiescent Current: 9μA (typ.)
- External Enable Input
- Open Drain Output (Rated at 18V)
- Temperature Range: -40°C to 125°C
- RoHS Compliant and Halogen Free
- Compact Package Minimizes Board Space: DFN1.45mm×1.0mm - 6

Applications

- DSPs, Microcontrollers, and Microprocessors
- Notebook and Desktop Computers
- PDAs and Handheld Products
- Portable and Battery-powered Products
- FPGAs and ASICs

Typical Applications

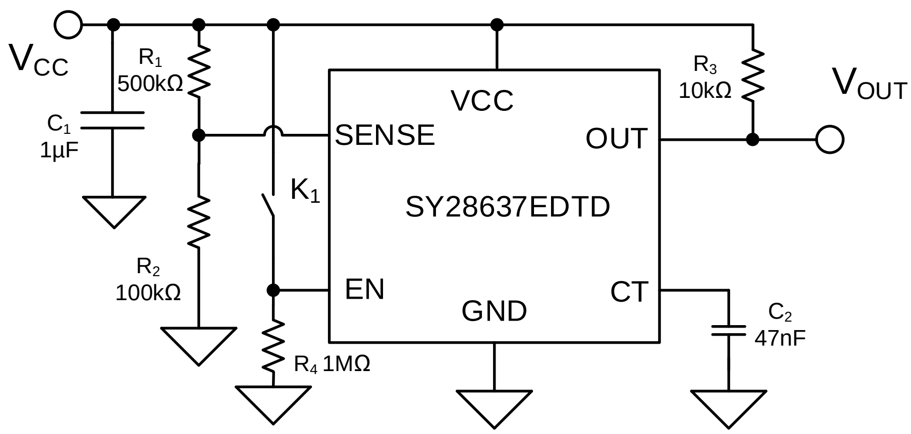
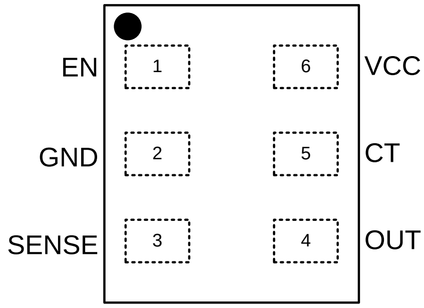


Figure1. Schematic Diagram

Pinout



(DFN1.45×1-6)

Top Mark: b*xyz* (device code: b, ***x=year code, y=week code, z= lot number code)***

Pin Name	Pin NO.	I/O	Pin Description
EN	1	I	Active high input. Driving EN low immediately makes OUT go low, independent of V_{SENSE}. With V_{SENSE} already above V_{IT+}, drive EN high to make OUT go high after the capacitor-adjust delay time.
GND	2		Ground.
SENSE	3	I	This pin is connected to the voltage that is monitored with the use of an external resister. The output asserts after the capacitor-adjustable delay time when VSENSE rises above 0.5V and EN is asserted. The output de-asserts after a minimal propagation delay (16µs) when VSENSE falls below V_{IT+} - V_{HYS}.
OUT	4	O	OUT is an open drain output that is immediately driven low after V_{SENSE} falls below (V_{IT+} - V_{HYS}) or the EN input is low. OUT goes high after the capacitor-adjustable delay time when V_{SENSE} is greater than V_{IT+} and the EN pin is high. Open drain device can be pulled up to 18V independent of VCC; Pull-up resister is required for this device.
CT	5	I	Capacitor-adjustable delay. The CT pin offers a user-adjustable delay time. Connecting this pin to a ground referenced capacitor sets the delay time for SENSE rising above 0.5V to OUT asserting. $t_{pd(r)}(s) = [C_{CT}(\mu F)\times 4] + 40\mu s$
VCC	6	I	Supply Voltage Input. Connect a 1.7V to 6.5V supply to VCC to power the device. It is good analog design practice to place a 0.1µF ceramic capacitor close to this pin.

Block Diagram

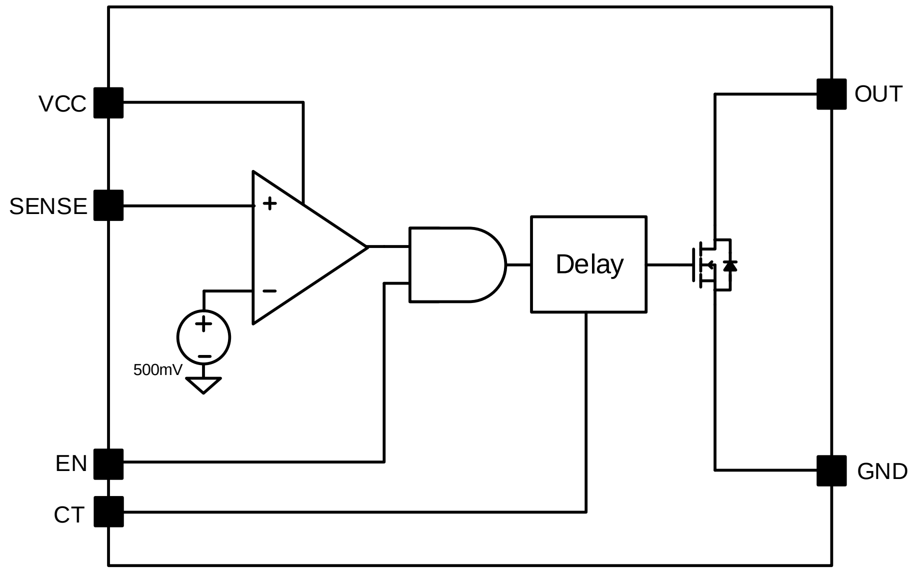


Figure2. Block Diagram

Absolute Maximum Ratings (Note 1)

VCC	-0.3V to 7V
CT	-0.3V to VCC + 0.3V
EN, SENSE	-0.3V to 7V
OUT (Open Drain)	-0.3V to 20V
OUT Current	±10mA
Power Dissipation, P_D @ T_A = 25°C	0.34W
Package Thermal Resistance (Note 2)	
θ_{JA}	293.8°C/W
θ_{JC}	165.1°C/W
Junction Temperature Range	-40°C to 125°C
Lead Temperature (Soldering, 10 sec.)	260°C
Storage Temperature Range	-65°C to 150°C

Recommended Operating Conditions (Note 3)

VCC	1.7V to 6.5V
CT	0V to 6.5V
EN, SENSE	0V to 6.5V
OUT (Open Drain)	0V to 18V
OUT Current	0.0003mA to 1mA

Electrical Characteristics

Over the operating temperature range of T_J = -40°C to 125°C, and 1.7V < V_{CC} < 6.5V, unless otherwise noted. Typical values are at T_J = 25°C and V_{CC} = 3.3V.

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Input Voltage Range	V_{CC}	T_J= -40°C to 125°C	1.7		6.5	V
Power On Reset Voltage	V_{POR}	V_{OL}(max) =0.2V, I_{OUT} =15μA (Note 4)		0.72		V
Supply Current (into VCC pin)	I_{CC}	V_{CC}=3.3V, T_A=25°C, No load		9	12	μA
		V_{CC}=3.3V, T_A=125°C, No load		12	14	μA
		V_{CC}=6.5V, T_A=25°C, No load		11	13.5	μA
		V_{CC}=6.5V, T_A=125°C, No load		14	16	μA
Positive-going Input Threshold Voltage	V_{IT+}	V_{SENSE} rising, -40°C <T_J < 125°C	0.495	0.5	0.505	V
Hysteresis Voltage	V_{HYS}	V_{SENSE} falling		5		mV
SENSE Input Current	I_{SENSE}	V_{SENSE} = 0V to V_{CC} (Note 5)	-15		15	nA
CT Pin Charge Current	I_{CT}		260	310	360	nA
CT Pin Comparator Threshold Voltage	V_{CT}		1.18	1.238	1.299	V
CT Pin Down Resistance	R_{CT}			200		Ω
Low-level Input Voltage	V_{IL}				0.4	V
High-level Input Voltage	V_{IH}		1.4			V
Under Voltage Lockout	V_{UVLO}	V_{CC} falling, (Note 6)	1.3		1.7	V
EN Leakage		EN = V_{CC} or GND	-100		100	nA
Low-level Output Voltage	V_{OL}	$V_{CC} \geq$ 1.2V, I_{SINK} = 90μA			0.3	V
		$V_{CC} \geq$ 2.25V, I_{SINK} = 0.5mA			0.3	V
		$V_{CC} \geq$ 4.5V, I_{SINK} = 1mA			0.4	V
Open-drain Output Leakage Current	$I_{LKG(OD)}$	V_{OUT} high impedance = 18V		20		nA

Timing Requirements

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
SENSE (Rising) to OUT Propagation Delay	$t_{PD(r)}$	V_{SENSE} rising, C_{CT} = open		40		μs
		V_{SESNE} rising, C_{CT} = 0.047μF		190		ms
Sense (Falling) to OUT Propagation Delay	$t_{PD(f)}$	V_{SENSE} falling		16		μs
Start-up Delay		(Note 7)		50		μs
EN Pin Minimum Pulse Duration	t_W		1			μs
EN Glitch Rejection	t_{EN_GLH}			100		ns
EN to OUT Delay Time (Output Disable)	t_{d_off}	EN deasserted to output deasserted		200		ns
EN to VOUT Delay Time	t_{d_ct}	EN asserted to output asserted delay, C_{CT}=open		20		μs
		EN asserted to output asserted delay, C_{CT}= 0.047μF		190		ms

Note 1: Stresses beyond the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: θ_{JA} is measured in the natural convection at T_A = 25°C on a low effective single layer thermal conductivity test board of JEDEC 51-3 thermal measurement standard.

Note 3: The device is not guaranteed to function outside its operating conditions

Note 4: The lowest supply voltage (VCC) at which output is active (OUT is low); t_{r_VCC} > 15 µs/V. Below V_{POR}, the output cannot be determined.

Note 5: Specified by design.

Note 6: When VCC falls below the UVLO threshold, the output de-asserts (OUT goes low). Below V(POR), the output cannot be determined

Note 7: During power on, V_{CC} must exceed 1.7V for at least 50 µs (plus propagation delay time, $t_{PD(r)}$) before output is in the correct state.

Sequence:

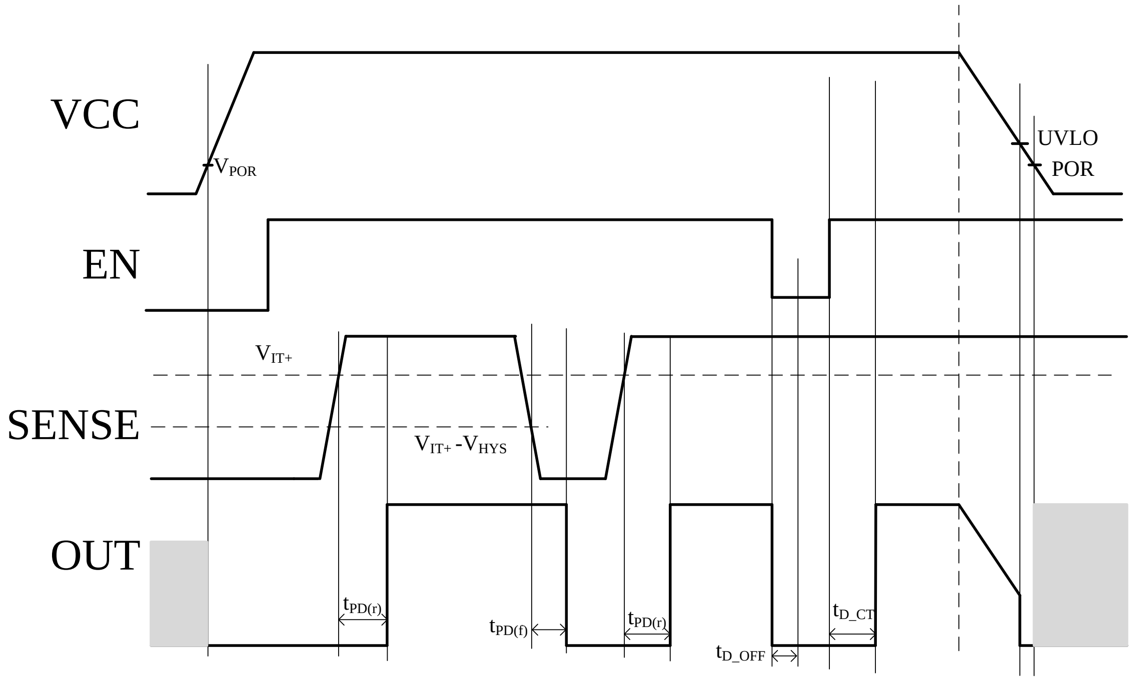
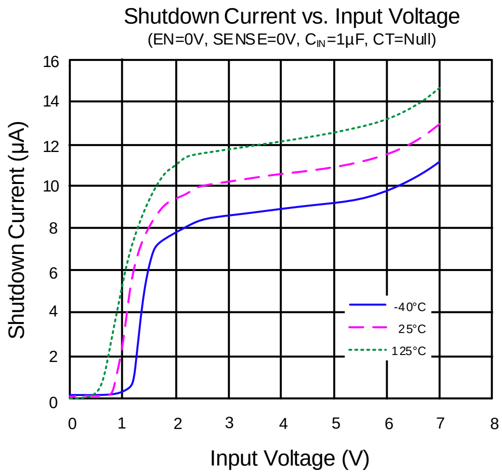
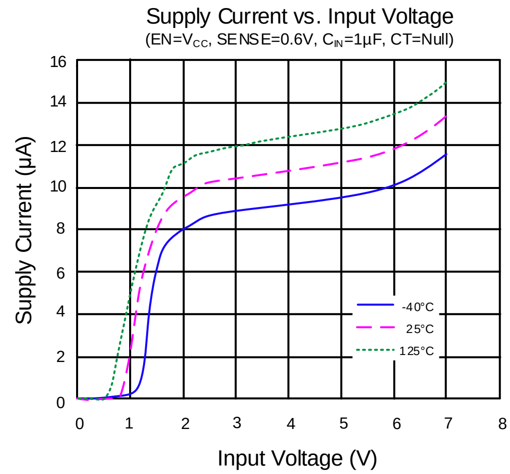
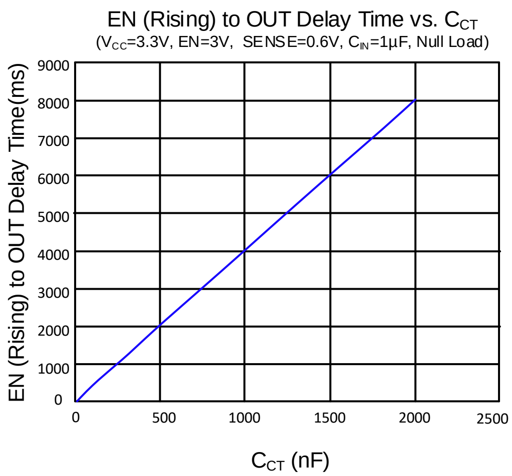


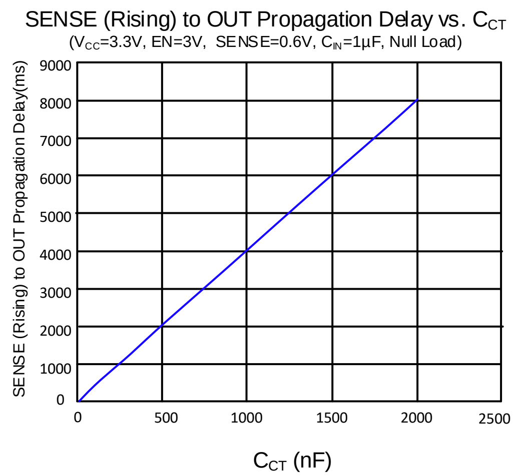
Figure3. SY28637E Sequence

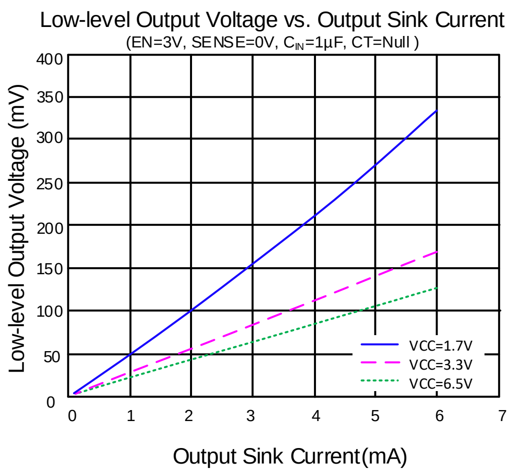
Typical Operating Characteristics

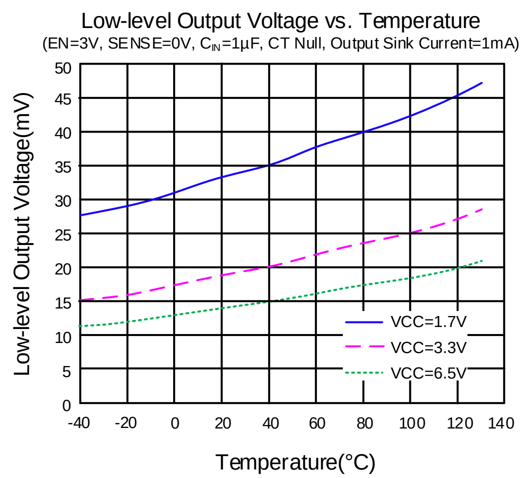


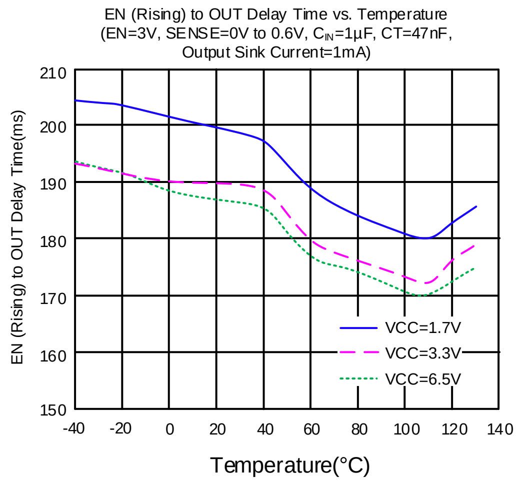


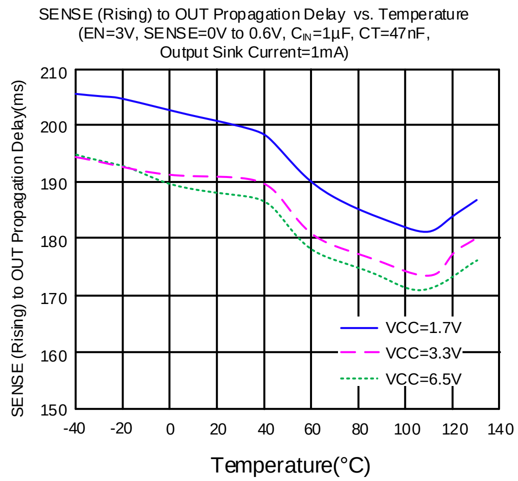


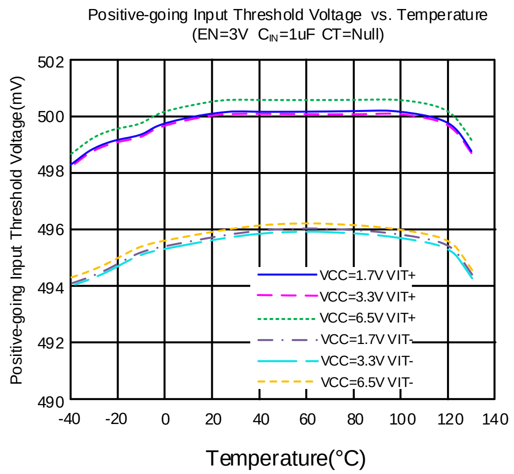


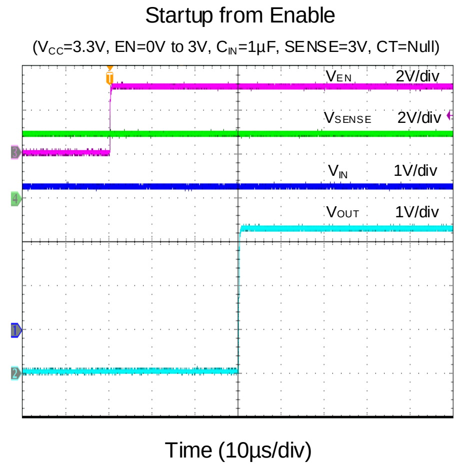


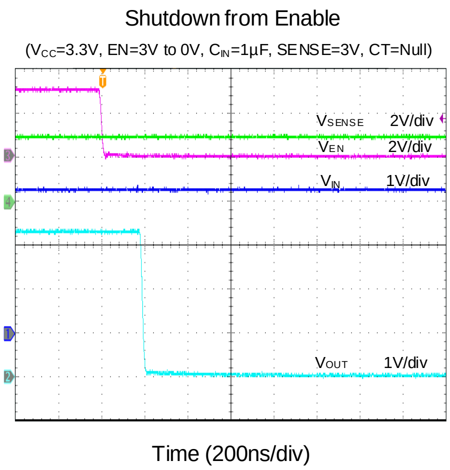


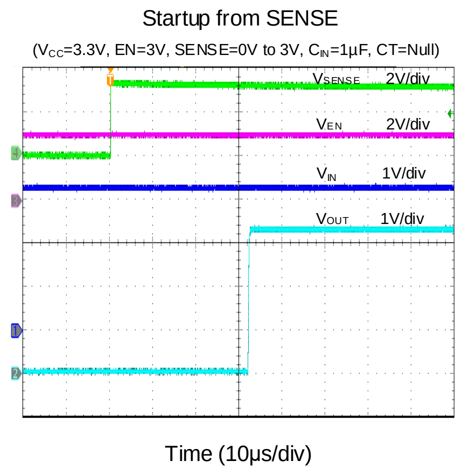

EN (Rising) to OUT Delay Time vs. Temperature
(EN=3V, SENSE=0V to 0.6V, CIN=1µF, CT=47nF,
Output Sink Current=1mA)
EN (Rising) to OUT Delay Time(ms)
Temperature(°C)
VCC=1.7V
VCC=3.3V
VCC=6.5V


SENSE (Rising) to OUT Propagation Delay vs. Temperature
(EN=3V, SENSE=0V to 0.6V, CIN=1µF, CT=47nF,
Output Sink Current=1mA)
SENSE (Rising) to OUT Propagation Delay(ms)
Temperature(°C)
VCC=1.7V
VCC=3.3V
VCC=6.5V


Positive-going Input Threshold Voltage vs. Temperature
(EN=3V CIN=1uF CT=Null)
Positive-going Input Threshold Voltage(mV)
Temperature(°C)
VCC=1.7V VIT+
VCC=3.3V VIT+
VCC=6.5V VIT+
VCC=1.7V VIT-
VCC=3.3V VIT-
VCC=6.5V VIT-

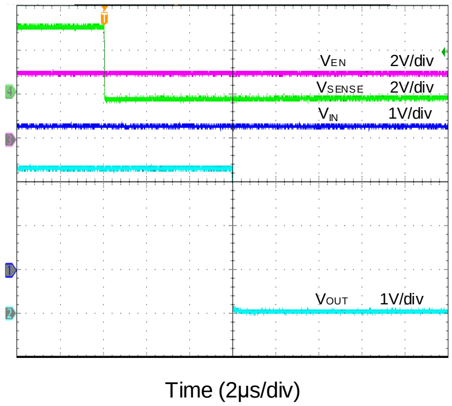

Startup from Enable
(VCC=3.3V, EN=0V to 3V, CIN=1µF, SENSE=3V, CT=Null)
VEN 2V/div
VSENSE 2V/div
VIN 1V/div
VOUT 1V/div
Time (10µs/div)


Shutdown from Enable
(VCC=3.3V, EN=3V to 0V, CIN=1µF, SENSE=3V, CT=Null)
VSENSE 2V/div
VEN 2V/div
VIN 1V/div
VOUT 1V/div
Time (200ns/div)


Startup from SENSE
(VCC=3.3V, EN=3V, SENSE=0V to 3V, CIN=1µF, CT=Null)
VSENSE 2V/div
VEN 2V/div
VIN 1V/div
VOUT 1V/div
Time (10µs/div)

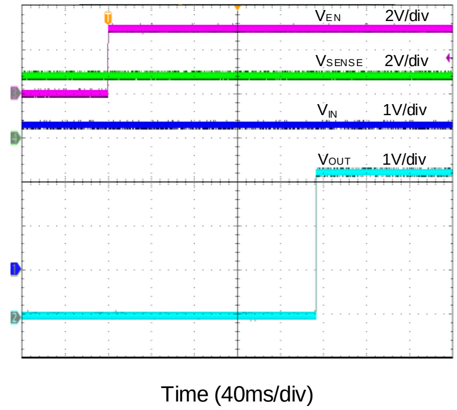
Shutdown from SENSE

(V_{CC}=3.3V, EN=3V, SENSE=3V to 0V, C_{IN}=1µF, CT=Null)



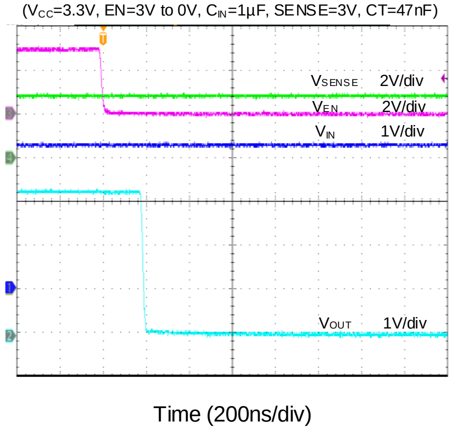
Startup from Enable

(V_{CC}=3.3V, EN=0V to 3V, C_{IN}=1µF, SENSE=3V, CT=47nF)



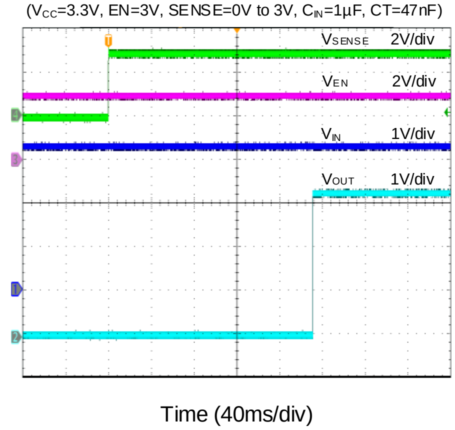
Shutdown from Enable

(V_{CC}=3.3V, EN=3V to 0V, C_{IN}=1µF, SENSE=3V, CT=47nF)



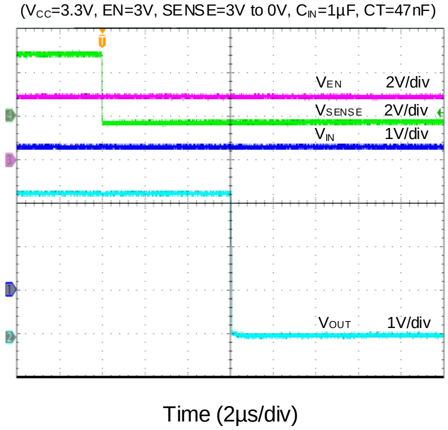
Startup from SENSE

(V_{CC}=3.3V, EN=3V, SENSE=0V to 3V, C_{IN}=1µF, CT=47nF)



Shutdown from SENSE

(V_{CC}=3.3V, EN=3V, SENSE=3V to 0V, C_{IN}=1µF, CT=47nF)



Overview

The SY28637E device a very small supervisory circuit that monitor voltage greater than 500mV with a 1% threshold accuracy and offer adjustable delay time using external capacitor. The SY28637E has a logic enable pin to power on and off the output.

The SY28637E operates from 1.7V to 6.5V and has a typical quiescent current of 9μA with an open drain output rated at 18V. The SY28637E is available in an ultra-small DFN package and is fully specified over the temperature range of TJ=-40°C to 125°C.

Table 1. SY28637EDTD Truth Table

CONDITIONS		OUTPUT	STATUS
ENABLE = high	SENSE < VIT+	OUT = low	Output not asserted
ENABLE = low	SENSE < VIT+	OUT = low	Output not asserted
ENABLE = low	SENSE > VIT+	OUT = low	Output not asserted
ENABLE = high	SENSE > VIT+	OUT = high	Output asserted after delay

Applications Information

Input Pin (SENSE)

The SENSE input pin allows any system voltage above 0.5 V to be monitored. If the voltage at the SENSE pin exceeds VIT+, and provided that the enable pin is asserted (ENABLE = high), then the output is asserted after the capacitor-adjustable delay time elapses. When the voltage at the SENSE pin drops below (VIT+ – Vhys),then the output is de-asserted. The comparator has a built-in hysteresis to ensure smooth output assertions and de-assertions. Although not required in most cases, for extremely noisy applications, it is good analog design practice to place a 1nF to 10nF bypass capacitor at the SENSE input in order to reduce sensitivity to transients and layout parasitic. The target threshold voltage can be calculated by using Equation 1:

$$V_{TARGET}=(1+R_1/R_2)\times 0.5(V) \quad (1)$$

Output Delay Time Pin (CT)

To program a user-defined, adjustable delay time, an external capacitor must be connected between the CT pin and GND. If the CT pin is left open, there will be a delay of 40 μs. The adjustable delay time can be calculated through Equation 2:

$$t_{pd(r)}\ (s) = [C_{CT}(\mu F)\times 4] + 40\ \mu s \quad (2)$$

The reset delay time is determined by the time it takes an on-chip, precision 310nA current source to charge the external capacitor to 1.24 V. When SENSE > V_{IT+} and with ENABLE high, the internal current sources are enabled and begin to charge the external capacitors. When the CT voltage on a capacitor reaches 1.24V, the corresponding OUT is asserted. Note that a low-leakage type capacitor (such as ceramic) should be used, and that stray capacitance around this pin may cause errors in the reset delay time.

Output pin (OUT)

In a typical SY28637E application, the OUT outputs is connected to a reset/enable input of the processor (DSP, CPU, FPGA, ASIC, and so on) or connected to the enable input of a voltage regulator. The SY28637E provide open-drain outputs. Pull up resistors must be used to hold these lines high when OUT is asserted. By connecting the pull up resistors to the proper voltage rails, OUT can be connected to other devices at the correct interface voltage levels. The outputs can be pulled up to 18 V independent of the supply voltage (VCC). To ensure proper voltage levels, some thought should be given to choosing the correct pull up resistor values. The ability to sink current is determined by the supply voltage; therefore, if VCC = 5V and the desired output pull up is 18 V, then to obtain a sink current of 1 mA or less (as mentioned in the Electrical Characteristics), the pull up resistor value should be greater than 18 kΩ. By using wired-OR logic, any combination of OUT can be merged into one logic signal.

Enable Function

The enable input allows an external logic signal from other processors, logic circuits, and/or discrete sensors to turn on or turn off the output. The SY28637E offers an active-high enable input (ENABLE). Driving ENABLE high forces OUT to go high. The 0.4V (maximum) low and 1.4V (minimum) high allow ENABLE to be driven with a 1.5V or greater system supply.

For SY28637E devices with VSENSE > VIT+, driving ENABLE high makes SENSE_OUT go high after the capacitor-adjustable delay time.

PCB Layout Guide

For best performance of the SY28637EDTD, the following guidelines must be strictly followed:

1. Keep all power traces as short and wide as possible and use at least 1 ounce copper for all power traces.
2. Place a ground plane under all circuitry to lower both resistance and inductance and improve DC and transient performance.
3. Place the VCC decoupling capacitor close to the device.

4. Avoid using long traces for the VCC supply node. The VCC capacitor (CVCC), along with parasitic inductance from the supply to the capacitor, can form an LC tank and create ringing with peak voltages above the maximum VCC voltage.

5. Input and output capacitors should be placed closed to the IC and connected to ground plane to reduce noise coupling.

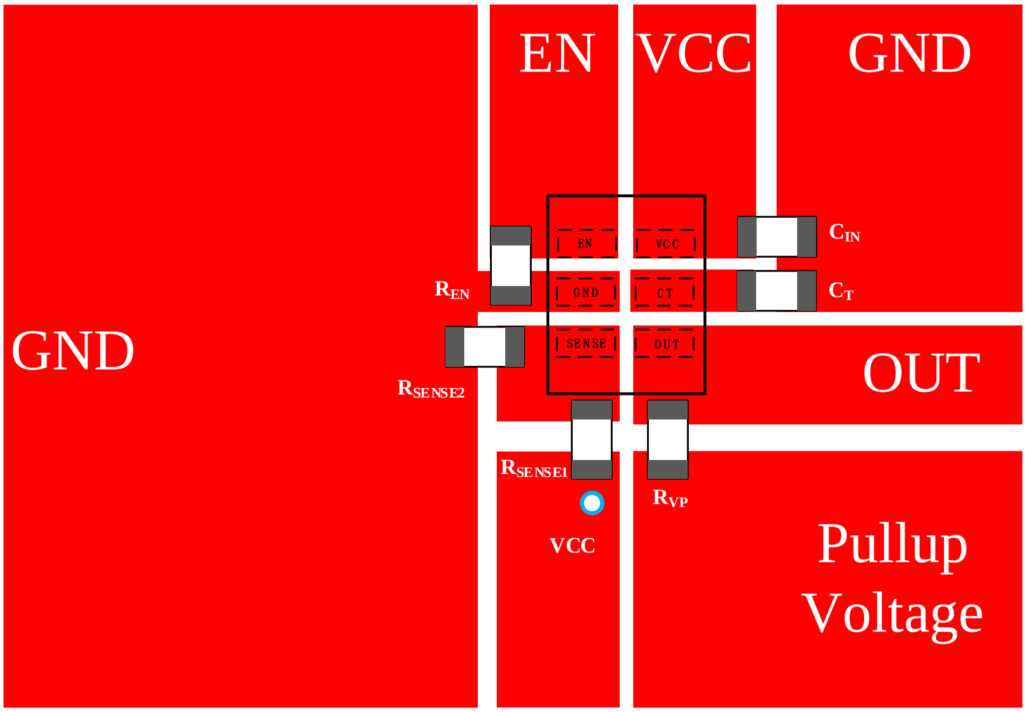
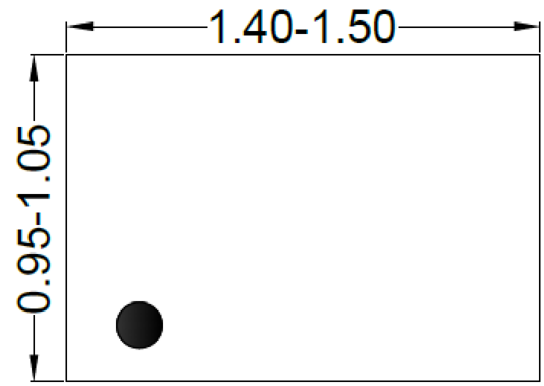
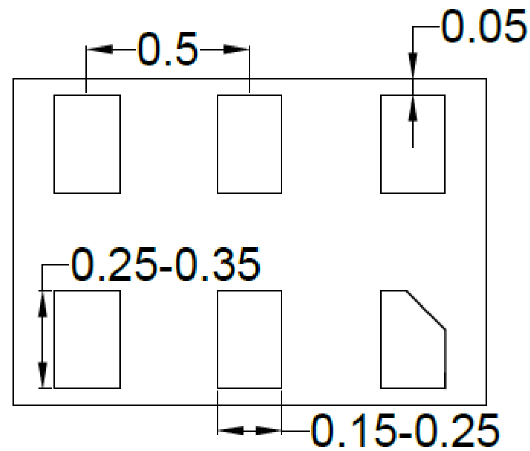


Figure4. PCB Layout Suggestion

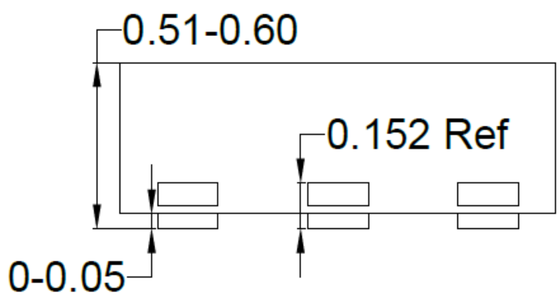
DFN1.45×1-6 Package Outline Drawing



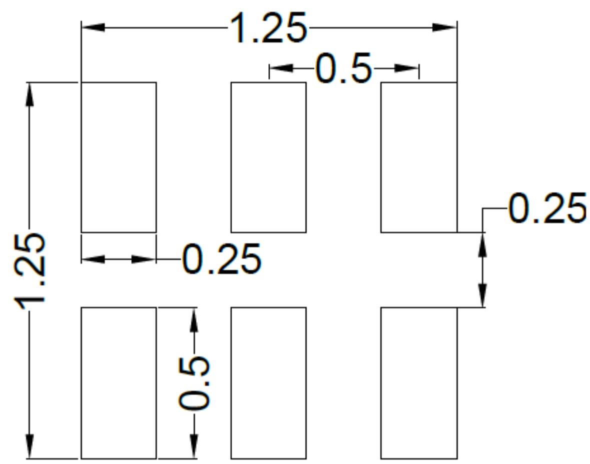
Top View



Bottom View



Side View

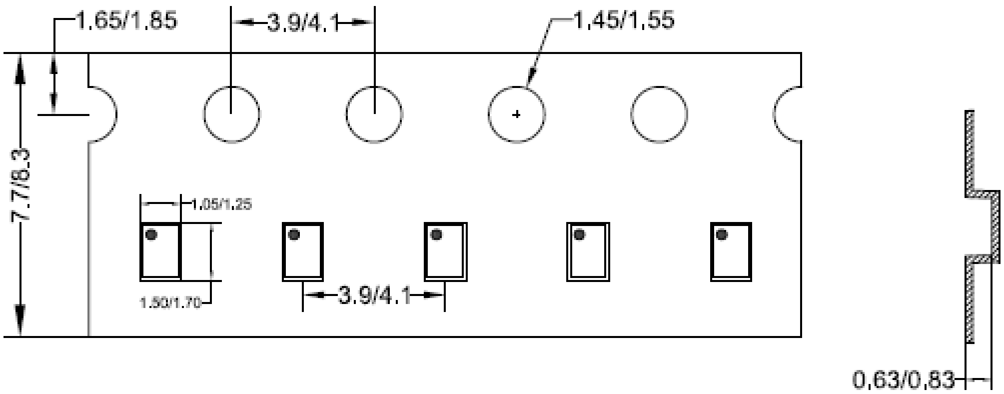


Recommended PCB Layout
(only for reference)

Notes: **All dimension in millimeter and exclude mold flash & metal burr.**

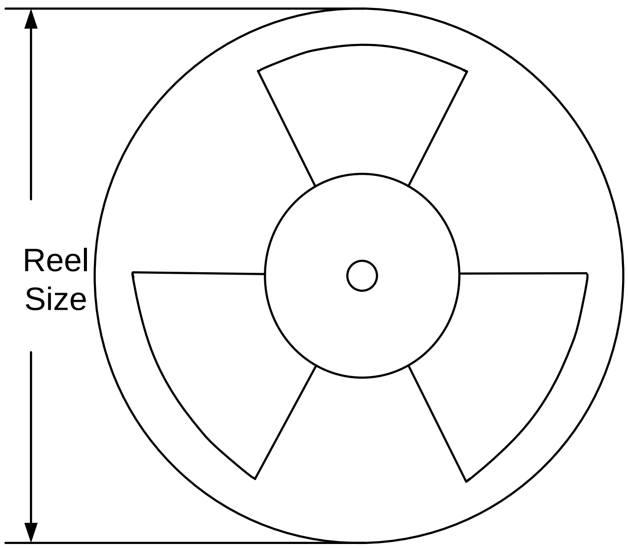
Taping & Reel Specification

1. Taping orientation



Feeding direction →

2. Carrier Tape & Reel specification for packages



Package types	Tape width (mm)	Pocket pitch(mm)	Reel size (Inch)	Trailer length(mm)	Leader length (mm)	Qty per reel
DFN1.45×1	8	4	7"	400	160	3000

3. Others: NA

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