SY23425

Secondary Side Synchronous Rectification Controller

General Description

The SY23425 is a synchronous rectification controller with high performance capabilities, ideal for use in flyback converters operating in CCM (Continuous Conduction), DCM (Discontinuous Conduction), and QR (Quasi-Resonant) modes.

It can drive both standard and logic-level N-channel MOSFETs for secondary-side synchronous rectification.

To prevent false turn-on by parasitic ringing under DCM or QR mode, the device uses the D_{SEN} voltage falling slope rate detection.

The SY23425 features a DSEN high-voltage blanking time detection function that enhances system ESD performance, preventing external noise from false turn-on of the SR (Synchronous Rectifier) MOSFET.

Under CCM operating mode, it has an extremely short turn-off delay time, while the DSEN voltage regulation fully utilizes the conduction time of the SR MOSFET for optimizing the efficiency under DCM and QR modes.

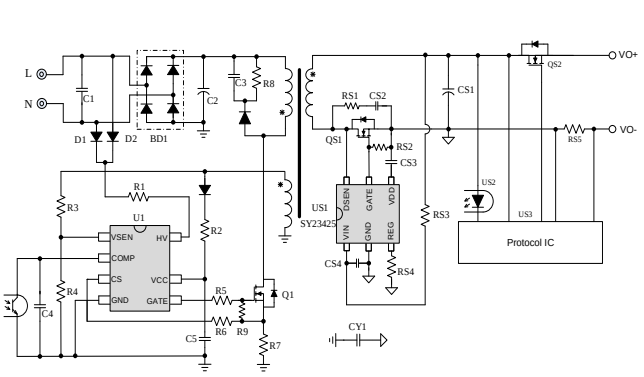
During light load conditions, the controller enters power saving mode to improve light load efficiency

Features

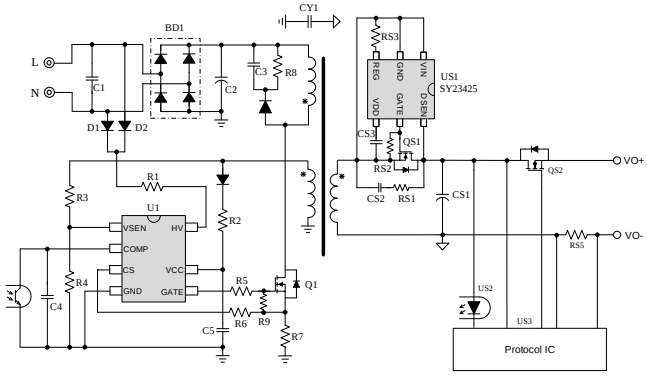
- Suitable for CCM, DCM and QR Mode Flyback Converters
- DSEN Pin Sensing up to 200V
- DSEN Falling Slope Rate Detection to Avoid False Turn on of SR MOSFET by Parasitic Ring
- Uses DSEN High Voltage Blanking Time to enhance system ESD performance
- GATE Pin Clamped before VDD On
- Dual Supply Channel for 3.3V to 21V Output Systems
- Supports the use of GaN MOSFETs
- Up to 500kHz switching frequency
- 10 ns Typical Turnoff Propagation Delay
- 2A Sink, 0.5A Source Gate Driver Capability
- Compact Package: SOT23-6

Applications

- AC/DC Adapters
- USB Type-C and Power Delivery AC Adapters
- Server and Telecom Power Supply
- Auxiliary Power Supplies



SR MOSFET location: Low Side



SR MOSFET location: High Side

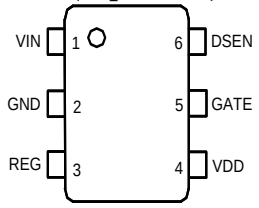
Fig. 1. Typical Application Circuit

Ordering Information

Ordering Part Number	Package type	Top mark
SY23425ABC	SOT23-6 RoHS Compliant and Halogen	D2xyz

x=year code, y=week code, z= lot number code

Pinout (top view)



Pin No	Pin Name	Pin Description
1	VIN	Power supply pin, connect it to the output of converter when a low-side SR MOSFET is used. Connect it to GND pin when a high-side SR MOSFET is used.
2	GND	Connect this pin to SR MOSFET Source terminal.
3	REG	Connect a resistor between this pin and GND to set the falling slope timer reference (Tref).
4	VDD	Output of internal LDO, power supply for control unit and gate drive circuit. Connect a 0.1μF or larger ceramic capacitor between the VDD and GND pins.
5	GATE	Connect this pin to the gate terminal of the SR MOSFET
6	DSEN	This pin should be connected to the DRAIN of SR MOSFET for voltage sensing. This pin is also used as a power supply option.

Block Diagram

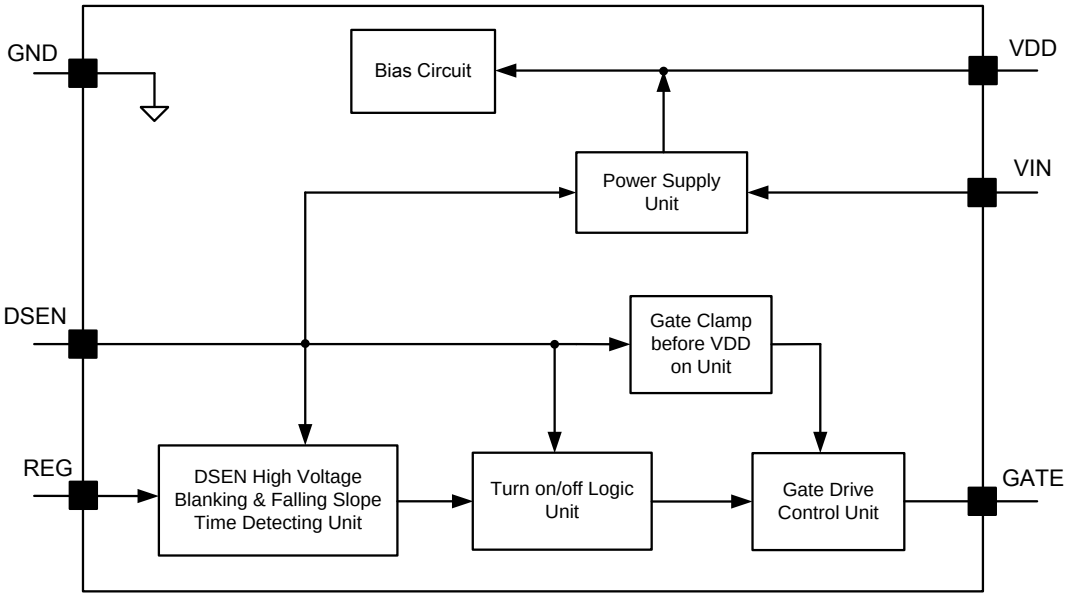


Fig.2 Block diagram

Absolute Maximum Ratings (1) (Note 1)	Min	Max	Unit
VIN	-0.3	28	V
REG, VDD, GATE	-0.3	16	
DSEN	-1.5	200	
I_{VDD}		20	mA
Junction Temperature, Operating	-40	150	°C
Lead Temperature (Soldering, 10 sec.)		260	
Storage Temperature	-65	150	

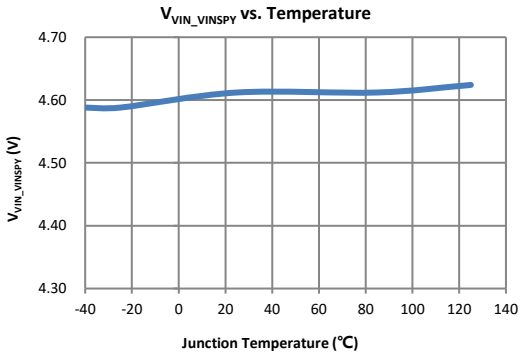
Thermal Information (2) (Note 2)	Min	Max	Unit
θ_{JA} Junction-to-ambient Thermal Resistance		170	°C/W
θ_{JC} Junction-to-case Thermal Resistance		130	
PD Power Dissipation TA = 25°C		0.6	W

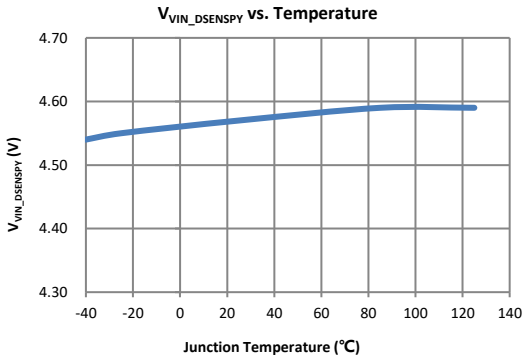
Recommended Operating Conditions (3)	Min	Max	Unit
VIN	3.3	21	V
DSEN	-1	150	
Junction Temperature	-40	125	°C
Ambient Temperature	-40	105	

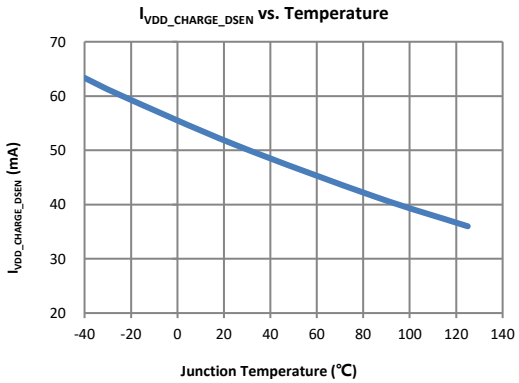
Electrical Characteristics V_{VIN}=12V, T_A=25°C unless otherwise specified (4)							
Parameter		Symbol	Test conditions	Min	Typ	Max	Unit
VIN	Threshold of Switching to VIN Supply Channel	V_{VIN_VINSPY}	V_{VIN} is rising	4.35	4.6	4.85	V
	Threshold of Switching to DSEN Supply Channel	$V_{VIN\_DSENSPY}$	V_{VIN} is falling	4.3	4.55	4.8	V
VDD	On Threshold	V_{VDD_ON}		5	5.26	5.52	V
	VDD on Hysteresis	V_{VDD_HYS}		1.9	2.15	2.4	V
	VDD Regulation Voltage when VIN Pin is Active to Supply IC	$V_{VDD\_REG\_VIN}$		8.55	9	9.4	V
	VDD Regulation Voltage when DSEN Pin is Active to Supply IC	$V_{VDD\_REG\_DSEN}$		4.75	5.1	5.35	V
	Operating Current	I_{VDD_OP}	V_{VDD}=9V,C_{GATE}=2.2nF, F_{SW}=100kHz		3	3.5	mA
	Maximum VDD Pin Capacitor Charging Current	$I_{VDD\_CHARGE\_MAX}$	VIN pin is active to charge VDD capacitor	12	17		mA
			DSEN pin is active to charge VDD capacitor	40	50		mA
	Quiescent Current	I_{VDD_STBY}	Under Standby Mode		220	280	μA
DSEN	Ratio of PVS to DSEN	$K_{\_PVS\_RATIO}$			50		
	PVS Initial Enable Threshold	$V_{PVS\_INITIAL\_EN}$		120	150	180	mV
	Blanking Time for Sample PVS Pin Voltage	T_{PVS_BLK}		210	310	410	ns
	Low Level Threshold to Sense VDSEN Falling Time	V_{DSEN_LTH}	V_{DSEN} is falling	0	20	40	mV
	DESN Threshold to Force Turn off	V_{FORCE_TH}		5	15	25	mV
	Closed Loop V_{DSEN} Regulation Voltage Level	V_{DS_REG}	SR MOSFET is conducting	-54	-33	-22	mV
	SR MOSFET Turn off Threshold	V_{OFF_TH}	V_{DSEN} is rising	-10	0	10	mV
	Time Threshold IC Go into Sleep	$T_{STANDBY}$		16	20	24	us
REG	Resistor to Program Frequency Option	R_{REG}	R_{REG}=50k(Note3)	75	100	125	ns
			R_{REG}=300k(Note3)	225	300	375	ns
GATE	GATE Pin Clamped Current before VDD ON	I_{CLP}	Vgs=1V	160	200		mA
	Max. Source Current	I_{SOURCE_MAX}	V_{VDD}=9V, C_{LOAD}=2.2nF, Vgs from 1V to 8V	0.375	0.5		A
	Max. Sink Current	I_{SINK_MAX}	V_{VDD}=9V, C_{LOAD}=2.2nF, Vgs from 8V to 1V	1.5	2		A
	Minimum ON Time	T_{ON_MIN}		450	700	950	ns
	Minimum OFF Time	T_{OFF_MIN}		250	400	550	ns
	Turn on propagation Delay	T_{DELAY_ON}	C_{GATE}=2.2nF		30	50	ns
	Turn off propagation Delay	T_{DELAY_OFF}	C_{GATE}=2.2nF		10	20	ns
OTP	Thermal Shutdown Temperature	T_{SD}(Note3)		150	160	170	°C
	Hysteresis to Resume Operating	T_{OTP_HYS}(Note3)		15	20	25	°C

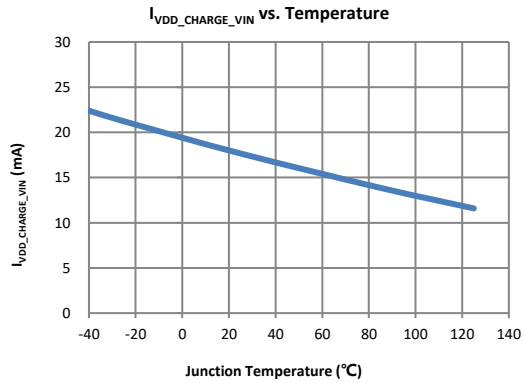
Note 1: Stresses beyond the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
Note 2: θ_{JA} is measured in the natural convection at T_A = 25°C on a low effective single layer thermal conductivity test board of JEDEC 51-3 thermal measurement standard. Test condition: Device mounted on "2x 2" FR-4 substrate PCB, 2oz copper, with minimum recommended pad on top layer and thermal via to bottom layer ground plane.
Note 3: Guaranteed by design.

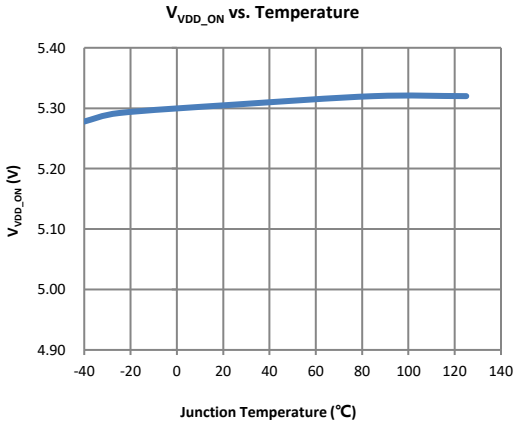
Typical Characteristics

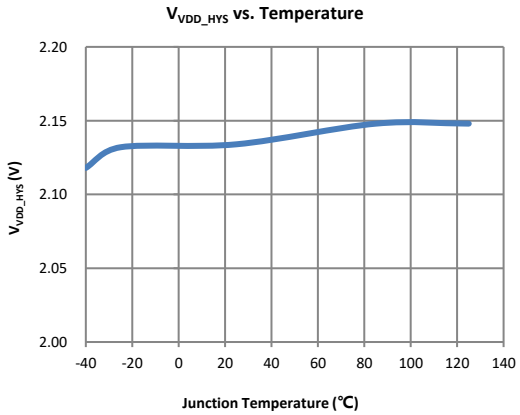




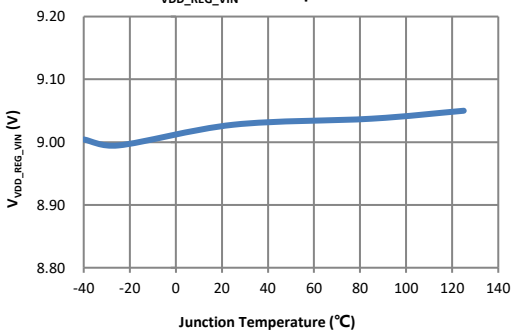




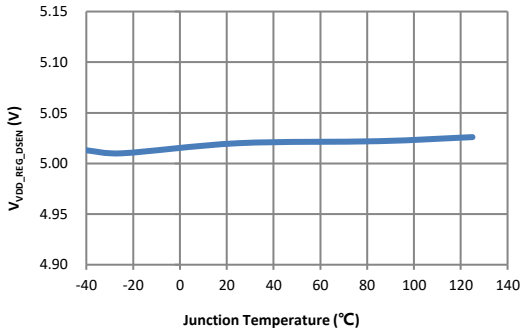




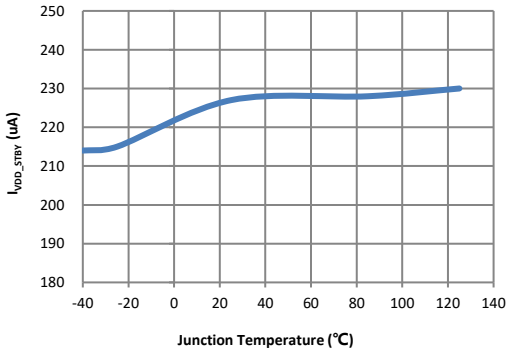
$V_{VDD\_REG\_VIN}$ vs. Temperature



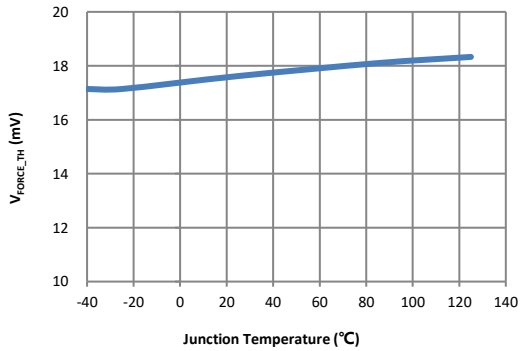
$V_{VDD\_REG\_DSEN}$ vs. Temperature



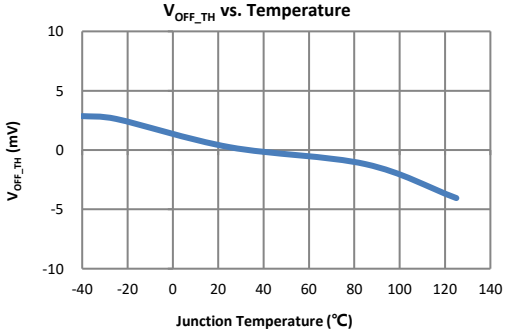
I_{VDD_STBY} vs. Temperature



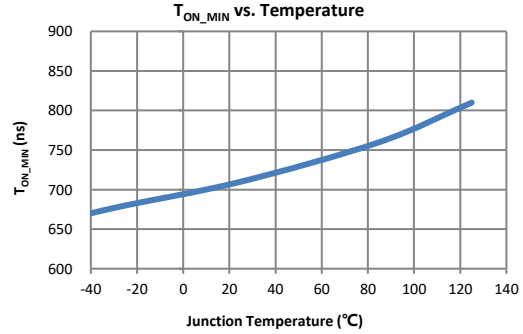
V_{FORCE_TH} vs. Temperature



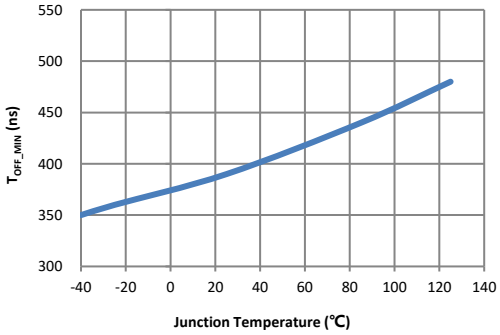
V_{OFF_TH} vs. Temperature



T_{ON_MIN} vs. Temperature



T_{OFF_MIN} vs. Temperature

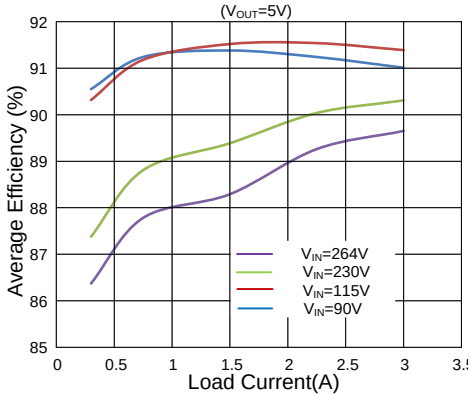


Typical Performance Characteristics

(T_A= 25℃, 65W PD Charger, Input voltage: 90Vac~264Vac, Output spec: 5V3A, 20V3.25A.)

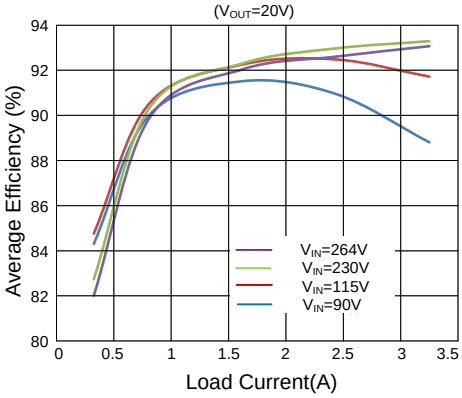
Efficiency vs. Load Current

(V_{OUT}=5V)



Efficiency vs. Load Current

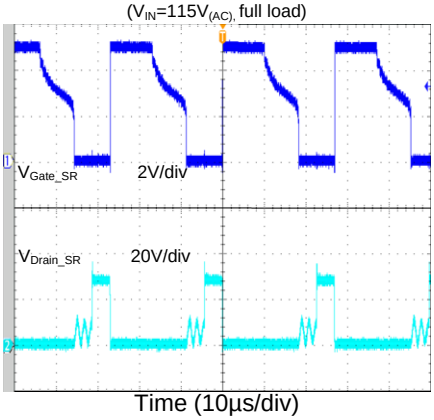
(V_{OUT}=20V)



5V Output Characteristics

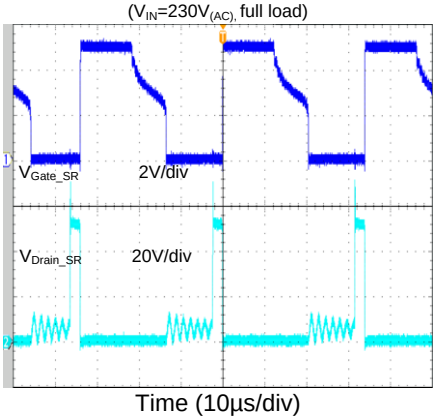
Steady States

(V_{IN}=115$V_{(AC)}$, full load)



Steady States

(V_{IN}=230$V_{(AC)}$, full load)



Steady States

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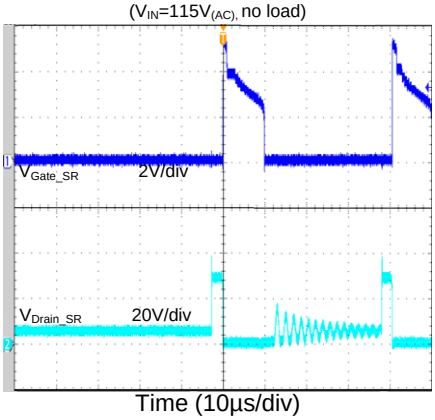
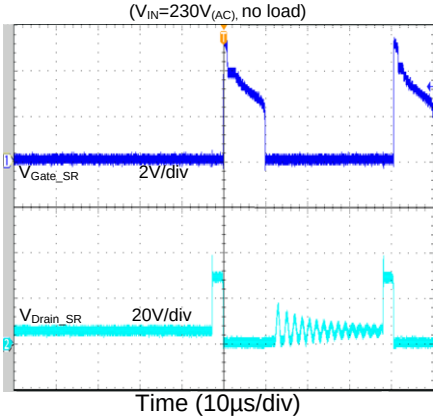


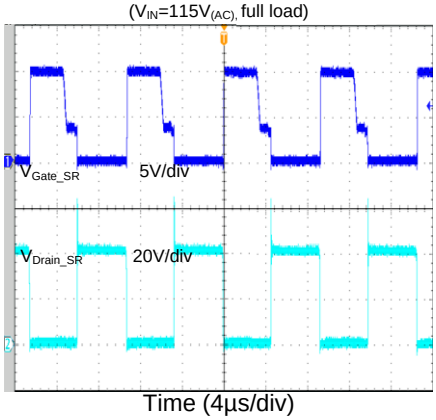
Steady States

(V_{IN}=230$V_{(AC)}$, no load)



20V Output Characteristics

Steady States
(V_{IN}=115$V_{(AC)}$, full load)



Steady States
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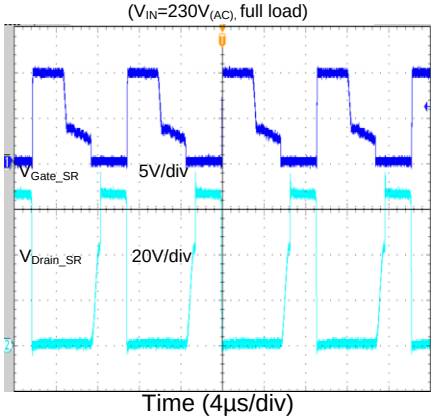

Steady States
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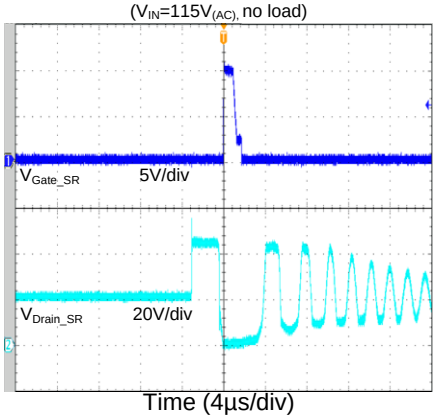
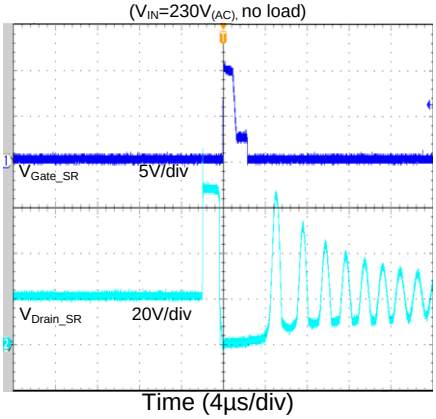


Steady States
(V_{IN}=230$V_{(AC)}$, no load)



Detailed Description

General Features

GATE Drive

For proper operation, while V_{VDD}<V_{VDD_ON} the SR MOSFET gate is pulled down. The circuit in the diagram below is used for this purpose:

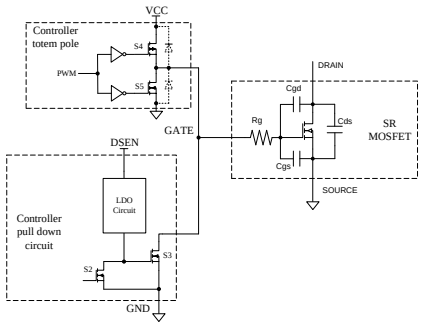


Fig. 3 Circuit used for SR MOSFET Control during start-up

When V_{VDD}<V_{VDD_ON}, switch S2 is Open and the DSEN voltage will charge the Cgs capacitance for the S3 switch. When S3 turns ON, it will pull down the gate of the SR MOSFET. The pull down current of S3 is 200mA (@Vgs=1V for the POWER MOSFET) to optimize the performance.

While V_{VDD}>V_{VDD_ON}, the S2 switch is closed, leading to S3 being turned OFF (switch open). The GATE pin will be controlled only by the driver circuit consisting of S4 and S5, as shown in Fig.3 & Fig.4.

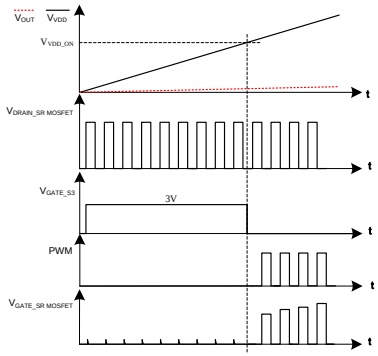


Fig. 4 GATE Pin Timing diagram

SR MOSFET GATE Control

The traditional method of turning ON the SR MOSFET is to use a set turn-on threshold VON_TH.

When the DSEN voltage falls and reaches VON_TH, the SR MOSFET is turned ON after a short delay.

While in DCM or QR operating modes, a resonant waveform may appear after the transformer secondary current decreases to zero. Sometimes, the amplitude of this resonant waveform can be large enough to cause the DSEN voltage to drop below the turn-on threshold VON_TH, which may lead to the false turn-on of the SR MOSFET. To address this issue, a circuit to detect the falling slope rate of V_{DSEN} is used.

When the primary MOSFET Q1 is turned off, the V_{DSEN} falling slope rate is very high, and the SR MOSFET will turn on. During the resonant phase, the V_{DSEN} falling slope rate is relatively low, and the SR MOSFET will not turn on. The SY23425 uses a resistor divider circuit to sense the DSEN voltage, where V_{PVS} is 0.02 x V_{DSEN}.

Two thresholds are set to sense the V_{PVS} falling slope rate. △T is the time duration measured when V_{PVS} is falling between the high-level threshold V_{PVS_HTH} and the low-level threshold V_{DSEN_LTH} (0mV). △T is compared with a falling slope reference time TREF using a counter.

A blanking period is used to prevent external noise (such as ESD noise) from falsely turning on the SR MOSFET.

If V_{PVS} is above V_{PVS_HTH}, lasts for T_{PVS_BLK} (300ns) and the falling slope time △T <T_{REF}, the IC considers this action as a primary MOSFET turn-off event, and will turn ON the SR MOSFET after a short delay. In all other cases the SR MOSFET will not be turned ON.

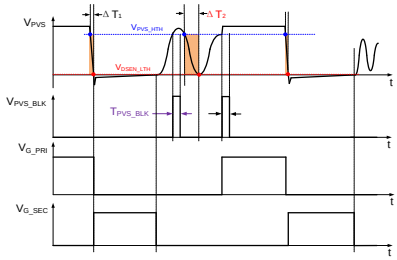


Fig.5 SR MSOFET Turn ON Time diagram

V_{PVS_HTH} is a dynamically adjusted value, and it has a value of 0.85 x V_{DSEN}.

The falling slope ref time threshold T_{REF} is controlled by REG resistor as shown below:

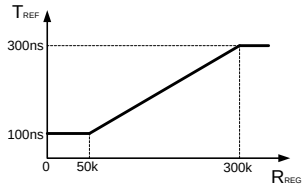


Fig. 6 Tref Programming

In DCM mode, the current through the SR MOSFET will decrease before the primary MOSFET is turned on. The closed-loop V_{DS} regulation circuit will gradually reduce V_{GATE} once V_{DS} is above the V_{DS_REG} (-33mV) level. As the current through the SR MOSFET decreases, V_{GATE} drops close to the turn-off threshold of the SR MOSFET. At this point, the product of the (I_D x R_{DSON}) can no longer be regulated to V_{DS_REG}, causing V_{DS} to increase beyond V_{OFF_TH}. After a short time delay (T_{OFF_DLY}), a large sink current will pull down the gate voltage to zero to turn OFF the SR MOSFET.

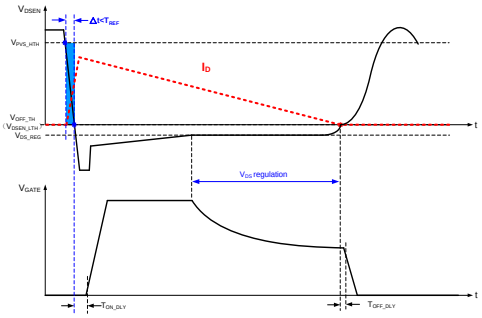


Fig. 7 SR MOSFET control in DCM mode

During the CCM mode, the primary MOSFET will be turned ON before secondary current decreases to ZERO, and V_{DSEN} will rapidly increase. The device will compare V_{DSEN} with another threshold V_{OFF_TH}, and once V_{DSEN} is rising and crossing V_{OFF_TH}, after a short delay time T_{OFF_DLY}, the gate voltage will be pulled down by a large sink current to achieve fast turn off. The turn off delay time T_{OFF_DLY} is designed to be very short to minimize the power loss caused by primary and secondary MOSFET overlap.

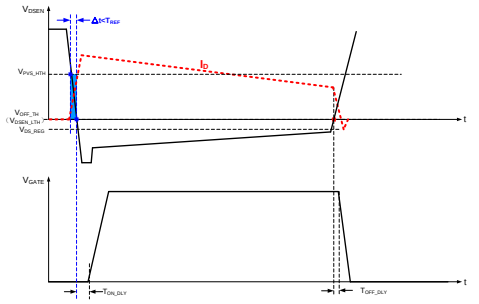


Fig. 8 SR MOSFET in CCM Mode

Min ON Time & Min OFF Time

When primary MOSFET is turned off, the DRAIN voltage of the secondary SR MOSFET will drop rapidly to about -700mV, due to the circuit parasitics resonance.To void false turn off of the SR MOSFET, a blanking time T_{ON_MIN} is applied after the SR MOSFET is turned ON. During this blanking time, the GATE pin output is latched off.

After SR MOSFET is turned OFF, a ringing will appear on DRAIN voltage waveform. To avoid the internal logic circuit false trigger, a blanking time T_{OFF_MIN} used.

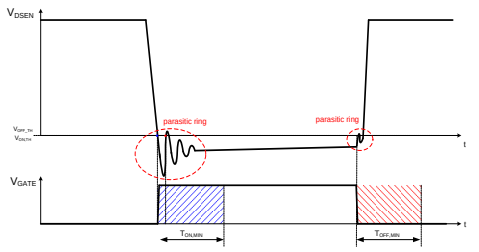


Fig. 9 timing diagram of Min ON/OFF time

Power Supply

The device optimizes the overall efficiency by using two possible power sources during normal operation.

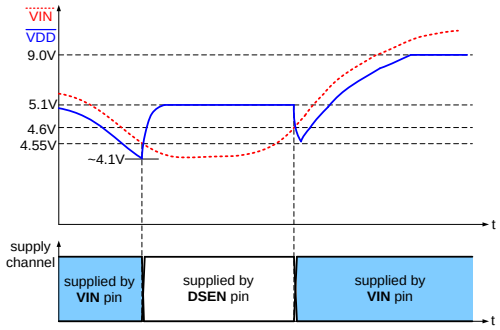


Fig. 10 Timing diagram of dual channel supply

Before VDD voltage reaches the V_{VDD_ON} threshold, the voltage is supplied by DSEN pin. When the voltage exceeds the V_{IN_INSPY} threshold, the VIN pin will be used instead.

As VIN increases, VDD will follow VIN (with about 0.5V voltage drop). When the voltage goes above 9V, the rail is regulated internally to this value.

When VIN is decreasing and crossing V_{DSEN_VINSPY}, the device will switch to using the DSEN pin, and VDD will be regulated to 5.1V. The timing diagram is shown in Fig. 10.

Power Saving Mode

Under light load conditions, the SY23425 will enter power saving mode to improve light load efficiency.

During the switching cycle, a timer will start to count after SR MOSFET is turned off. If the timer counts to 20us before next SR turn ON, the device will enter the power saving mode to

reduce the power consumption. The SY23425 will exit power saving mode on the next SR MOSFET turn ON event.

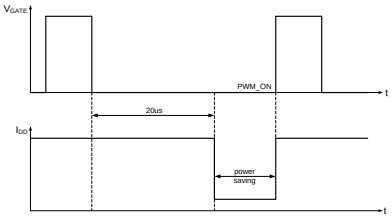


Fig. 11 timing diagram of power saving mode

Over Temperature Protection

IC die temperature is monitored, if the die temperature rises above 160℃, IC will stop driving SR MOSFET and the keep gate voltage to 0V. When die temperature drops below 140℃, IC will resume normal operating again.

Typical Application Schematic

Typical application circuit information is displayed in a 65W PD Flyback design. The PD charger circuit includes a primary side controller (SY5033A), synchronous rectification controller (SY23425), and a protocol controller (SY5258).

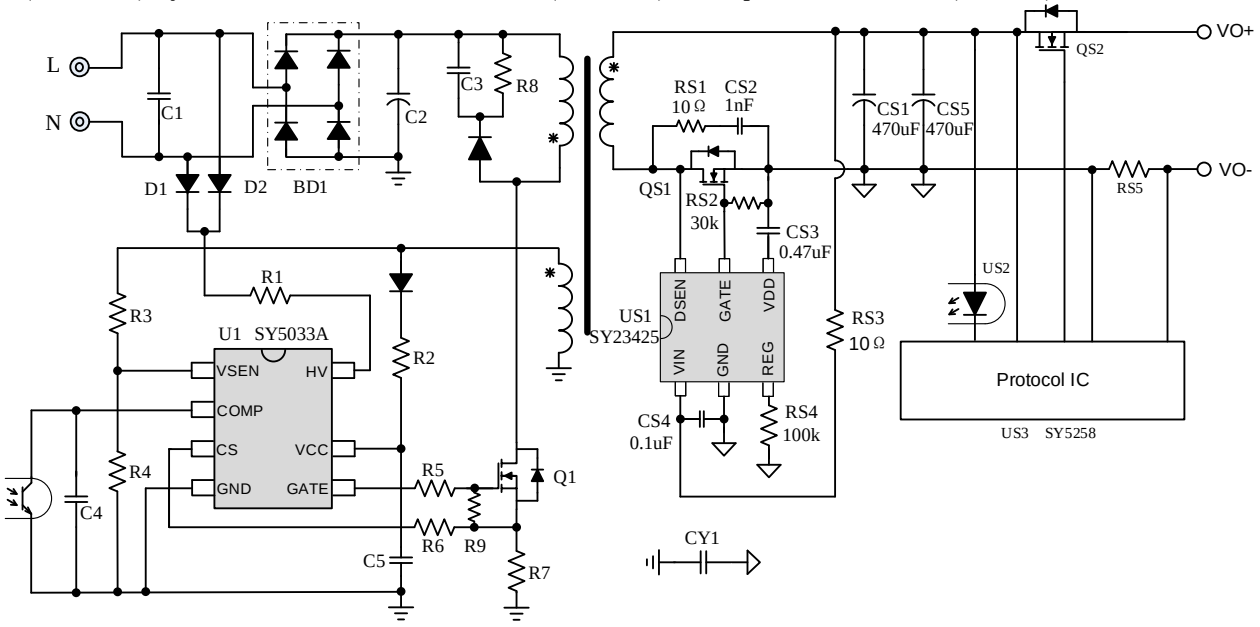


Fig. 12 65W PD Typical Application Circuit

Recommended BOM List

Designator	Description	Part Number	Manufacturer
RS1, RS3	10Ω/0805	0805W8F100JT5E	UNI-ROYAL
RS2	30k/0805	0805W8F3002T5E	UNI-ROYAL
RS4	100k/0805	0805W8F1003T5E	UNI-ROYAL
CS1, CS5	470uF/25V/Solid Cap	250ARHA471M08A2	APAQ
CS2	1nF/100V/X7R, 0805	CC0805KRX7R0BB102	YAGEO
CS3	0.47uF/16V/X7R, 0805	CC0805KRX7R0BB474	YAGEO
CS4	0.1uF/25V/X7R, 0805	CC0805KRX7R0BB104	YAGEO

Design Procedure

SR MOSFET Selection

The MOSFET selection is based on optimizing the RDSON verus Gate Charge losses.

Below a certain level, the RDSON of the MOSFET doesn't directly reduce the conduction loss, because SY23425 uses a loop that regulates the voltage drop in the forward direction to around 33 mV across the drain-source terminals.

For optimal performance consider a mimimum of 30% SR MSOFET conduction period at maximum load for optimal performance.

For example, for a 65W converter, the peak current of the SR MOSFET should be about 14A for 3.25A load current. To achieve a control time corresponding to 30% duty cycle, the R_{DSON} should be selected using the formula:

$$R_{DSON} \geq \frac{V_{DS\_REG}}{I_{PEAK\_SR} \times 0.3} = \frac{33mV}{4.2A} \approx 7.86m$$

For the MOSFET voltage rating, the maximum Vds should be lower than breakdown derated voltage. For example, for the 65W converter example, the transformer turn ratio is 7 and the derating coefficient $K_{Derating}$ is 0.9.

The breakdown voltage of the MOSFET should be higher than the value calculated using the formula below:

$$V_{DS(BR)} \geq \frac{V_{DS\_MAX}}{K_{Derating}} = \frac{\frac{V_{IN}}{N_{PS}} + \Delta V_{Spike}}{K_{Derating}} = \frac{\frac{373}{7}V + 10V}{0.9} = 70V$$

A 100V/8mΩ MOSFET is recommended for the above requirements.

Other considerations for selecting the right MOSFET are: overall efficiency, thermal performance, cost.

Snubber Selection

The Snubber components RS1 and CS1 are used to damp the switching ringing caused by stray inductance L_{Stray} and equivalent capacitance C_{EQ} in the secondary switching loop.

The L_{Stray} can be tested using a LCR meter. The C_{EQ} can be calculated considering the switching ringing period, based on the formula:

$$C_{EQ} = \frac{T_r^2}{(2\pi)^2 \times L_{Stray}} = \frac{50ns^2}{(6.28)^2 * 100nH} = 634pF$$

Considering the Q of the circuit equal to 1, the snubber resistor RS1 can be calculated using the formula:

$$R_{RS1} = \frac{1}{Q}\sqrt{\frac{L_{stray}}{C_{EQ}}} = \sqrt{\frac{100nH}{634pF}} = 12.56\Omega$$

A value of 10Ωcan be selected in this case.

C_{CS1} will influence the spike of VDS and thermal performance. The recommended value for CCS1 is 1nF.

External Components Selection

When used in low-side configuration, the SY23425 uses two power inputs. VIN pin is one of the supply channels, and a reservoir capacitor, CS4, has to be connected close to this pin.

The recommended value and voltage rating for CS4 are:

0.1 µF/25V.

The recommended value for RS3 is 10Ω.

The recommended value and voltage rating for CS3 in most applications are:

0.47uF/16V.

The REG pin is used to programm the falling slope reference. The recommended value for corresponding to a falling slope rate of 100 ns is 100k.

Layout Design

Follow the follwing PCB layout guidelines for optimal performance and thermal dissipation:

- Minimize the size of the switching loops: secondary power loop, secondary RC snubber circuit loop and IC power supply loop.
- GND pin should be connected to the Source of the SR MOSFET using a short trace.
- DSEN pin should be connected to the Drain of the SR MOSFET using a short connection.
- To achieve better EMI and Efficiency performance, use a decoupling capacitor between the output connector and the SR MOSFET output.
- To reduce ringing the parasitic inductance should be reduced by optimizing the layout, and/or increasing the RC snubber.

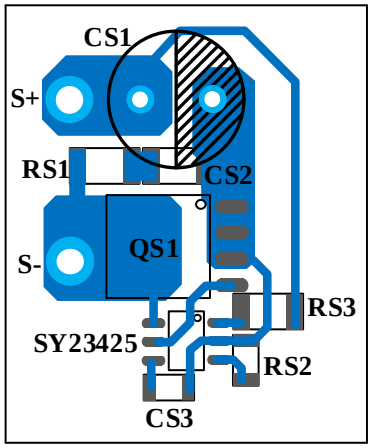
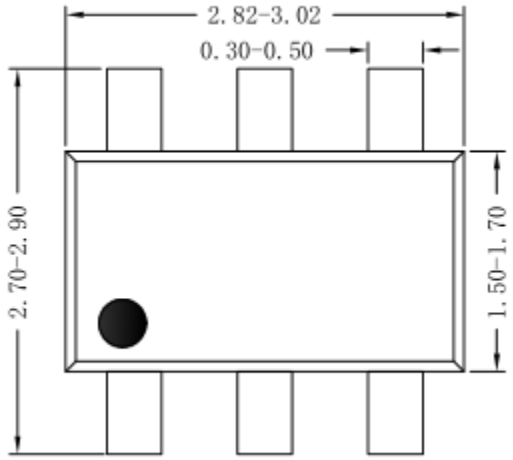
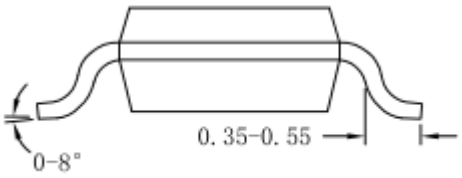


Fig.13 PCB Layout suggestion

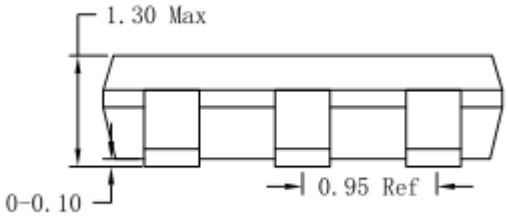
SOT23-6 Package Outline & PCB layout



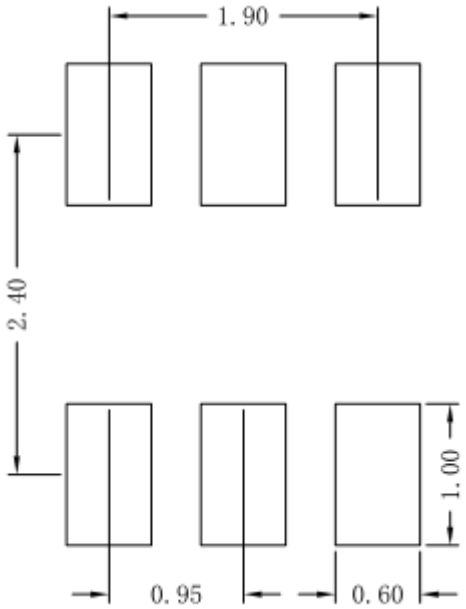
Top View



Side View



Side View

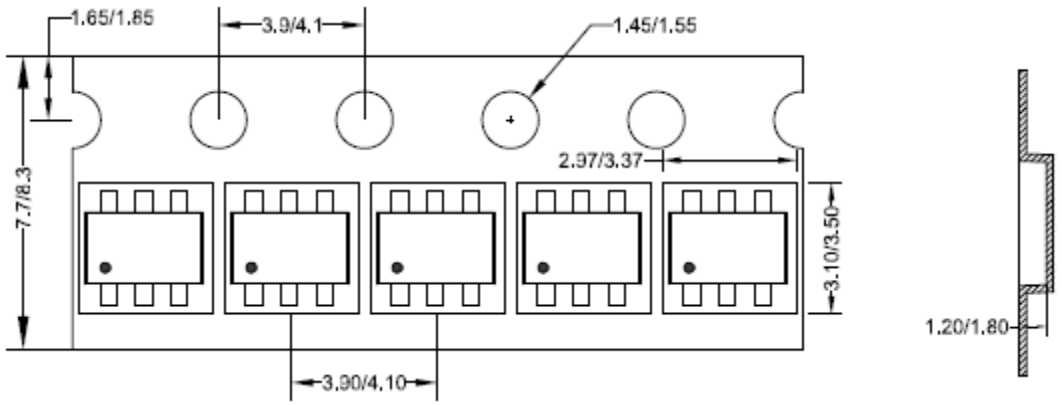


Recommended Pad Layout

Notes: **All dimension in millimeter and exclude mold flash & metal burr.**

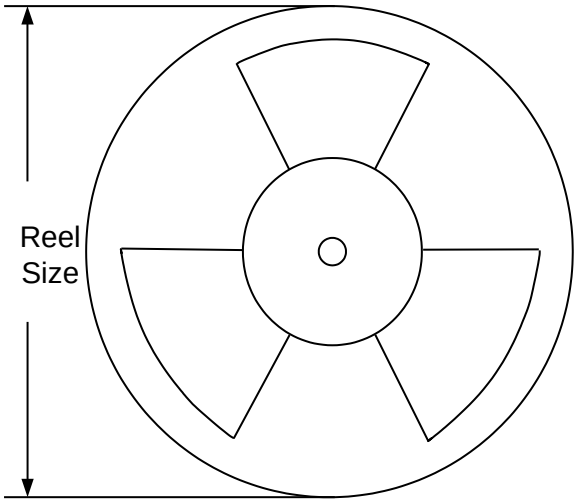
Taping & Reel Specification

1. Taping orientation for packages（SOT23-6）



Feeding direction ⟶

2. Carrier Tape & Reel specification for packages



Package type	Tape width (mm)	Pocket pitch(mm)	Reel size (Inch)	Trailer length(mm)	Leader length (mm)	Qty per reel
SOT23-6	8	4	7"	280	160	3000

Revision History

The revision history provided is for informational purpose only and is believed to be accurate, however, not warranted. Please make sure that you have the latest revision.

Date	Revision	Change
October 13, 2022	Revision 0.9	Initial Release

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