SY23432

ZVS Flyback SR Controller

General Description

SY23432 is a Flyback SR controller compatible with QR mode converter to achieve ZVS operation. The primary side PWM converter must work in quasi resonant mode. SY23432 adopts proprietary operation mode to achieve flyback ZVS turn on, which greatly improves Flyback efficiency and power density. SY23432 also adopts adaptive gate voltage control for safe operation.

SY23432 adopts DSEN voltage falling slope rate detecting technology to avoid SR MOSFET false turn on by parasitic ring under DCM or QR mode.

The SY23432 is available in a DFN2*3-8 package.

Features

- Proprietary Operation Mode for Flyback ZVS
- High Efficiency, High Power Density
- Adaptive Gate Voltage Control
- DSEN Falling Slope Rate Detecting to Prevent SR False Trigger
- 130V DSEN Pin to Directly Sense DRAIN Voltage of SR MOS
- Power Saving Mode to Improve Light Load Efficiency
- Dual Power Supply Channel for 3.3V to 21V Output Systems

Applications

- USB PD, Fast Charger
- Adaptor

Typical Applications

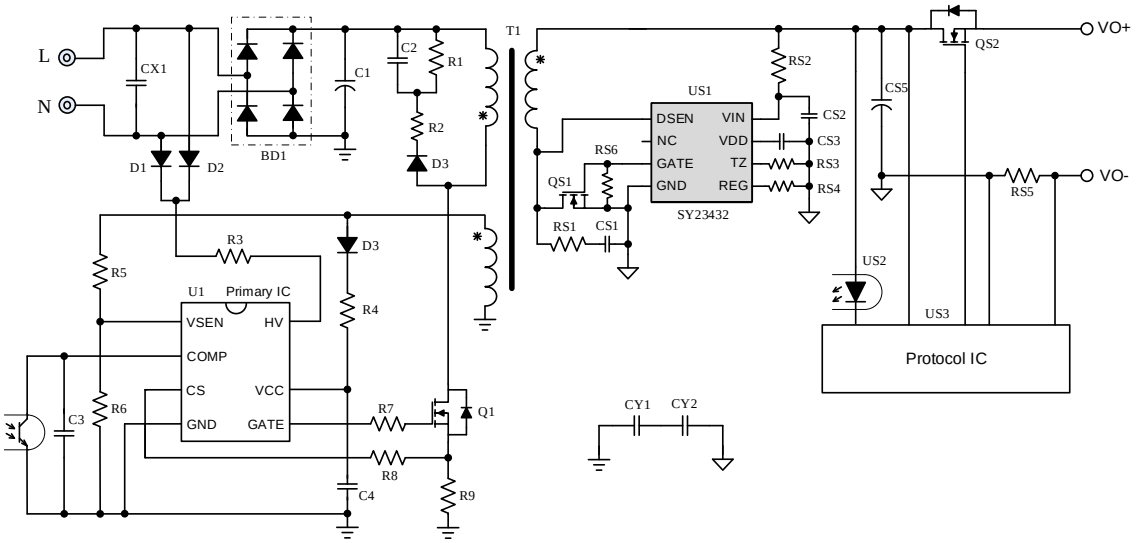


Fig. 1 Typical Application Circuit (SR MOSFET location: Low Side)

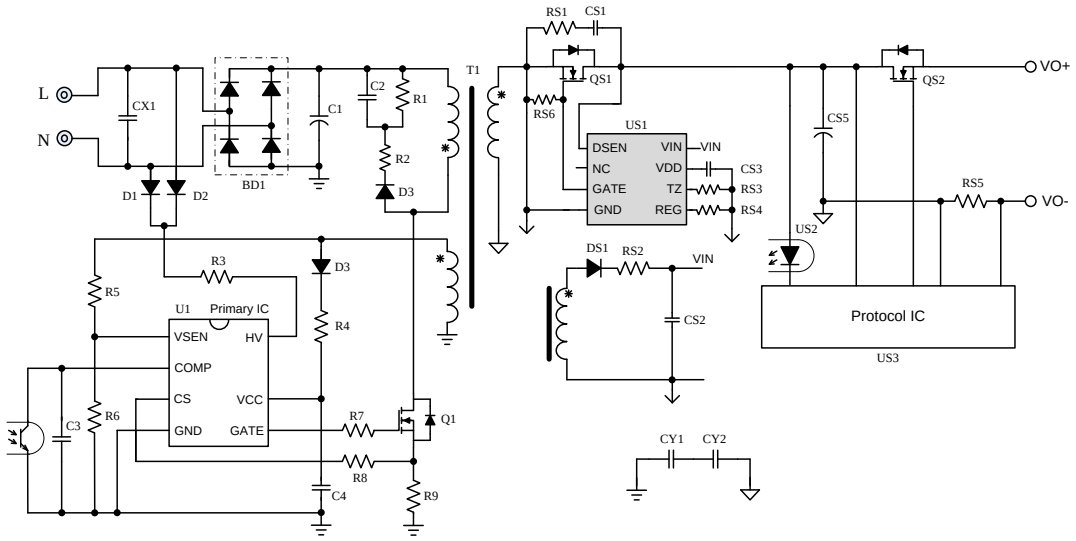


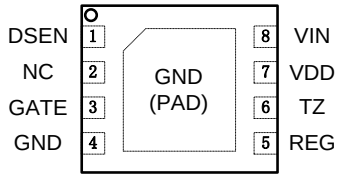
Fig. 2 Typical Application Circuit (SR MOSFET location: High Side)

Ordering Information

SY23432□(□□□)

Package Code

Optional Spec Code



(DFN2*3-8**)**

Pinout (top view)

Ordering Number	Package	Top Mark
SY23432DGD	DFN2*3-8	W7xyz

x=year code, y=week code, z= lot number code

Pinout (top view)

Pin number	Pin Name	Pin Description
1	DSEN	Drain sense input, and used as a self-supply channel
2	NC	Not connected
3	GATE	Gate drive pin
4	GND	Ground pin
5	REG	Connect a resistor between this pin and GND to set the falling slope ref time threshold
6	TZ	Connect a resistor to program ZVS coefficient.
7	VDD	Output of internal LDO, power supply for control unit and GATE drive circuit. Connect a 0.47μF or larger ceramic capacitor between VDD and GND pin
8	VIN	Low voltage power supply input
9	GND	Ground pin

Absolute Maximum Ratings (Note1)

DSEN ---------- -0.3V ~ 130V
VIN ---------- -0.3V ~ 30V
VDD ---------- -0.3V ~ 15V
GATE ---------- -0.3V ~ VDD+0.3V
TZ, REG ---------- -0.3V ~ 4V
Power Dissipation, @ T_A = 25°C DFN2x3 ---------- 1W
Package Thermal Resistance (Note 2)
DFN2x3, θ_{JA}---------- 46°C/W
DFN2x3, θ_{JC}---------- 28°C/W
Maximum Junction Temperature ---------- 150°C
Lead Temperature (Soldering, 10 sec.) ---------- 260°C
Storage Temperature Range ---------- -65°C to 150°C

Block Diagram

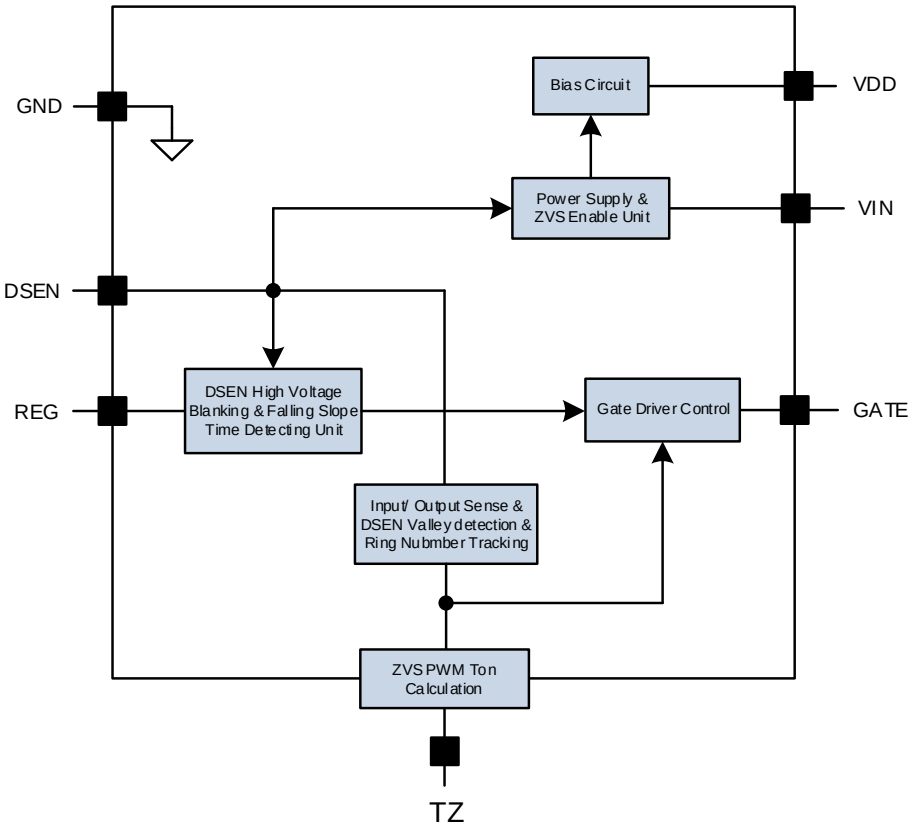


Fig.3 Block diagram

Electrical Characteristics

(V_{VIN} = 12V, T_A = 25°C unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
VDD Pin						
VDD ON Threshold	V_{VDD_ON}		3	3.3	3.6	V
UVLO Hysteresis	V_{VDD_HYS}		100	200	300	mV
VDD Regulation Voltage when VIN Pin is Active to Supply IC	$V_{VDD\_REG\_VIN}$		8.3	9.1	9.95	V
VDD Regulation Voltage when DSEN Pin is Active to Supply IC	$V_{VDD\_REG\_DSEN}$		4.2	4.6	5	V
Operating Current (Note3)	I_{VDD_OP}	V_{DD}=9V, C_{GATE}=2.2nF, F_{SW}=200kHz		5.35	6.4	mA
		V_{DD}=5V, C_{GATE}=2.2nF, F_{SW}=200kHz		3.5	4.2	mA
Maximum VDD Pin Capacitor Charging Current	$I_{VDD\_CHARGE\_MAX}$	VIN pin is active to charge VDD capacitor	25	35		mA
		DSEN pin is active to charge VDD capacitor	40	50		mA
Quiescent Current	I_Q	Under Sleep Mode	250	320	400	μA
VIN Pin						
Threshold of Switching to VIN Supply Channel	V_{VIN_VINSPY}	V_{VIN} is rising	4.5	4.8	5.1	V
Threshold of Switching to DSEN Supply Channel	$V_{VIN\_DSENSPY}$	V_{VIN} is falling	4.4	4.7	5	V
REG Pin						
Resistor to Program Drain Falling Slope to Enable SR(Note3)	R_{REG}	R_{REG}=50k	60	80	100	ns
		R_{REG}=300k	115	155	195	ns
TZ Pin						
ZVS Time Program Coefficient	k_{TZ}			4.5		10^{-9}
DSEN Pin						
Operating Voltage Range	V_{DS_OP}				110	V
Ratio of PVS to DSEN	$K_{\_PVS\_RATIO}$			50		
PVS Initial Enable Threshold	$V_{PVS\_INITIAL\_EN}$			150		mV
Turn on Threshold	V_{ON_TH}		-115	-85	-55	mV
V_{DS} Regulation Voltage	V_{DS_REG}		-52	-35	-20	mV
Turn off Threshold	V_{OFF_TH}		-4	10	26	mV
Force Turn off Threshold	$V_{DS\_FORCE\_TH}$		35	48	61	mV
Force Turn off Debounce Time(Note3)	T_{DBC_FORCE}		50	76	100	ns
Enter Sleep Mode Time Threshold	T_{SLP_TH}		50	67	80	μs
GATE Pin						
GATE Pin Clamped Current before VDD ON(Note3)	I_{CLP}	Vgs=1V	160	200		mA

Max. Source Current (Note3)	I_{SOURCE_MAX}	C_{LOAD}=2.2nF, Vgs from 1V to 6V	0.375	0.5		A
Max. Sink Current (Note3)	I_{SINK_MAX}	C_{LOAD}=2.2nF, Vgs from 6V to 1V	1.5	2		A
Minimum ON Time	T_{ON_MIN}		550	700	850	ns
Minimum OFF Time	T_{OFF_MIN}		400	530	660	ns
Turn on Delay Time (Note3)	T_{ON_DLY}	C_{GATE}=2.2nF		35	50	ns
Turn off Delay Time (Note3)	T_{OFF_DLY}	C_{GATE}=2.2nF		10	20	ns
OTP						
Thermal Shutdown Temperature (Note3)	T_{SD}			150		°C
Hysteresis to Resume Operating (Note3)	T_{OTP_HYS}			20		°C

Note 1: Stresses beyond the "Absolute Maximum Ratings" may cause perm anent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
Note 2: θ_{JA} is measured in the natural convection at T_A = 25°C on a low effective single layer thermal conductivity test board of JEDEC 51-3 thermal measurement standard. Test condition: Device mounted on 2" x 2" FR-4 substrate PCB, 2oz copper, with minimum recommended pad on top layer and thermal vias to bottom layer ground plane.
Note 3: Guarantee by design.

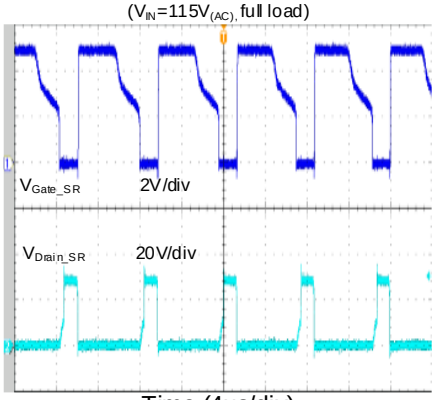
Typical Performance Characteristics

(Test condition: input voltage: 90Vac~264Vac; output spec: 5V3A, 20V3.25A; Ambient temperature: 25±5 ℃; Ambient humidity: 65±25 %.)

5V3A output

Steady States

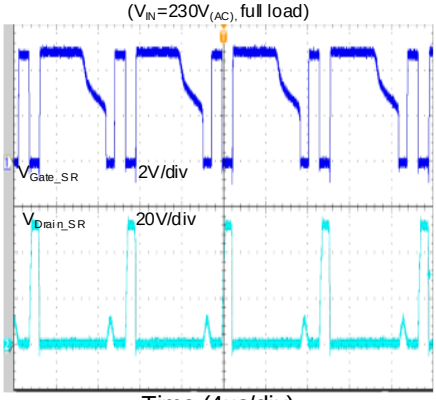
(V_{IN}=115$V_{(AC)}$, full load)



Time (4μs/div)

Steady States

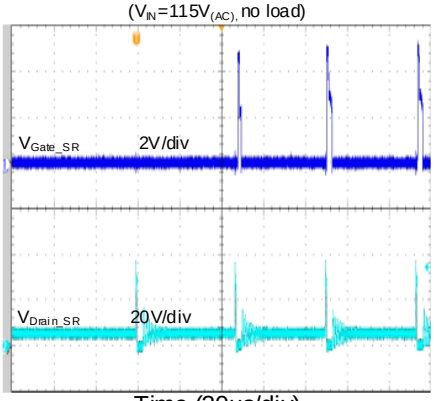
(V_{IN}=230$V_{(AC)}$, full load)



Time (4μs/div)

Steady States

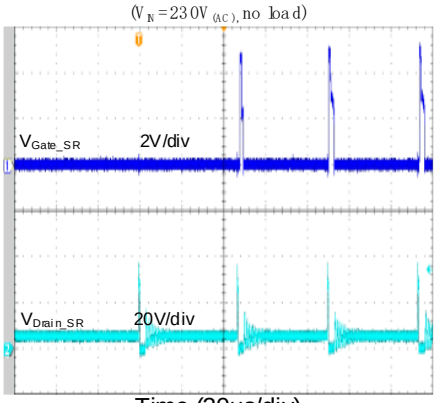
(V_{IN}=115$V_{(AC)}$, no load)



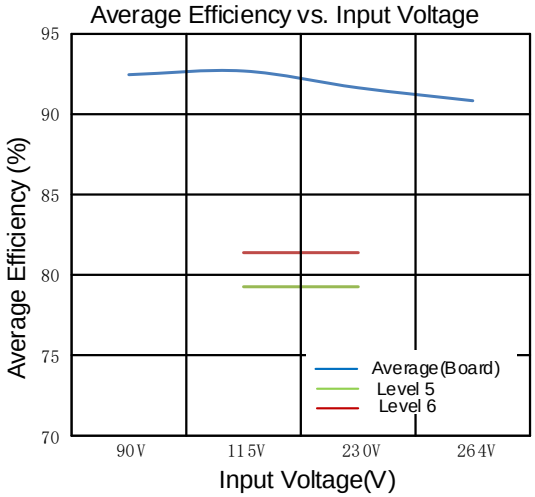
Time (20μs/div)

Steady States

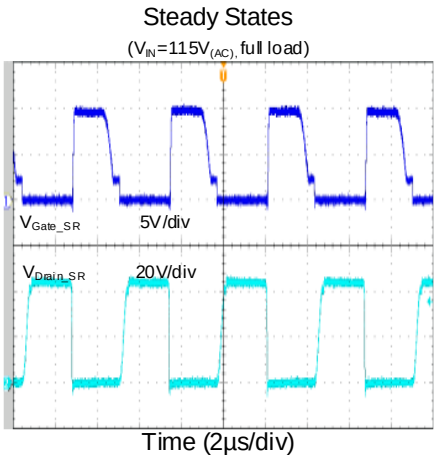
(V_{IN}=230$V_{(AC)}$, no load)

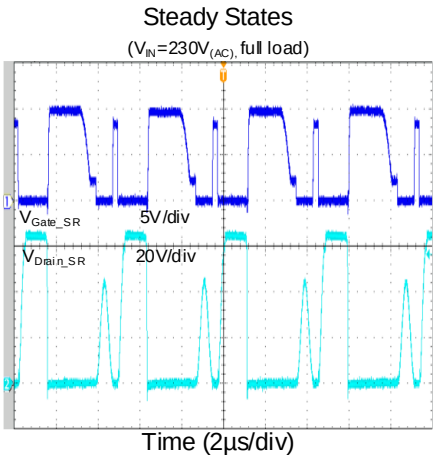


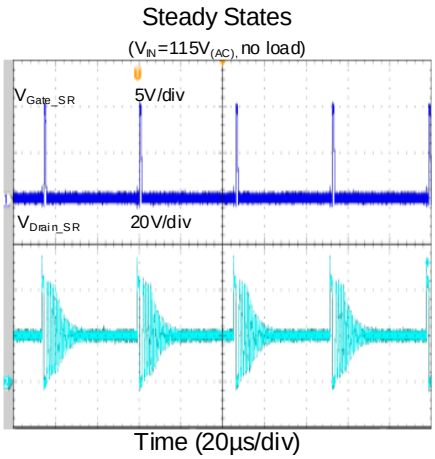
Time (20μs/div)

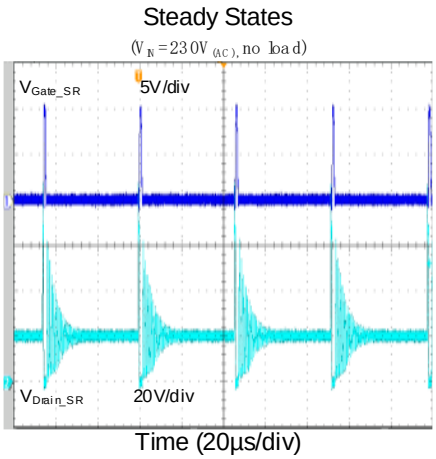


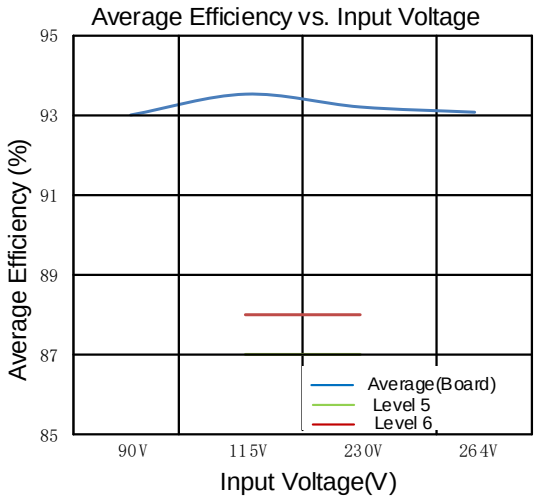
20V3.25A output











Operation Principles

Introduction

The SY23432 is a Flyback SR with proprietary operation mode to achieve flyback ZVS. It supports primary side PWM IC with QR mode, and the valley numbers should be 1 to 6. To ensure safety operation, SR control includes turn on/off control, Vds regulation, slope program, etc. The ZVS control logic helps primary side FET turning on at ~0V to reducing switching losses to maximize system efficiency and achieve high power density.

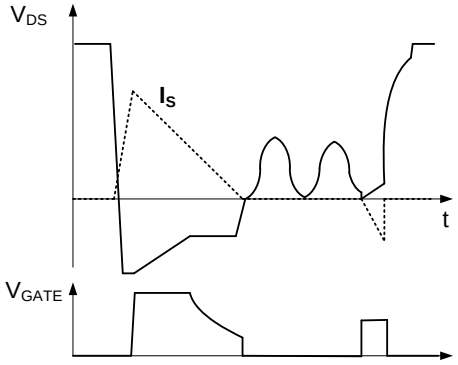


Fig. 1 SR operation diagram

SR Turn on

Traditional method is to set a SR MOSFET turn on threshold V_{ON_TH}, when DSEN voltage is falling and down to V_{ON_TH}, then turn on SR MOSFET after a short delay time. However, under DCM or QR operating mode, after secondary current decrease to zero, a resonant waveform will appear. Sometimes, the amplitude of this resonant waveform can be large enough, which will cause DSEN voltage drops below turn on threshold V_{ON_TH}, SR MOSFET may be falsely turned on by parasitic resonant.

To solve the above issue, V_{DS} falling slope rate is detected. When primary MOSFET is turned off, V_{DS} falling slope rate is very high, SR will turn on; while during resonant phase, V_{DS} falling slope rate is relatively low, SR will not turn on.

SY23432 use resistor divide circuit to sense the DSEN voltage, the V_{PVS} is 0.02 times of V_{DS}. It set 2 thresholds to indirectly sense V_{PVS} falling slope rate, the V_{PVS} is the time duration (△t) when V_{PVS} is falling between high-level threshold V_{PVS_HTH} and low-level threshold V_{PVS_LTH} (0mV) is measured, and the falling time duration (△t) will be compared with a falling slope ref time threshold T_{REF}.

To prevent external noise (for example: ESD noise) false turn on SR MOSFET by making fast V_{DS} falling slope rate, the DSEN blanking time is adopted.
V_{PVS} is the resistor divide voltage of V_{DS}. If V_{PVS} is above V_{PVS_HTH} and lasting for T_{PVS_BLK} (200nS) and falling slope time △t<T_{REF}, IC considers this action as primary MOSFET turn off event and then turn on SR MOSFET after a short delay. Otherwise, IC will not turn on SR MOSFET.

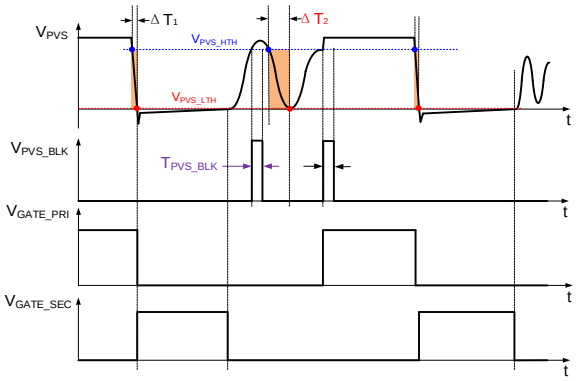


Fig. 2 Time diagram of SR enable strategy

V_{PVS_HTH} is a dynamically adjusted value, it is 0.85 times of DSEN high-level voltage value. The falling slope ref time threshold T_{REF} is controlled by REG resistor as below.

T_{REF} setting has 4 steps:		
Step	T_{REF}	R_{REG} (kΩ)
1	80ns	50
2	105ns	100
3	130ns	175
4	155ns	300

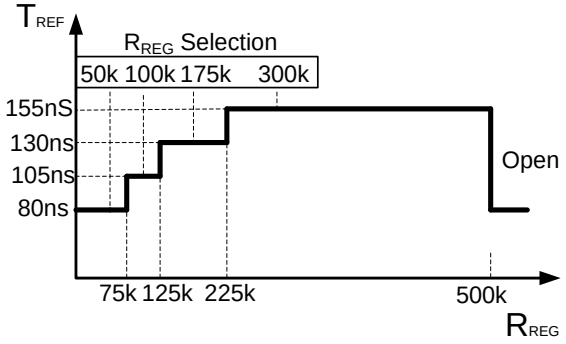


Fig. 3 Programmable curve of falling slope ref

SR Gate Control

After primary side FET turn off, the inductor current freewheels in SR, the current decreases linearly. When V_{DS} drops to V_{DS_REG}(-35mV), the closed loop V_{DS} regulation circuit will gradually decrease V_{GATE} to maintain the V_{DS} above V_{DS_REG}. As SR current becomes smaller, V_{GATE} drops near the SR MOSFET turn off threshold, I_D*R_{DSON} cannot be regulated to V_{DS_REG} anymore, V_{DS} will increase higher than V_{DS_REG}. If V_{DS} rises and cross V_{OFF_TH}, after a short delay time T_{OFF_DLY}, GATE voltage will be pulled down to 0V by a large sink current to turn off SR MOSFET.

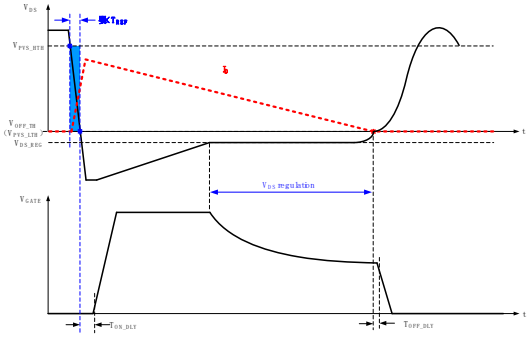


Fig. 4 SR gate control diagram

Min ON Time& Min OFF Time

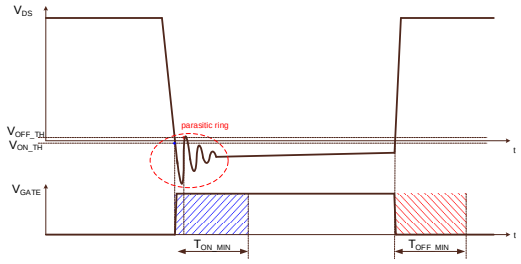


Fig. 5 timing diagram of min ON/OFF time

When primary MOSFET is turned off, DRAIN voltage of secondary SR MOSFET will drop rapidly to about -700mV, due to resonant between parasitic inductors and capacitors, a ringing will appear on DRAIN voltage waveform, the V_{DS} may reach the turn off threshold V_{OFF_TH}.

To avoid false turn off SR MOSFET, a blanking time T_{ON_MIN} is applied when SR MOSFET is turned on. During this blanking time, GATE pin output state is latched off unless it exceeds force turn off threshold lasting for debounce time.

Meanwhile, after SR MOSFET is turned off, a ringing will appear on DRAIN voltage waveform. To void IC internal logic circuit false action, a blanking time T_{OFF_MIN} is also applied. During T_{OFF_MIN}, the SR logic can't begin a new switching cycle and the normal gate drive not allowed turning on.

ZVS Operation

The key function of SY23432 is achieving primary MOS ZVS turn on for high efficiency and high-power density. SY23432 is compatible with primary side QR IC to achieve this function.

SY23432 adopts proprietary drive method to increase resonation magnitude of switching node, which pulls $V_{Drain,P}$ to approximately ~50V to achieve primary side MOSFET ZVS turns on. The ZVS PWM only active in QR mode within 6 valleys, beyond this range, the ZVS is disabled.

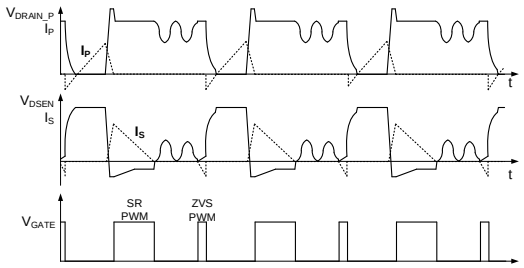


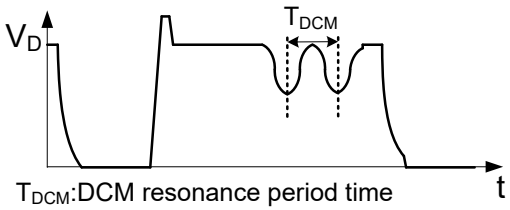
Fig. 6 ZVS control diagram

ZVS Coefficient R_{TZ} Setting

The ZVS performance is affected by transformer's magnetizing inductance (Lm) and the total equivalent capacitance (Csw) of switching node. To tune the best operation efficiency, the resistor value of TZ pin to GND can be adjusted. The resistor set ZVS PWM turn on time coefficient; it is choosing as follows.

$$R_{TZ} = \frac{\sqrt{C_{SW} \times L_m}}{4.5 \times 10^{-9}} \text{ (k}\Omega\text{)}$$

method 1, calculate coefficient base on magnetizing inductance and equivalent switching node capacitance capacitor.



$$R_{TZ} = \frac{T_{DCM}}{2\pi} \frac{1}{4.5\times10^{-9}}(\text{k}\Omega)$$

method 2, calculate coefficient base on DCM resonance period time

The resistor can be adjusted slightly around the calculated value. The resistance range is preferred to be 20kΩ-60kΩ, if it is <10kΩ or >100kΩ range, the ZVS function is disabled.

ZVS Enable Condition

1. Power supply: when VIN supply is active, ZVS is enabled. When DSEN supply is active, the ZVS is disabled. (DSEN pin supply power loss is much higher, the extra driving loss may be greater than ZVS affect)

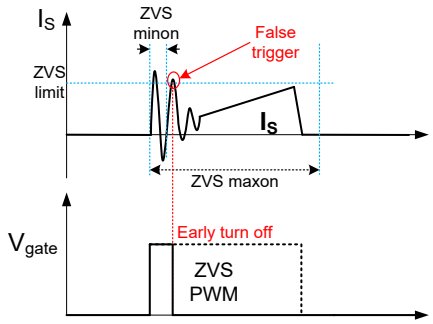
2. Input voltage condition: at low line input, the ZVS has little efficiency improvement. So, the input voltage range is limited to maximize ZVS effect. Input voltage condition calculation is shown as below with hysteresis:

ZVS enable: $V_{BULK} > N(0.333 \cdot V_{OUT} + 24V)$

ZVS disable: $V_{BULK} < N(0.333 \cdot V_{OUT} + 19V)$

ZVS Protection

To guarantee ZVS logic working correctly, the maximum ZVS on time is limited to 2.5us, so the primary side IC QR detecting timeout time must be greater than 2.5us+Treso. (Treso is the DCM resonating period).



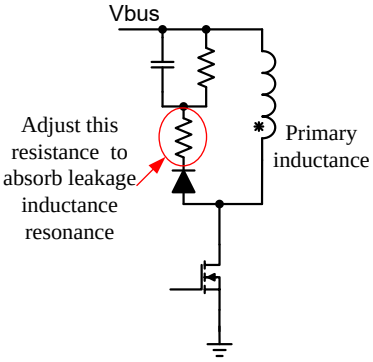
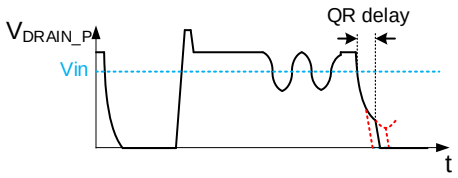


Fig. 7 ZVS limit protection

To prevent ZVS current is to big or primary false turn on, secondary current is limited during ZVS. But primary leakage inductance resonance may trigger ZVS limit, cause ZVS PWM turn off early, add primary inductance resonance absorb resistance is recommended.

ZVS Performance Adjust



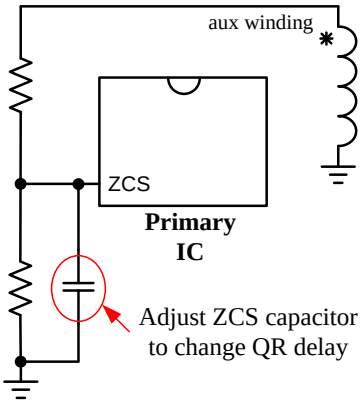


Fig. 8 adjust ZVS performance

To achieve best ZVS performance, primary IC QR delay need slightly adjust. Consider primary IC turn on at DCM resonance valley is the best.

Dual Channel Power Supply

When the output voltage is as low as 3V, which is not high enough to drive the SR MOSFET, the DSEN pin supply is preferred. When the output voltage is high, the power supply efficiency of DSEN pin is lower than VIN pin, the VIN pin supply is preferred.

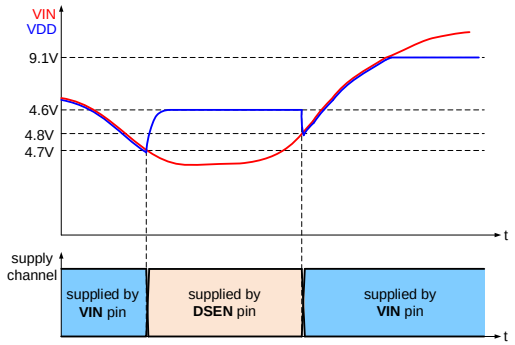


Fig.9 Timing diagram of dual channel supply

SY23432 adopts dual channel power supply. Before VDD voltage reaches ON threshold V_{VDD_ON}, SY23432 is supplied by DSEN pin. As V_{VDD} rises and reach ON threshold, VIN pin voltage will be monitored. If VIN voltage is higher than V_{VIN_VINSPY}, then power supply channel will switch to VIN pin. As VIN increase higher, VDD will follow V_{IN} (with about 0.5V voltage drop), finally VDD will be clamped to 9.1V. As VIN is decreasing and crossing V_{DSEN_VINSPY}, then the power supply channel will switch to DSEN pin and V_{DD} will be regulated to 4.6V. Timing diagram is shown in Fig.9.

Power Saving Mode

Under light load conditions, SY23432 will enter power saving mode to improve light load efficiency.

During each switching cycle, after SR MOSFET is turned off, a timer will start to count, if the timer has counted to 67us before next SR turn on instant, IC will enter power saving mode, and reduce the power consumption. IC will exit power saving mode by SR MOSFET turn on event.

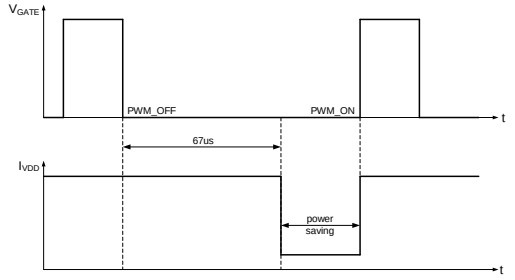


Fig. 10 timing diagram of power saving mode

Force Turn off

To prevent primary MOSFET and secondary MOSFET turned on at same time, the IC adopts force turn off function, which has higher priority than T_{ON_MIN}. When V_{DS} is above DSEN force turn off threshold $V_{DS\_FORCE\_TH}$ lasting for debounce time T_{DBC_FORCE}, SR GATE will turn off immediately.

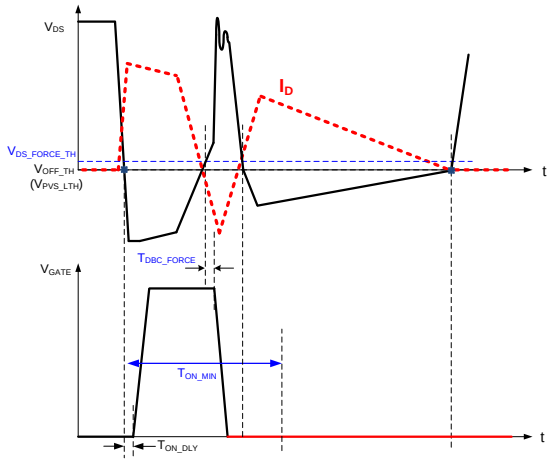


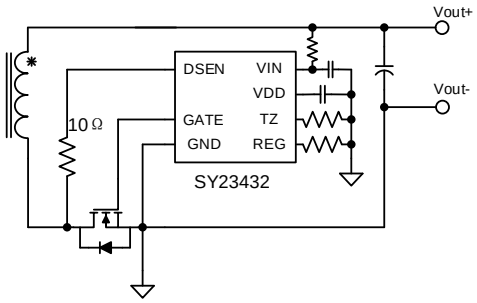
Fig.11 timing diagram of forced turn off

OTP

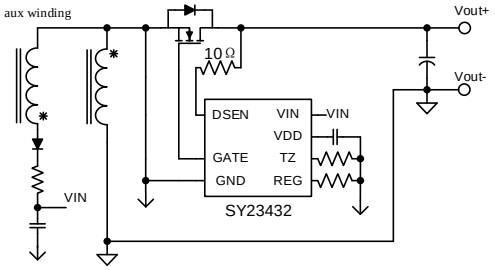
IC die temperature is always monitored, if the die temperature rises above 150℃, IC will stop driving SR MOS and keep GATE voltage to 0V. When temperature drops below 130℃, IC die will resume normal operating again.

Application Information

Typical System Implementations



Low side Rectification with Vout supply power

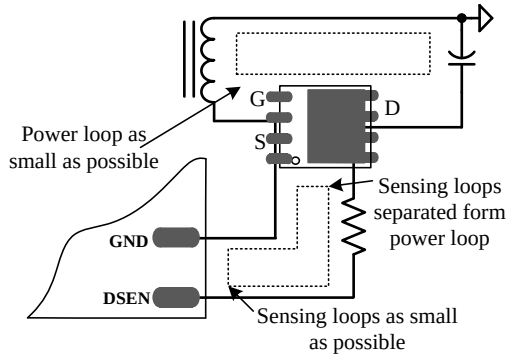


High side Rectification with aux winding supply power

Layout Guideline

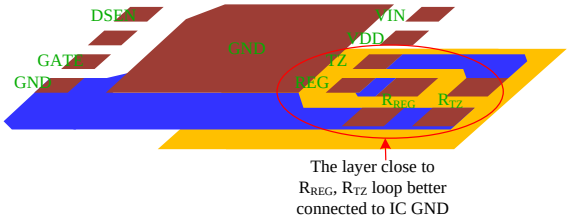
Sensing for DSEN/GND

1. Make the sensing connection (DSEN/GND) as close as possible to the MOSFET (drain/source).
2. Keep the IC out of the power loop to prevent the sensing loop and power loop from interrupting each other.



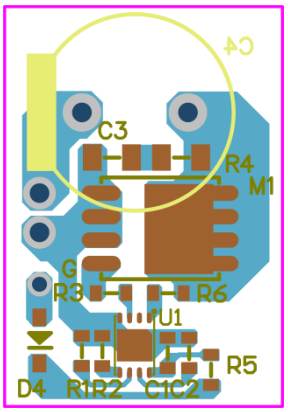
(a) To achieve better EMI and Efficiency performance, the output connector should be connected to the output cap first, then to the SR Power pin.

(b) The circuit loop of all switching circuit should be kept small: secondary power loop, secondary RC snubber circuit loop and IC power supply loop.

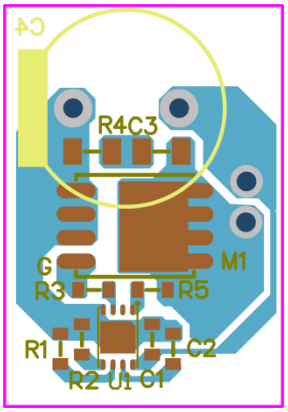


(c) Due to the high resistance on REG and TZ pin, the layout size and length of each loop should be as small as possible. Meanwhile, the layer directly under these two loops better connected to IC GND to shield switching noise.

Layout Example



High side SR layout @bottom view

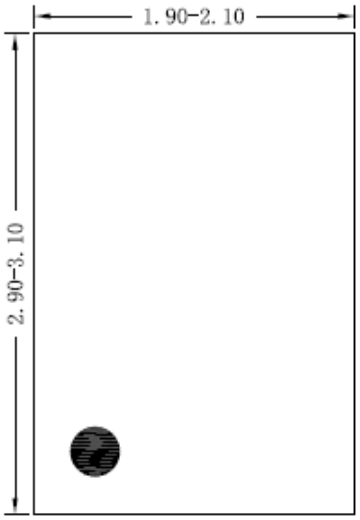


Low side SR layout @bottom view

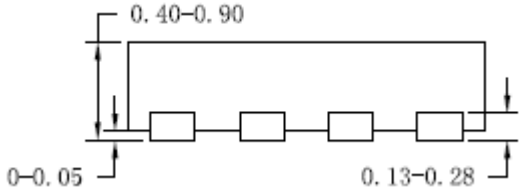
Design Notice

1. To achieve better EMI performance and reduce secondary rectifier loss, the circuit loop of secondary winding terminal, the output cap and SR MOSFET should be short.
2. To improve the system ESD performance, at least 10Ω resistor should be in series between VIN pin and Output cap, and at least 100nF cap should be in parallel between VIN pin and GND pin.
3. To achieve better ZVS effect, the SR MOSFET is recommended to use DFN or SO-8 package, which has a smaller package inductance that will not cause SR or ZVS turn off early.
4. The Ciss and Coss capacitors of SR MOSFET should be chosen as small as possible, Ciss is recommended not to exceed 6nF, and the ZVS effect will be better.
5. DSEN pin should be connected to Drain of SR MOSFET shortly.
6. GND pin should be connected to Source of SR MOSFET shortly.

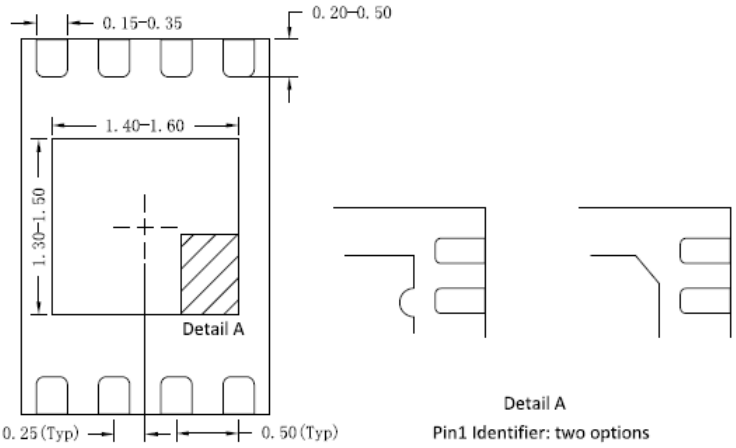
DFN2x3-8 Package Outline



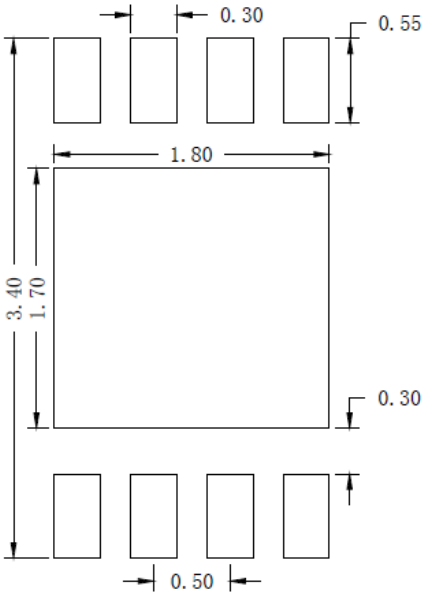
Top View



Side View



Bottom View



Recommended PCB layout
(Reference only)

Notes: **All dimension in millimeter and exclude mold flash & metal burr.**

Revision History

The revision history provided is for informational purpose only and is believed to be accurate, however, not warranted. Please make sure that you have the latest revision.

Date	Revision	Change
December 29, 2022	Revision 0.9A	Electrical Characteristics Modification
November 17, 2022	Revision 0.9	Initial Release

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