SQ82958

Octal, 16-Bit, SPI, Voltage Output DAC with Internal Reference

General Description

The SQ82958 is an octal, 16-bit, buffered voltage-output DAC with low power consumption. The device is a highly efficient and accurate digital-to-analog converter designed for applications requiring the conversion of digital signals into analog voltages. Operating within a voltage supply range of 2.7V to 5.5V, this device is suitable for a wide range of electronic systems. The SQ82958 includes an on-chip 1.25V/2.5V, 11 ppm/°C reference with an internal gain of two, providing full-scale output voltage range of 2.5V or 5V. The internal reference is turned off at power-up, and an external reference is enabled by default. The internal reference can be selected and enabled using a SPI write.

The SQ82958 power-on reset output voltages are set to 0V or midscale and remain at this level until a valid write occurs. The device has a power-down feature, which can significantly reduce current consumption to as low as 0.1µA at 3V (0.2µA at 5V), offering software selectable output load for individual or multiple DAC channels during power-down mode and optimizing power efficiency. The SQ82958 also offers a simultaneous update LDAC_N input pin, enabling the simultaneous update of all DAC outputs. This feature is further enhanced by the capability to select specific DAC channels for the simultaneous update, providing precise control over the output voltages. The device features an asynchronous CLR_N input pin that allows all DAC outputs to be updated to a user-programmable zero, midscale, or full scale.

The versatile 3-wire serial interface operates at clock rates of up to 50MHz and is compatible with standard SPI®, QSPI™, MICROWIRE™, and DSP interface standards. The on-chip precision output amplifiers facilitates rail-to-rail output swing.

The SQ82958 is available in a 4mm x 4mm 16-lead QFN package.

Features

- Low Power, Small Footprint, Octal, 16-bit DAC
- 2.7V to 5.5V Power Supply
- Power-down Capability
- Shutdown Current: 0.1µA at 3V and 0.2µA at 5V(typ.)
- On-chip 1.25V/2.5V, 11 ppm/°C Reference
- Power-on Reset to 0V or Midscale
- Configurable Power-down DAC Outputs
- Hardware/Software LDAC_N and LDAC_N Controls
- Software Configurable DAC Output Reset to 0V, Mid-Scale or Full Scale
- Rail-to-rail Operation
- Available in 16-lead QFN Package

Applications

- Optical Networking
- Battery Test Equipment
- Industrial Automation
- Data Acquisition Systems

Typical Application

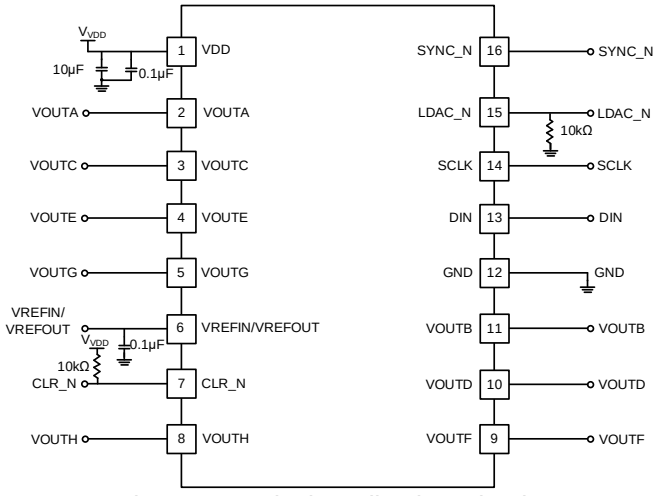


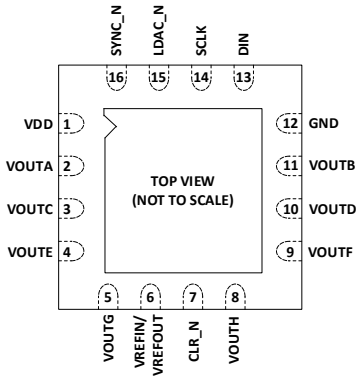
Figure 1. Typical Application Circuit

Ordering Information

Ordering Part Number	Package Type	Top Mark	Note
SQ82958QIQ	QFN4×4-16	**FMYxyz**	16-bit, 1.25V internal reference, power-on reset to 0V
SQ82958BQIQ	QFN4×4-16	**AACM*xyz***	16-bit, 1.25V internal reference, power-on reset to midscale
SQ82918QIQ	QFN4×4-16	**AACGxyz**	12-bit, 1.25V internal reference, power-on reset to 0V

Note: ***x = year code, y = week code, z = lot number code.***

Pinout (Top View)



(QFN4×4-16)

Pin Description

Pin No.	Pin Name	Pin Description
1	VDD	Power Supply Input (2.7 to 5.5V).
2	VOUTA	Analog Output Voltage from DAC A.
3	VOUTC	Analog Output Voltage from DAC C.
4	VOUTE	Analog Output Voltage from DAC E.
5	VOUTG	Analog Output Voltage from DAC G.
6	VREFIN/ VREFOUT	The device has a common pin for reference input and reference output. When using the internal reference, this is the reference output pin. When using an external reference, this is the reference input pin. The default for this pin is as a reference input.
7	CLR_N	Asynchronous Clear Input. The CLR_N input is falling edge sensitive. When CLR_N is low, all LDAC_N pulses are ignored. When CLR_N is activated, the input register and the DAC registers are updated with the data contained in the CLR_N code register-zero, midscale, or full scale. Default setting is 0V for all the outputs.
8	VOUTH	Analog Output Voltage from DAC H.
9	VOUTF	Analog Output Voltage from DAC F.
10	VOUTD	Analog Output Voltage from DAC D.
11	VOUTB	Analog Output Voltage from DAC B.
12	GND	Ground reference level for all circuitry.
13	DIN	Serial Data Input. This device has a 32-bit shift register. Data is clocked into the register on the falling edge of the serial clock input.
14	SCLK	Serial Clock Input. The interface supports clock rates up to 50MHz.
15	LDAC_N	Pulsing this pin low allows any or all DAC registers to be simultaneously updated if the input registers have new data. Alternatively, this pin can be tied permanently low.
16	SYNC_N	Active Low Control Input. This serves as the frame synchronization signal for the input data. Upon its transition to a low state, it activates the SCLK and DIN buffers, enabling the input shift register. The subsequent data transfer occurs during the falling edges of the next 32 clocks. If the signal returns to a high state prior to the 32nd falling edge, The next rising edge functions as an interrupt and the write sequence is disregarded.

Block Diagram

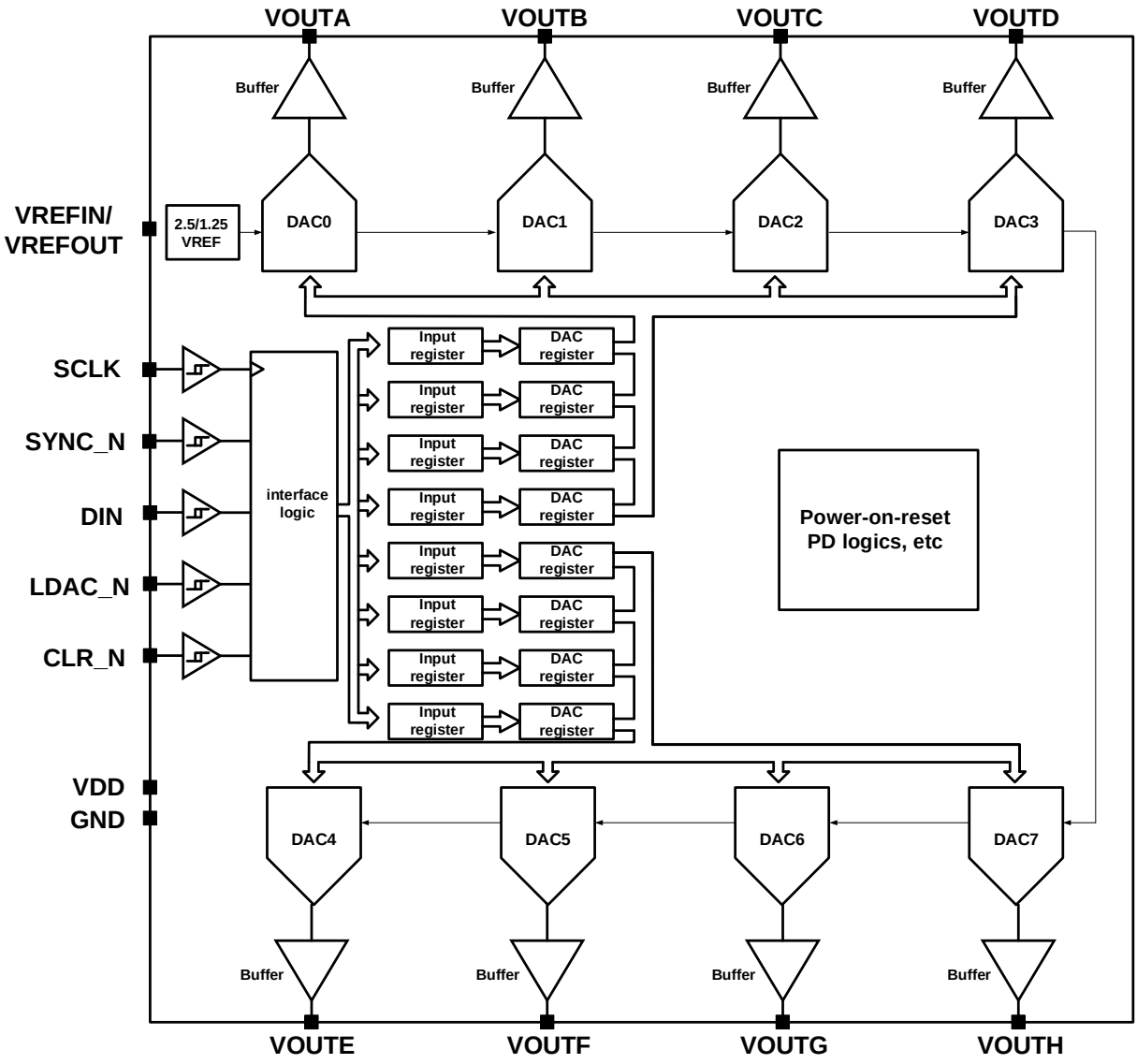


Figure 2. Functional Block Diagram

Absolute Maximum Ratings

Parameter (Note 1)	Min	Max	Unit
VDD	-0.3	6.5	V
DIN, SCLK, SYNC_N, LDAC_N, CLR_N (Digital Inputs)	-0.3	V_{VDD}+0.3	
VOUTA ~ VOUTH	-0.3	V_{VDD}+0.3	
VREFIN/VREFOUT	-0.3	V_{VDD}+0.3	
Junction Temperature	-40	150	°C
Storage Temperature	-65	150	
Reflow Soldering Peak Temperature		260	
ESD: HBM (Human Body Model)	± 3000		V
ESD: CDM (Charged Device Model)	± 750		V

Thermal Information

Parameter (Note 2)	Value	Unit
θ_{JA} Junction-to-Ambient Thermal Resistance	29	°C/W
θ_{JC} Junction-to-Case (Top) Thermal Resistance	18	
θ_{JB} Junction-to-Board Thermal Resistance	15	

Recommended Operating Conditions

Parameter (Note 3)	Min	Max	Unit
Operation Ambient Temperature Range	-40	125	°C
Operation Junction Temperature Range	-40	135	°C
VDD	2.7	5.5	V
Digital Inputs	0	V_{VDD}	V

Electrical Characteristics

V_{VDD}= 2.7V to 5.5V, R_L = 2kΩ to GND, C_L = 200pF to GND, V_{REFIN} = V_{VDD}. T_A = -40°C to 125°C, typical values are T_A = 25°C, unless otherwise noted (Note 4).

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Static Performance						
Resolution	RES		16			LSB
Integral Nonlinearity	INL	Code range of 512 to 65024, Output unloaded, V_{VDD} = 4.5V – 5.5V		±0.78	±3.5	LSB
		Code range of 512 to 65024, Output unloaded, V_{VDD} = 2.7V – 3.6V		±0.68	±3.5	LSB
Differential Nonlinearity	DNL	Code range of 512 to 65024, Output unloaded, V_{VDD} = 4.5V – 5.5V		±0.57	±3.1	LSB
		Code range of 512 to 65024, Output unloaded, V_{VDD} = 2.7V – 3.6V		±0.55	±3.1	LSB
Zero Code Error (Refer to 错误!未找到引用源。)		V_{VDD} = 4.5V – 5.5V		0.24	5.2	mV
		V_{VDD} = 2.7V – 3.6V		0.25	3.9	mV
Zero Code Error Drift (Note 5)		V_{VDD} = 5V		±2.6		μV/°C
		V_{VDD} = 3V		±2.1		μV/°C
Full Scale Error	FSE	V_{VDD} = 4.5V – 5.5V		±0.06	±0.32	%FSR
		V_{VDD} = 2.7V – 3.6V		±0.04	±0.30	%FSR
Gain Error	GE	V_{VDD} = 4.5V – 5.5V		±0.06	±0.29	%FSR
		V_{VDD} = 2.7V – 3.6V		±0.04	±0.26	%FSR
Gain Temperature Coefficient (Note 5)		Of FSR/°C, V_{VDD} = 5V		±2.0		ppm
		Of FSR/°C, V_{VDD} = 3V		±3.0		ppm
Offset Error	OFE	V_{VDD} = 4.5V – 5.5V		±0.65	±7.9	mV
		V_{VDD} = 2.7V – 3.6V		±0.26	±4.3	mV
DC Power Supply Rejection Ratio (Note 5)	DC_PSRR	V_{VDD} ± 10%, V_{VDD} = 5V		-78		dB
		V_{VDD} ± 10%, V_{VDD} = 3V		-78		dB
DC Crosstalk (External Reference) (Note 5) (Refer to 错误!未找到引用源。)		Full-scale change, R_L = 2kΩ to GND or V_{VDD}, V_{VDD} = 5V		±40		μV
		Full-scale change, R_L = 2kΩ to GND or V_{VDD}, V_{VDD} = 3V		±27		μV
		Load current change, V_{VDD} = 5V		±42		μV/mA
		Load current change, V_{VDD} = 3V		±55		μV/mA
		Powering down, V_{VDD} = 5V		±30		μV
		Powering down, V_{VDD} = 3V		±22		μV
DC Crosstalk		Full-scale change, R_L = 2kΩ to GND or V_{VDD}, V_{VDD} = 5V		±37		μV

(Internal Reference) (Note 5) (Refer to 错误!未找到引用源。)		Full-scale change, R_L = 2kΩ to GND or V_{VDD}, V_{VDD} = 3V		±30		μV
		Load current change, V_{VDD} = 5V		±38		μV/mA
		Load current change, V_{VDD} = 3V		±56		μV/mA
Output Characteristics						
Output Voltage Range (Note 5)	V_{OUT}		0		V_{VDD}	V
Capacitive Load Stability (Note 5)	C_L	R_L = ∞		2		nF
		R_L = 2 kΩ		10		nF
DC Output Impedance (Note 5)	R_{OUT}			0.07		Ω
Short-Circuit Current (Note 5)	I_{SHORT}	V_{VDD} = 5V		81		mA
		V_{VDD} = 3V		81		mA
Output Current (Note 5)	I_{OUT}	Headroom = 0.2V	30			mA
Output Headroom		Single channel output current = 30mA, V_{VDD} = 4.5V – 5.5V		90	200	mV
		Single channel output current = 30mA, V_{VDD} = 2.7V – 3.6V		150	300	mV
Power-up Time (Note 5)		Coming out of power-down mode, V_{VDD} = 5 V		3.5		μs
		Coming out of power-down mode, V_{VDD} = 3 V		3.0		μs
Reference Inputs						
Reference Current	I_{REFIN}	V_{REF} = V_{VDD} = 5.5 V (per DAC channel)		55		μA
Reference Input Range	V_{REFIN}		0		V_{VDD}	V
Reference Input Impedance	R_{FEFIN}			100		kΩ
Reference Output						
Output Voltage	V_{REFOUT}	V_{VDD} = 4.5V – 5.5V		2.5		V
		V_{VDD} = 2.7V – 3.6V		1.25		V
Reference TC (Note 5)				11		ppm/°C
Reference Output Impedance (Note 5)	R_{REFOUT}	V_{VDD} = 5V		0.04		Ω
		V_{VDD} = 3V		0.14		Ω
Logic Inputs (Note 5)						
Input Current		All digital inputs			±0.33	μA
Input Low Voltage	V_{INL}	V_{VDD} = 4.5V – 5.5V			0.8	V
		V_{VDD} = 2.7V – 3.6V			0.6	V
Input High Voltage	V_{INH}	V_{VDD} = 4.5V – 5.5V	2.9			V
		V_{VDD} = 2.7V – 3.6V	2			
Pin Capacitance				3		pF
Power Requirements						
Power Supply Voltage	V_{VDD}	All digital inputs at 0 or V_{VDD}, DAC active, excludes load current, V_{VDD} = 4.5V – 5.5V	4.5	5	5.5	V
		All digital inputs at 0 or V_{VDD}, DAC active, excludes load current, V_{VDD} = 2.7V – 3.6V	2.7	3	3.6	V

VDD Current (Normal Mode)	I_{DD}	Interface inactive. All DACs active. DAC outputs unloaded. V_{IH} = V_{VDD} and V_{IL} = GND, Internal reference off, V_{VDD} = 4.5V – 5.5V		4.0	7.2	mA
		Interface inactive. All DACs active. DAC outputs unloaded. V_{IH} = V_{VDD} and V_{IL} = GND, Internal reference off, V_{VDD} = 2.7V – 3.6V		3.6	6.6	mA
		Interface inactive. All DACs active. DAC outputs unloaded. V_{IH} = V_{VDD} and V_{IL} = GND, Internal reference on, V_{VDD} = 4.5V – 5.5V		4.4	8.1	mA
		Interface inactive. All DACs active. DAC outputs unloaded. V_{IH} = V_{VDD} and V_{IL} = GND, Internal reference on, V_{VDD} = 2.7V – 3.6V		4.2	7.6	mA
VDD Current (All Power-Down Modes)	I_{DD}	All eight DACs powered down, V_{IH} = V_{DD} and V_{IL} = GND, V_{VDD} = 4.5V – 5.5V		0.2	4.5	μA
		All eight DACs powered down, V_{IH} = V_{VDD} and V_{IL} = GND, V_{VDD} = 2.7V – 3.6V		0.1	3.0	μA
AC Characteristics (Each output)						
Output Voltage Settling Time		¼ to ¾ scale settling to ±2 LSB		3.0		μs
Slew Rate	SR			1.5		V/μs
Multiplying Bandwidth (Refer to 错误!未找到引用源。)		V_{REF} = 2 V ± 0.2Vpp		400		kHz
Total Harmonic Distortion (Refer to 错误!未找到引用源。)	THD	V_{REF} = 2 V ± 0.2Vpp, frequency = 10kHz		-78		dB
Output Noise Spectral Density	NSD	DAC code = 0x8400, 10kHz		113		nV/√Hz
Output Noise		0.1Hz to 10Hz, DAC code = 0x0000		71		μV p-p

Note 1: Stresses beyond the “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

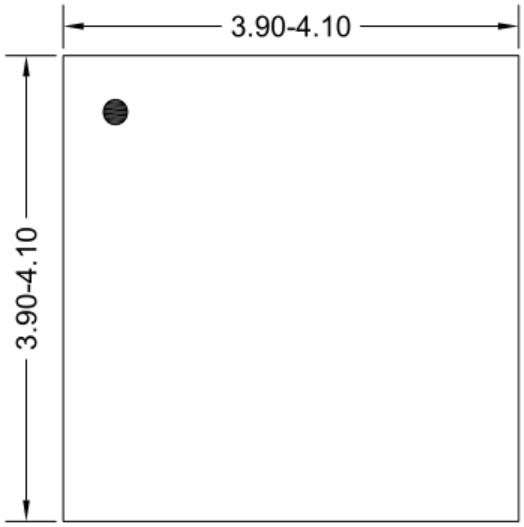
Note 2: Package thermal resistance is measured in the natural convection at T_A = 25˚C on an 8.5cm×8.5cm four-layer Silergy Evaluation Board.

Note 3: The device is not guaranteed to function outside its operating conditions.

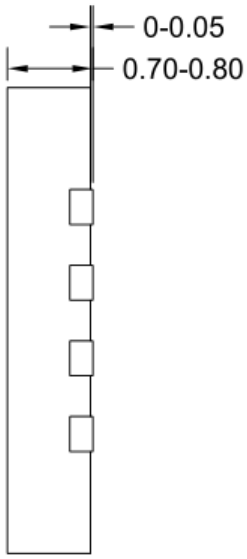
Note 4: Production tested at 25°C. Limits are guaranteed by design, test or statistical correlation.

Note 5: Guaranteed by design and characterization; not production tested.

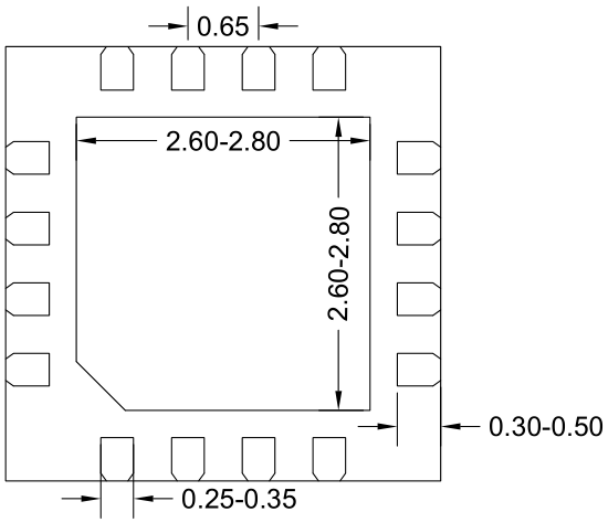
QFN4x4-16 Package Outline Drawing



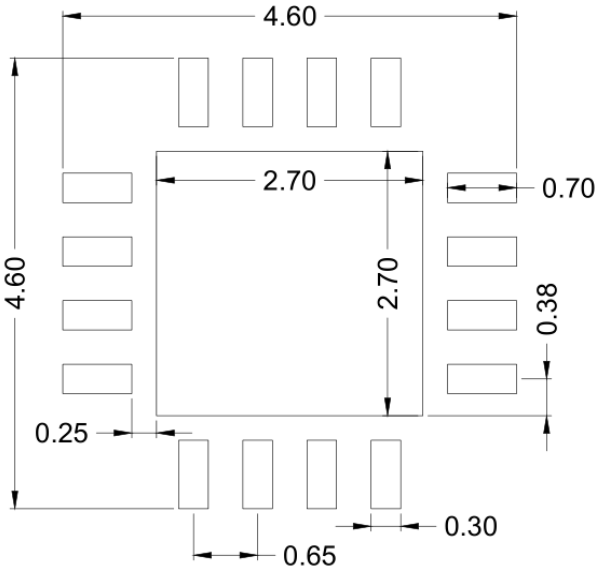
Top View



Side View



Bottom View

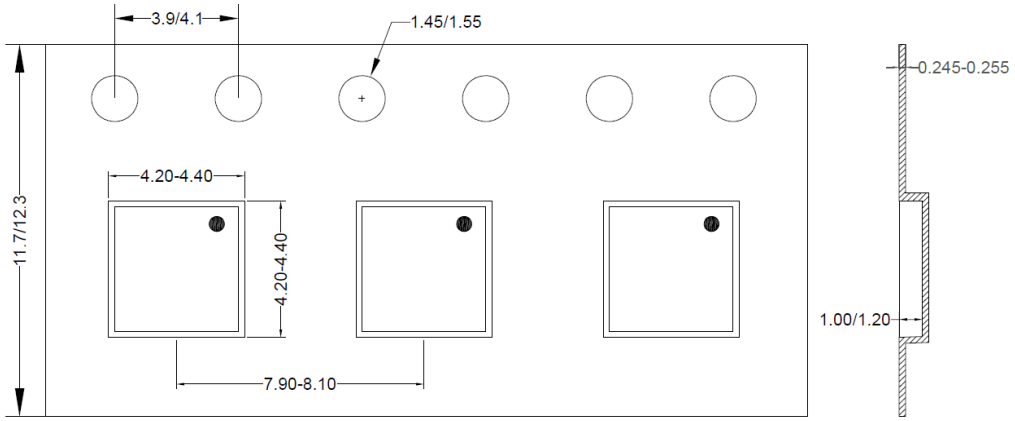


Recommended PCB layout
(Reference only)

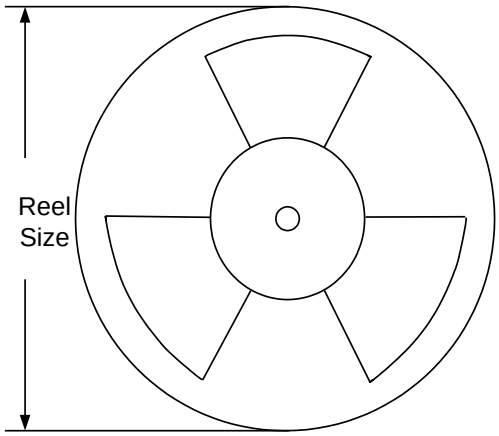
Notes: **All dimension in millimeter and exclude mold flash & metal burr.**

Taping & Reel Specification

1. QFN4x4 Taping orientation



2. Carrier Tape & Reel specification for packages



Package types	Tape width (mm)	Pocket pitch(mm)	Reel size (Inch)	Trailer * length(mm)	Leader * length (mm)	Qty per reel (pcs)
QFN4x4	12	8	13"	400	400	5000

3. Others: NA

Revision History

The revision history provided is for informational purpose only and is believed to be accurate, however, not warranted. Please make sure that you have the latest revision.

Date	Revision	Change
Mar. 15, 2024	Revision 1.0	Initial Release

IMPORTANT NOTICE

1. **Right to make changes.** Silergy and its subsidiaries (hereafter Silergy) reserve the right to change any information published in this document, including but not limited to circuitry, specification and/or product design, manufacturing or descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products are sold subject to Silergy's standard terms and conditions of sale.

2. Applications. Application examples that are described herein for any of these products are for illustrative purposes only. Silergy makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification. Buyers are responsible for the design and operation of their applications and products using Silergy products. Silergy or its subsidiaries assume no liability for any application assistance or designs of customer products. It is customer's sole responsibility to determine whether the Silergy product is suitable and fit for the customer's applications and products planned. To minimize the risks associated with customer's products and applications, customer should provide adequate design and operating safeguards. Customer represents and agrees that it has all the necessary expertise to create and implement safeguards which anticipate dangerous consequences of failures, monitor failures and their consequences, lessen the likelihood of failures that might cause harm and take appropriate remedial actions. Silergy assumes no liability related to any default, damage, costs or problem in the customer's applications or products, or the application or use by customer's third-party buyers. Customer will fully indemnify Silergy, its subsidiaries, and their representatives against any damages arising out of the use of any Silergy components in safety-critical applications. It is also buyers' sole responsibility to warrant and guarantee that any intellectual property rights of a third party are not infringed upon when integrating Silergy products into any application. Silergy assumes no responsibility for any said applications or for any use of any circuitry other than circuitry entirely embodied in a Silergy product.

3. **Limited warranty and liability.** Information furnished by Silergy in this document is believed to be accurate and reliable. However, Silergy makes no representation or warranty, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information. In no event shall Silergy be liable for any indirect, incidental, punitive, special or consequential damages, including but not limited to lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges, whether or not such damages are based on tort or negligence, warranty, breach of contract or any other legal theory. Notwithstanding any damages that customer might incur for any reason whatsoever, Silergy' aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the Standard Terms and Conditions of Sale of Silergy.

4. **Suitability for use.** Customer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of Silergy components in its applications, notwithstanding any applications-related information or support that may be provided by Silergy. Silergy products are not designed, authorized or warranted to be suitable for use in life support, life-critical or safety-critical systems or equipment, nor in applications where failure or malfunction of a Silergy product can reasonably be expected to result in personal injury, death or severe property or environmental damage. Silergy assumes no liability for inclusion and/or use of Silergy products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

5. **Terms and conditions of commercial sale**. Silergy products are sold subject to the standard terms and conditions of commercial sale, as published at https://www.silergy.com, unless otherwise agreed in a valid written individual agreement specifically agreed to in writing by an authorized officer of Silergy. In case an individual agreement is concluded only the terms and conditions of the respective agreement shall apply. Silergy hereby expressly objects to and denies the application of any customer's general terms and conditions with regard to the purchase of Silergy products by the customer.

6. **No offer to sell or license**. Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights. Silergy makes no representation or warranty that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right. Information published by Silergy regarding third-party products or services does not constitute a license to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from Silergy under the patents or other intellectual property of Silergy.

For more information, please visit: www.silergy.com