SY2A58152

Twelve Half-Bridge Driver with SPI Control

General Description

The SY2A58152 is a twelve half-bridge motor driver solution for automotive, industrial, and other mechatronic applications. These half-bridges are fully controllable, facilitating the motor's forward, reverse, coasting, and braking operations. All functions are programmable via a serial peripheral interface (SPI).

The SY2A58152 provides internal shutdown functions and an nFAULT output pin to alert the system in the event of a fault. It is also equipped with protection features including overcurrent protection, open load detection, undervoltage lockout, overvoltage lockout, and thermal shutdown. The device is available in a QFN5×5-24 package with an exposed pad for enhanced thermal dissipation.

Features

- Operating Voltage: 4.5V to 32V
- Compatible with a 5V/3.3V Systems
- 12 Half-Bridge Outputs
- Up to 1A Output Current for Each Output
- Low-Power Sleep Mode
- Serial Peripheral Interface, Up to 5MHz
- Daisy Chain Functionality
- PWM Capable Output for Frequencies of 80Hz, 100Hz, 200Hz and 2kHz with an 8-Bit Duty Cycle Resolution
- Integrated Protection Features:
  - Overcurrent Protection
  - Short-Circuit Protection
  - Open Load Detection
  - Undervoltage Lockout
  - Overvoltage Protection
  - Thermal Shutdown
- nFAULT Pin Output
- QFN5×5-24 Package
- AEC-Q100 Qualified

Applications

- Automotive
- HVAC
- DC Brushed Motors
- LEDs

Typical Application

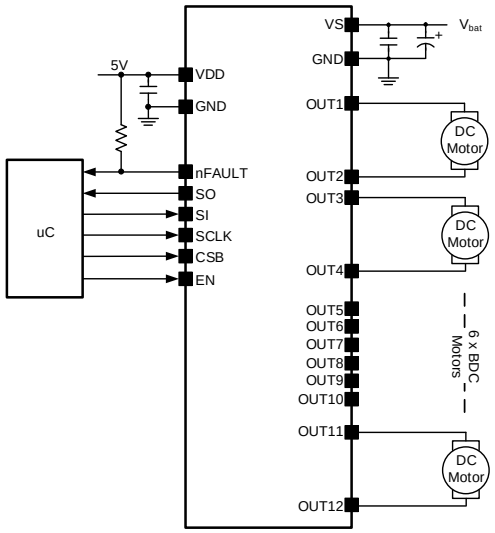


Figure 1. Typical Application Circuit

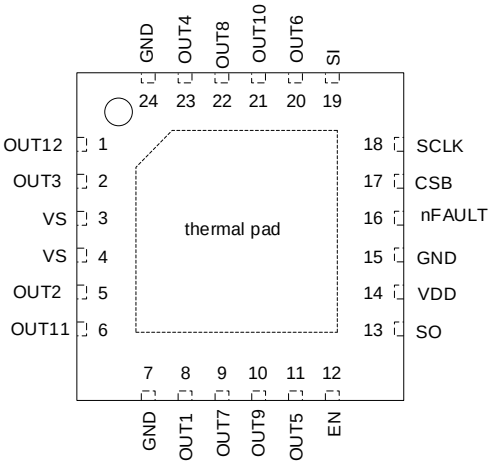
© 2023 Silergy Corp. All Rights Reserved.

Ordering Information

Ordering Part Number	Package Type	Top Mark
SY2A58152VAQ	QFN5×5-24 RoHS Compliant and Halogen Free	***FWWxyz***

x=year code, y=week code, z= lot number code

Pinout (Top View)



Pin Name	Pin No.	Pin Description
OUT12	1	Half-bridge Output 12.
OUT3	2	Half-bridge Output 3.
VS	3,4	Power supply for half bridges.
OUT2	5	Half-bridge Output 2.
OUT11	6	Half-bridge Output 11.
OUT1	8	Half-bridge Output 1.
OUT7	9	Half-bridge Output 7.
OUT9	10	Half-bridge Output 9.
OUT5	11	Half-bridge Output 5.
EN	12	Enable. Logic high enables the IC. Internal pull down.
SO	13	Serial data output. 16-bit serial communications output.
VDD	14	Power supply for internal logic.
GND	7,15,24	Ground. Internal connection to lead frame.
CSB	17	Chip select. Active low serial port enable.
SCLK	18	Serial clock. SPI interface clock input.
SI	19	Serial data input. SPI interface 16-bit serial data input.
OUT6	20	Half-bridge Output 6.
OUT10	21	Half-bridge Output 10.
OUT8	22	Half-bridge Output 8.
OUT4	23	Half-bridge Output 4.
nFAULT	16	Fault indicator output. Open drain output. This pin is pulled logic low during a fault condition and requires an external pull-up resistor.

© 2023 Silergy Corp. All Rights Reserved.

Function Block

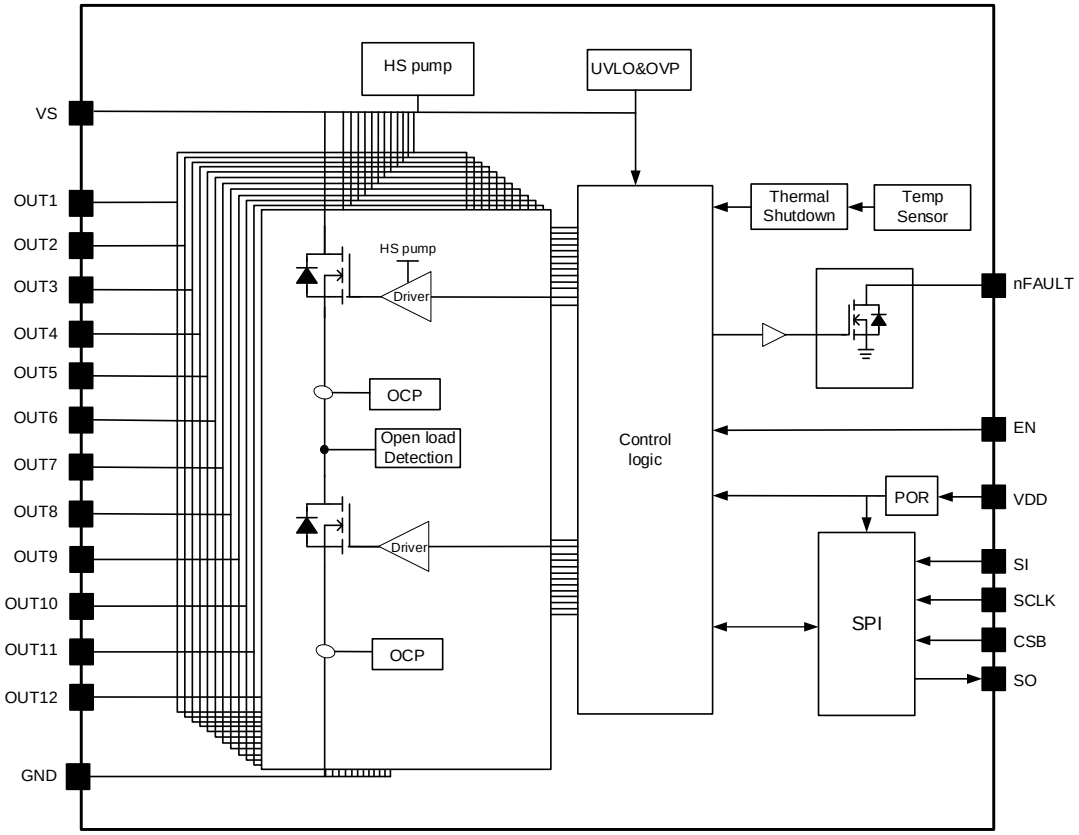


Figure 2. SY2A58152 Function Block Diagram

© 2023 Silergy Corp. All Rights Reserved.

Absolute Maximum Ratings (Note 1)

Parameter	Min	Max	Unit
VS (DC)	-0.3	40	V
OUTx(DC	-0.3	VS+0.7	V
Digital Pins (SI, SCLK, CS, SO, EN, nFAULT)	-0.3	VDD+0.3	V
VDD	-0.3	5.75	V
Continuous Supply Current (VS pins) (Note 2)	0	6	A
Continuous Sink Current (GND pins) (Note 2)	0	6	A
Junction Temperature (T_J)	-40	150	°C
Storage Temperature	-65	150	°C

Thermal Information

Parameter(Note 3)	Typ.	Unit
θ_{JA} Junction-to-ambient Thermal Resistance(QFN5×5-24)	22	°C/W
$\theta_{JC\ TOP}$ Junction-to-case Thermal Resistance(QFN5×5-24)	12	

Recommended Operating Conditions

Parameter	Min	Max	Unit
VS	4.5	32	V
VDD	3.15	5.5	V
Digital Pins	0	5.5	V
nFAULT Pullup Voltage	0	5.5	V
nFAULT Output Current	0	5	mA
Operating Temperature (T_A)	-40	125	°C
Junction Temperature (T_J)	-40	150	°C

© 2023 Silergy Corp. All Rights Reserved.

Electrical Characteristics

(-40°C <T_A < 125°C, 4.5V< VS <32V, 3.15V<VDD<5.5V, EN=VDD, unless otherwise specified)

Parameter		Symbol	Test Conditions	Min	Typ	Max	Unit
Power Supplies	VS Sleep Mode Current	I_{VS_sleep}	VS =13.5V, EN=L, T_A=25°C		0.35	1	μA
			VS =13.5V, EN=L, T_A=125°C			4.5	μA
	VS Standby Mode Current	$I_{VS_standby}$	VS=13.5V, EN=H, Driver=OFF,T_A=25°C		0.5	0.7	mA
			VS=13.5V, EN=H, Driver=OFF,T_A=125°C			0.7	mA
	VS Operating Mode Current	I_{VS}	VS=13.5V, EN=H, All High-Side, FETs=ON, T_A=25°C		2.6	4	mA
			VS=13.5V, EN=H, All High-Side, FETs=ON, T_A=125°C			4	mA
	VS Undervoltage Lockout Voltage	V_{UVLO_FALL}	VS falling	3.8		4.3	V
		V_{UVLO_RISE}	VS rising	4		4.5	V
		V_{UVLO_HYS}			200		mV
	VS Undervoltage Lockout Deglitch Time	t_{UVLO}			10		μs
	VS Overvoltage Protection	V_{OVP}	VS rising, EXT_OVP=0b	21		25	V
			VS falling, EXT_OVP=0b	20		24	V
			VS rising, EXT_OVP=1b	32.6		35.1	V
			VS falling, EXT_OVP=1b	32		34.5	V
		V_{OVP_HYS}	Rising to falling threshold, EXT_OVP=0b		1		V
			Rising to falling threshold, EXT_OVP=1b		0.7		V
	VS Overvoltage Protection Deglitch Time	t_{OVP}			10		μs
	VDD Power On Reset Threshold	V_{POR_ON}	Supply rising	2.75		3.05	V
	VDD Power Off Reset Threshold	V_{POR_OFF}	Supply falling	2.6		2.9	V
	POR Undervoltage Hysteresis	V_{POR_HYS}	Rising to falling threshold		150		mV
	VDD Operating Supply Current	I_{VDD}	VS=13.5V, VDD=3.3V, EN=H, all low-side FETs=ON, SPI=ON, T_A=25°C		3.5	5	mA
			VS =13.5V, VDD=3.3V, EN=H, all low-side FETs=ON, SPI=ON, T_A=125°C			5	mA
	VDD Standby Mode Current	$I_{VDD_standby}$	VS=13.5V, VDD=3.3V, EN=H,SPI=OFF, T_A=25°C		2	3	mA
			VS=13.5V, VDD=3.3V, EN=H,SPI=OFF, T_A=125°C			3	mA
	VDD Sleep Mode Current	I_{VDD_sleep}	VS=13.5V, VDD=3.3V, EN=L, T_A=25°C		1.1	2	μA
			VS=13.5V, VDD=3.3V, EN=L, T_A=125°C			2	μA
Logic Level Input (EN, SI, SCLK, CSB)	Input Low Voltage	V_{IL}		0		0.6	V
	Input High Voltage	V_{IH}		2			
	Input Logic Hysteresis	V_{HYS}		200			mV
	Input Low Current	I_{IL}	VIN=0V	-1		1	μA
	Input High Current	I_{IH}	VIN=VDD		60	100	μA
	Input Capacitance	C_{CAPINX}	(Note 4)		-	15	pF
Open-Drain Output(nFAULT)	Output Low Voltage	V_{OL}	I_{sink}=5mA	0		0.4	V
	Output High Current	I_{OH}	V_{OD}=5V	-1		1	μA
	Output Capacitance	C_{OD}	(Note 4)	-	-	15	pF
Push-pull Output (SO) (Note 4)	Output Low Voltage	V_{OL}	I_{out}= -5mA (Note 4)	0		0.4	V
	Output High Voltage	V_{OH}	I_{out}= 5mA (Note 4)	VDD-0.6		VDD	V
	Output Capacitance	C_{OD}	(Note 4)			30	pF
	Output Low Current	I_{OL}	V_{SO}=0V	-1		1	μA

© 2023 Silergy Corp. All Rights Reserved.

	Output High Current	I_{OH}	V_{SO}=VDD		-1		1	μA
Power MOSFETs	High Side FETs on Resistance	R_{DSON}	I_{out}=500mA	VS=13.5V		0.75	1.6	Ω
	Low Side FETs on Resistance		I_{out}=500mA	VS=13.5V		0.75	1.6	
	Output Rise and Fall Time (HS&LS)	$SL_{rise\ and\ fall}$	VS=13.5V,10-90%, R_{LOAD}=27Ω, HBx_SR=0b			1		V/μs
			VS=13.5V,10-90%, R_{LOAD}=27Ω, HBx_SR=1b			3.7		V/μs
	Output Dead Time (High to Low / Low to High)	t_{DEAD}	VS =13.5V, SR=0, HS/LS driver OFF to LS/HS driver ON		6	15	25	μs
			VS =13.5V, SR=1, HS/LS driver OFF to LS/HS driver ON		2	5	15	μs
	Propagation Delay (Hide-side and Low-side ON/OFF)	t_{PD}	High-side ON or low-side ON command (SPI last transition) to OUTx transition from Hi-Z state, SR=0		3	6	15	μs
			High-side ON or low-side ON command (SPI last transition) to OUTx transition from Hi-Z state, SR=1		1	3	8	μs
	Source Leakage Current	I_{source_LC}	OUTx=0V, EN=1			6	10	μA
			OUTx=0V, EN=0				2	μA
	Sink Leakage Current	I_{sink_LC}	OUTx=13.5V, EN=1, SR=0b			13.5	20	μA
			OUTx=13.5V, EN=1, SR=1b			13.5	20	μA
			OUTx=13.5V, EN=0, SR=0b				2	μA
PWM Mode	PWM Switching Frequency	f_{PWM}	PWM_CHx_FREQ=00b		56	80	104	Hz
			PWM_CHx_FREQ=01b		70	100	130	Hz
			PWM_CHx_FREQ=10b		140	200	260	Hz
			PWM_CHx_FREQ=11b		1400	2000	2600	Hz
Protections	Thermal Warning Temperature	T_{WARN}	(Note 4)		120	140	170	°C
	Thermal Warning Hysteresis	T_{WARN_HYS}	(Note 4)			20		°C
	Thermal Shutdown Temperature	T_{SD}	(Note 4)		150	165	185	°C
	Thermal Shutdown Hysteresis	T_{HYS}	(Note 4)			20		°C
	Over Current Shutdown Threshold (Source)	I_{OCSO}	VDD=5V, VS=13.5V		-2.3	-1.8	-1.3	A
	Over Current Shutdown Threshold (Sink)	I_{OCSI}	VDD=5V, VS=13.5V		1.3	1.8	2.3	A
	Over Current Shutdown Delay Time	t_{oc}	OCP_DEG=000b		6	10	14.5	μs
			OCP_DEG=001b(Note 4)		2.6	5	7.9	μs
			OCP_DEG=010b(Note 4)		0.4	2.5	5.9	μs
			OCP_DEG=011b		0.1	1	3.4	μs
			OCP_DEG=100b		38.2	60	80	μs
			OCP_DEG=101b(Note 4)		23.1	40	51.9	μs
			OCP_DEG=110b(Note 4)		18.5	30	41.5	μs
			OCP_DEG=111b(Note 4)		8.4	20	31.6	μs
	Open Load Detection Current	I_{OLD}	High-side or Low side		2	9	18	mA
	Open Load Detection Current in Low Current OLD Mode	I_{OLD_LOW}	Low side		0.2	0.8	2	mA
	Open Load Detection Delay Time	t_{OLD}	Continuous Mode		2.2	3	3.8	ms
			PWM Mode		150	200	300	μs

© 2023 Silergy Corp. All Rights Reserved.

Serial Peripheral Interface

(-40°C <T_A < 125°C, 4.5V< VS <32V, 3.15V<VDD<5.5V, EN=VDD, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
SCLK Frequency	f_{CLK}	(Note 4)			5	MHz
SCLK High Time	t_{CLKH}	(Note 4)	100			ns
SCLK Low Time	t_{CLKL}	(Note 4)	100			ns
SI Setup Time	t_{SU_SI}	(Note 4)	40			ns
SI Hold Time	t_{HD_SI}	(Note 4)	60			ns
SO Output Data Delay Time	t_{DLY_SO}	SCLK high to SO valid(Note 4)			60	ns
CSB Setup Time	t_{SU_CSB}	(Note 4)	100			ns
CSB Hold Time	t_{HD_CSB}	(Note 4)	100			ns
CSB Disable Delay Time	t_{DIS_CSB}	CSB high to SO High-Z (Note 4)		30		ns
CSB Minimum High Time before Active Low	t_{HI_CSB}	(Note 4)	600			ns
EN Low Valid Time	t_{ENL}	VDD=5V, EN going low 50% to OUTx turning off 50% (Note 4)	10			μs
EN High to SPI Valid	t_{ENH_SPIV}	(Note 4)			100	μs

Note 1: Stresses listed as the above "Absolute Maximum Ratings" may cause permanent damage to the device. These are for stress ratings. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied.

Note 2: Power dissipation and thermal limits must be observed.

Note 3: θ_{JA} is measured under the natural convention at T_A = 25°C on a highly effective four-layer thermal conductivity test board with thermal via.

Note 4: Guaranteed by design.

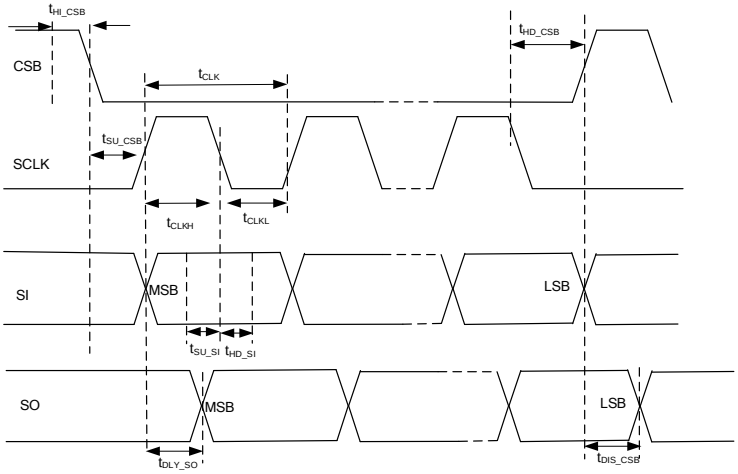
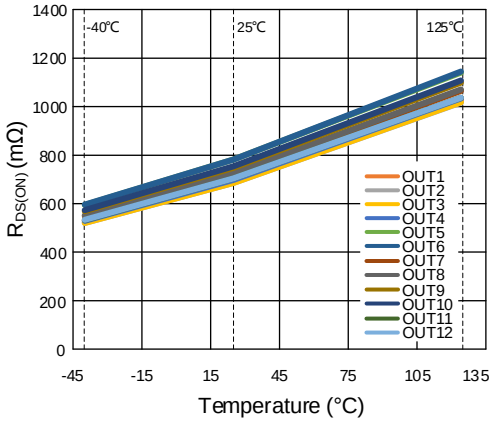


Figure 3. SPI Timing

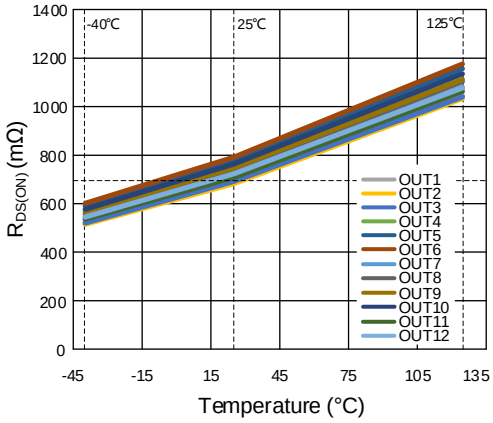
© 2023 Silergy Corp. All Rights Reserved.

Typical Performance Characteristics

High Side MOSFETs on Resistance

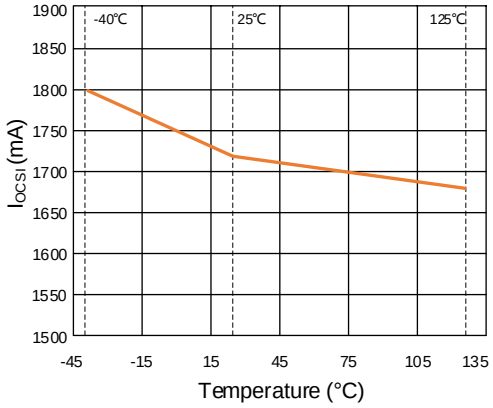


Low Side MOSFETs on Resistance



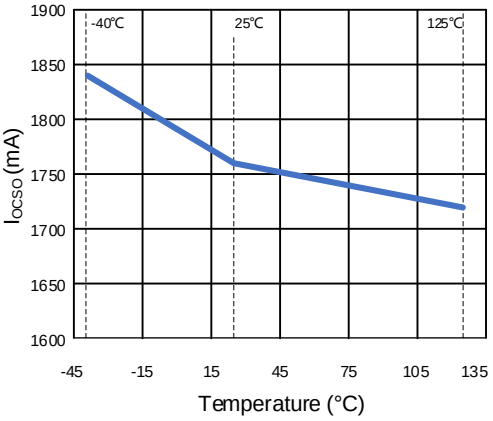
Low Side MOSFETs Over Current Limit

(VS=13.5V)



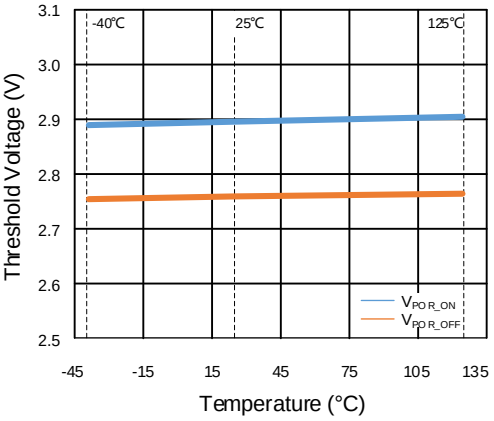
High Side MOSFETs Over Current Limit

(VS=13.5V)



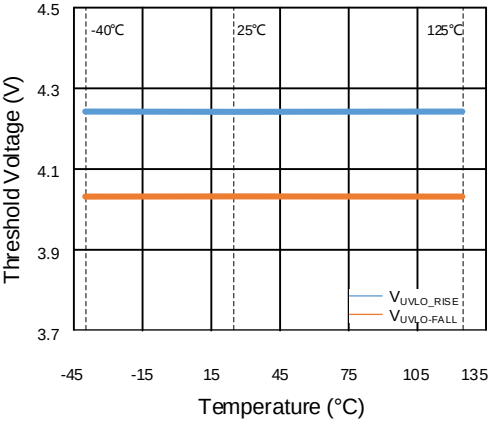
VDD Power On Reset and Power Off Reset

(VS=13.5V)

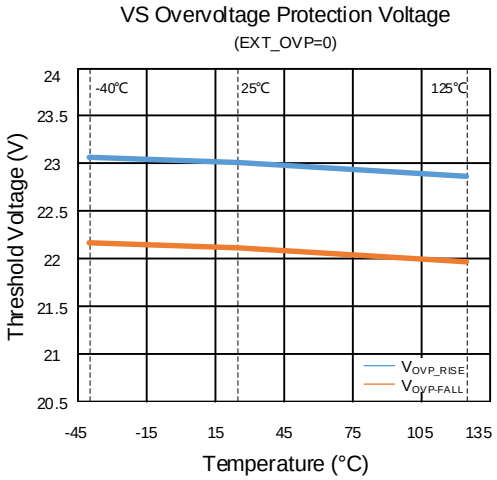


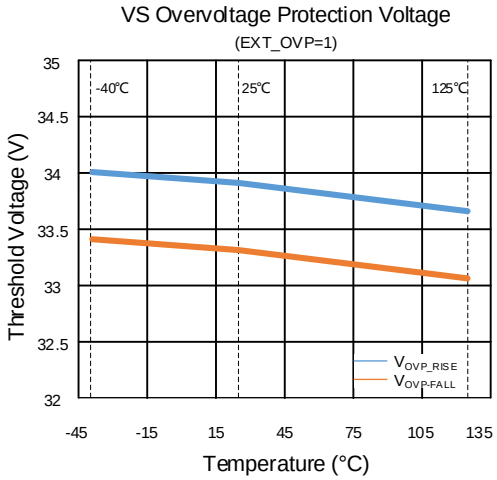
VS Undervoltage Lockout Voltage

(VDD=5V)



© 2023 Silergy Corp. All Rights Reserved.

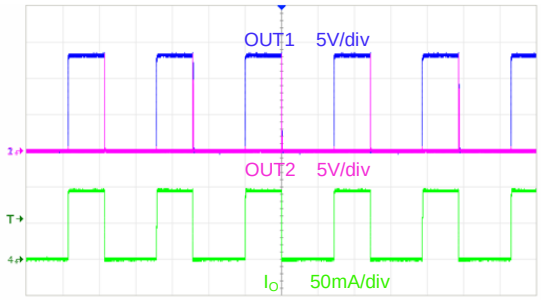




© 2023 Silergy Corp. All Rights Reserved.

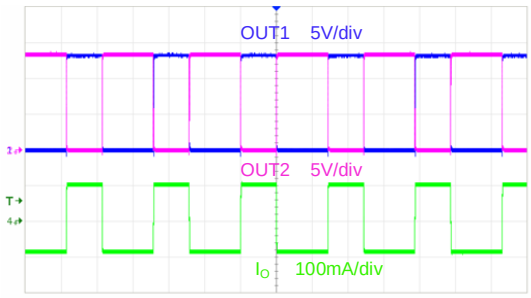
Normal Operation Waveforms

Passive Free-wheeling
(VS=13.5V Io=100mA Duty=25% Frequency=80Hz)



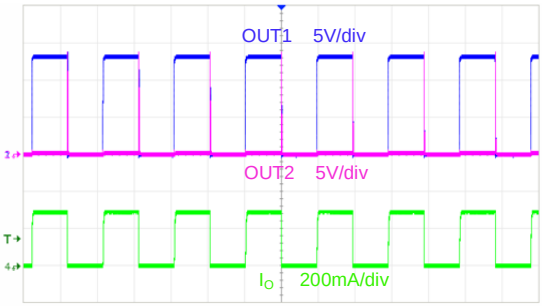
Time (5ms/div)

Active Free-wheeling
(VS=13.5V Io=100mA Duty=25% Frequency=80Hz)



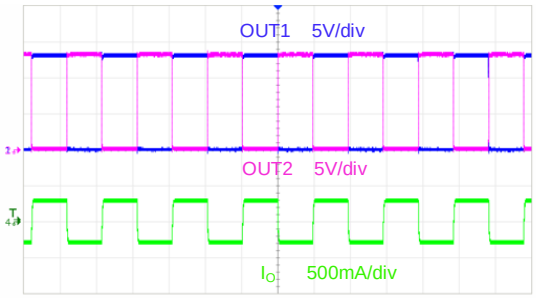
Time (5ms/div)

Passive Free-wheeling
(VS=13.5V Io=300mA Duty=50% Frequency=100Hz)



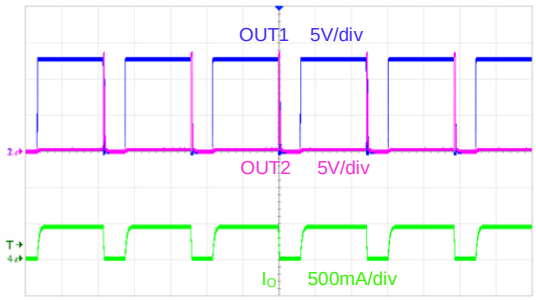
Time (5ms/div)

Active Free-wheeling
(VS=13.5V Io=300mA Duty=50% Frequency=100Hz)



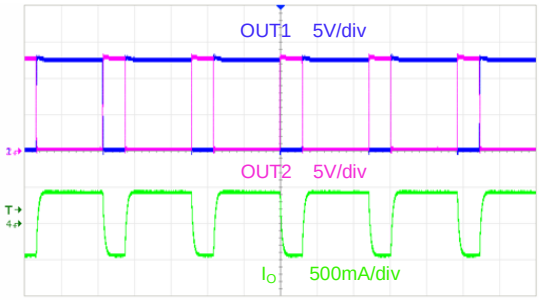
Time (5ms/div)

Passive Free-wheeling
(VS=13.5V Io=500mA Duty=75% Frequency=200Hz)



Time (2ms/div)

Active Free-wheeling
(VS=13.5V Io=500mA Duty=75% Frequency=200Hz)



Time (2ms/div)

© 2023 Silergy Corp. All Rights Reserved.

Detailed Description

The SY2A58152 is a twelve half-bridge motor driver solution for automotive, industrial, and other mechatronic applications. It can be configured as six independent H-bridges. The half-bridges are designed to support 1A per half-bridge.

The device supports a standard 16-bit, 5MHz serial peripheral interface (SPI). The device also features daisy-chain functionality, enabling the connection of multiple devices using a single CSB line.

Power Supply

VS supplies power to the MOSFETs, while VDD powers the logic circuits. Once VS is powered up, it permits the activation of the drivers. Initially, all drivers are set to an off condition and maintain this state regardless of the VDD status. Powering up VDD results in a reset of all internal logic. All internal registers are cleared upon VDD Power-On Reset (POR).

Driving Control

The device can be configured as an H-bridge, high-side or low-side driver. The half-bridge outputs of the device are designed to drive motor or LED loads. The half-bridge drivers can be programmed for continuous load driving (without PWM) or in chopping mode (with PWM). They also support parallel operation, which is ideal for driving high-current loads.

Continuous Mode (Without PWM)

The half-bridge drivers can be programmed to drive loads continuously (without PWM). The device can set the high-side enable bits (HBx_HS_EN) and low-side enable bits (HBx_LS_EN) in the SPI memory mapped control registers (OP_CTRL_1, OP_CTRL_2 and OP_CTRL_3) to switch high-side or low-side individually.

Additionally, the device will stay in Hi-Z mode if both the high-side and low-side switches of a particular half-bridge are set high. This configuration is depicted in Figures 4 and 5, which show OUT1 and OUT2 driving a DC brush motor. In this setup, the motor operates in the forward direction when the high-side FET of OUT1 and the low-side FET of OUT2 are activated, causing the motor current to flow from OUT1 to OUT2. Conversely, activating the high-side FET of OUT2 and the low-side FET of OUT1 will reverse the motor's direction, resulting in the motor current flowing from OUT2 to OUT1.

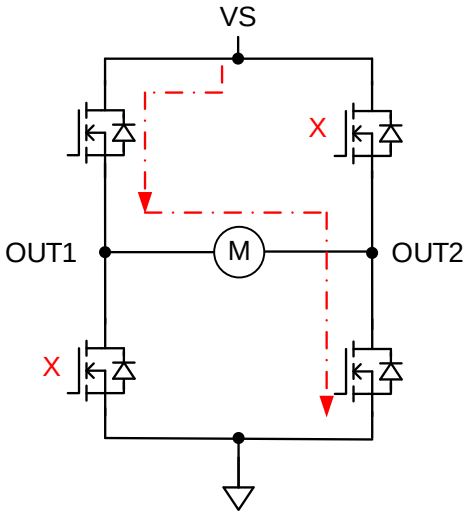


Figure 4. Continuous Mode (Forward)

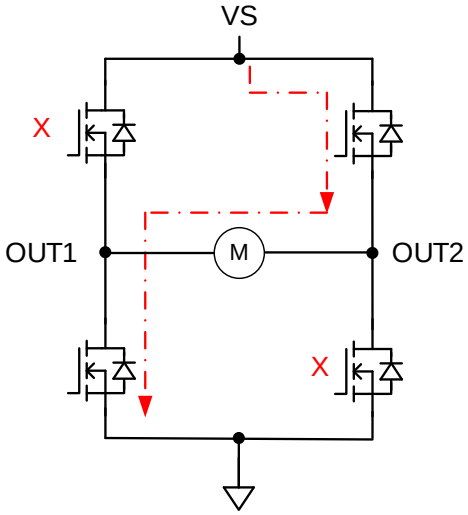


Figure 5. Continuous Mode (Reverse)

If the motor initially operates in either the forward or reverse direction, and then both the high-side and low-side are switched off, the H-bridge will enter coast mode. Due to the inductive energy, current will continue to flow in the motor, taking a path through the body diodes of the MOSFETs, as illustrated in Figures 6 and 7.

© 2023 Silergy Corp. All Rights Reserved.

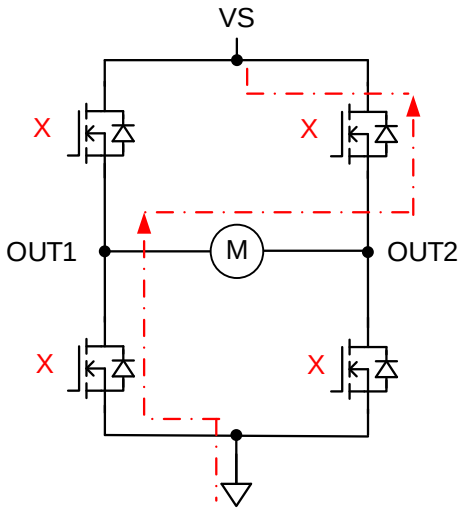


Figure 6. Coast-From Forward

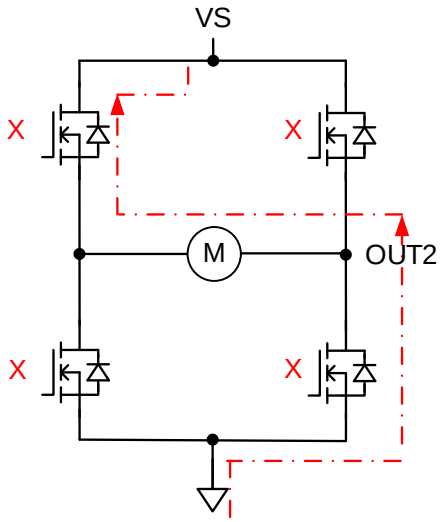


Figure 7. Coast-From Reverse

If the motor initially operates in either the forward or reverse direction, and then either the high-side or low-side is switched on, the H-bridge will operate in brake mode. In the case of low-side braking, both low-side MOSFETs of the driver are turned on. Similarly, for high-side braking, both high-side MOSFETs are turned on. These configurations are illustrated in Figures 8 and 9.

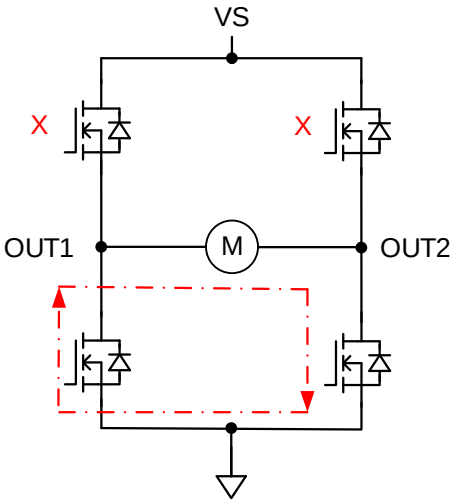


Figure 8. Brake-Low-Side

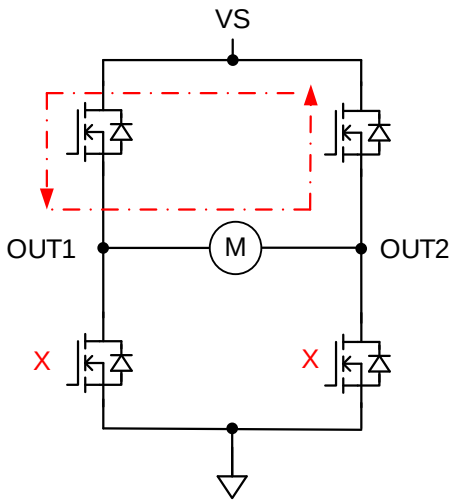


Figure 9. Brake-High-Side

Each half-bridge of the device can be configured for PWM mode, making it suitable for driving inductive loads such as DC brush motors. The device features four distinct PWM channels, each with its own duty cycle settings using an 8-bit resolution. It offers four selectable PWM frequencies — 80Hz, 100Hz, 200Hz, and 2kHz — for various application requirements.

The PWM chopping mode operation is carried out through the following steps:

1. PWM Configuration

The half-bridge can be configured into continuous or chopping mode (PWM mode) through the PWM control register (PWM_CTRL_1 and PWM_CTRL_2). The HBx_PWM bit must be set to 1 to enable PWM switching mode. If not set, the half-bridge will operate in continuous mode. Additionally, setting the PWM_CHx_DIS bit in the PWM control register (PWM_CTRL_2) activates the PWM generator.

© 2023 Silergy Corp. All Rights Reserved.

2. Free-Wheeling Mode (Synchronous Rectification) Disable/Enable

The device allows the selection of the synchronous rectification mode by setting the HBx_FW bit in the free-wheeling control registers (FW_CTRL_1 and FW_CTRL_2). As illustrated in Figure 10, when the HBx_FW is disabled, the current will flow through the high-side diode during the PWM off time. Conversely, enabling the HBx_FW bit allows for the opening of the MOSFET to create an alternative current path. Figure 11 provides an example of synchronous rectification, demonstrating how the high-side MOSFET of the OUT2 half-bridge is turned on while the low-side MOSFET of the same half-bridge is turned off during a PWM cycle.

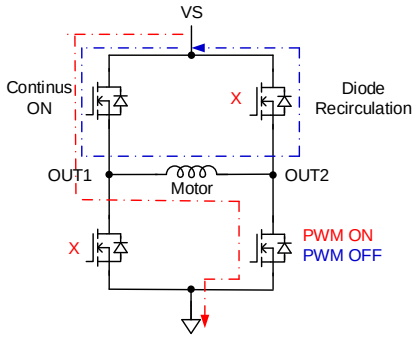


Figure 10. PWM Mode (Synchronous Rectification =OFF)

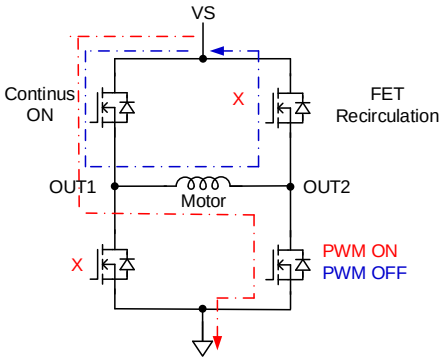


Figure 11. PWM Mode (Synchronous Rectification =ON)

3. PWM Channels Mapping

By configuring the PWM map control registers (PWM_MAP_CTRL_x), any OUTx half-bridge outputs can be mapped to any of the four available PWM generators. The HBx_PWM_MAP bits are used to map any of these twelve channels, as detailed in Table 1.

Table 1. PWM Mapping

HBx_PWM MAP BITS	PWM CHANNEL
HBx_PWM_MAP=00b	Channel 1 selected for OUTx
HBx_PWM_MAP=01b	Channel 2 selected for OUTx
HBx_PWM_MAP=10b	Channel 3 selected for OUTx
HBx_PWM_MAP=11b	Channel 4 selected for OUTx

4. PWM Channels Configuration (PWM Frequency and PWM Duty)

Each PWM generator can be independently configured with different frequency and duty-cycle. The PWM frequency for each channel is determined by the PWM frequency control register (PWM_FREQ_CTRL), as shown in Table 2. The PWM duty cycle is managed using the PWM_DUTY_CHx bit in the PWM control register (PWM_DUTY_CTRL_x), as shown in Table 3.

Table 2. PWM Frequency

PWM_CHx_FREQ BITS	PWM FREQUENCY
PWM_CHx_FREQ=00b	80Hz
PWM_CHx_FREQ =01b	100Hz

© 2023 Silergy Corp. All Rights Reserved.

PWM_CHx_FREQ =10b	200Hz
PWM_CHx_FREQ =11b	2000Hz

Table 3. PWM Duty Control Channelx Register Field Descriptions

Bit	Field	Type	Default	Description
7-0	PWM_DUTY_CHx	R/W	00000000b	00000000b = 0 % PWM Duty 11111111b = 100 % PWM Duty Calculate duty as decimal (xxxxxxxxb) × 1/255

5. Half-Bridge Enable

Following the initial four configuration steps, the final step involves enabling either the high-side or low-side MOSFETs. Once the half-bridge is configured for PWM generation, activation is achieved by enabling one of these switches. Specifically, the HBx_HS_EN bit in the operation control registers (OP_CTRL_1, OP_CTRL_2, OP_CTRL_3) is used to enable the high-side, while the HBx_LS_EN bit enables the low-side.

Protection Circuits

This device has embedded protection functions such as undervoltage, overvoltage, overcurrent, power-on reset, open load, and thermal shutdown.

Undervoltage Lockout (UVLO)

When the voltage VS drops below the switch-off voltage threshold, V_{UVLO_FALL}, all output stages are switched off. However, the configuration information remains intact and uncorrupted. The VS undervoltage error bit is also latched high in the device status register (IC_START), and the nFAULT pin is driven low. If VS rises again and reaches the switch on the voltage V_{UVLO_RISE} threshold, the power stages will be reactivated, and the nFAULT pin will be set to high-impedance. The UVLO error bit remains set until it is manually cleared through the CLR_FLT bit.

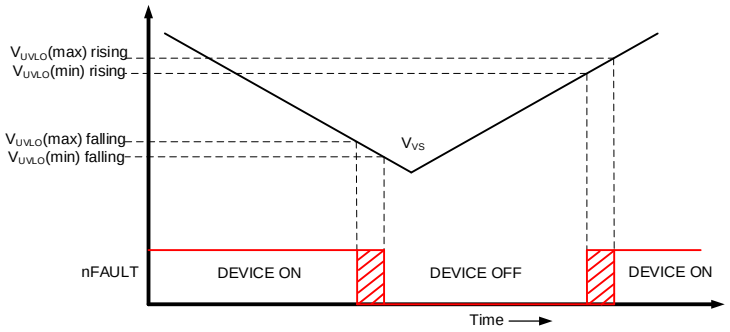


Figure 12. VS UVLO Operation

Overvoltage Protection (OVP)

If the supply voltage VS exceeds the overvoltage voltage threshold, V_{OVP}, all output stages are automatically deactivated. Simultaneously, the VS overvoltage error bit is latched high in the device status register (IC_START), and the nFAULT pin is driven low. If VS falls below the threshold (V_{OVP} -V_{OVP_HYS}), the power stages are enabled, and the nFAULT pin is set to high-impedance. The OVP error bit, however, remains set until cleared using a SPI command through the CLR_FLT bit. Additionally, the device supports an extended overvoltage operation, supporting a higher overvoltage range of up to 33V, by enabling the EXT_OVP bit in the configuration register (CONFIG_CTRL).

© 2023 Silergy Corp. All Rights Reserved.

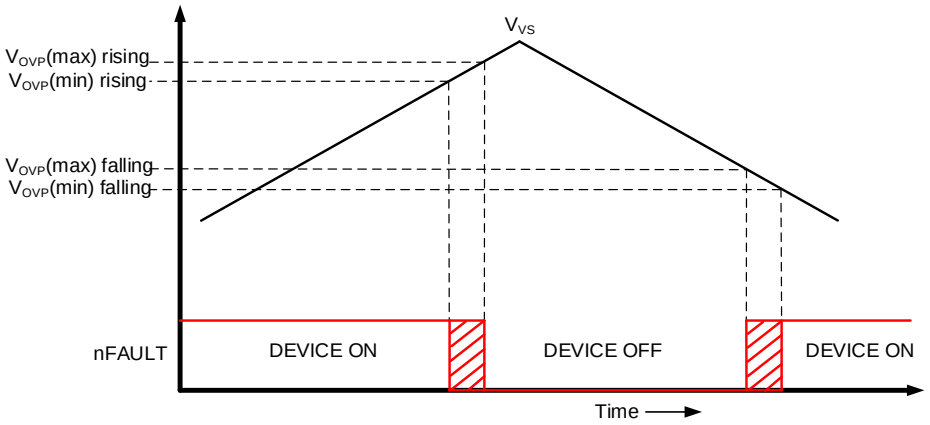


Figure 13. VS OVP Operation

VDD Power-On Reset (POR)

In the event that the VDD logic supply falls below the undervoltage threshold, V_{POR_FALL}, the SPI interfaces will become non-functional, and the device will enter reset mode. The digital block will be initialized, and the output stages will be switched off to high impedance. The undervoltage reset mode is released once the VDD voltage levels rise above the V_{POR_ON} voltage threshold. This reset event is reported in the CONFIG_CTRL register by resetting the NPOR bit. The NPOR error bit remains latched low until it is cleared through the CLR_FLT bit.

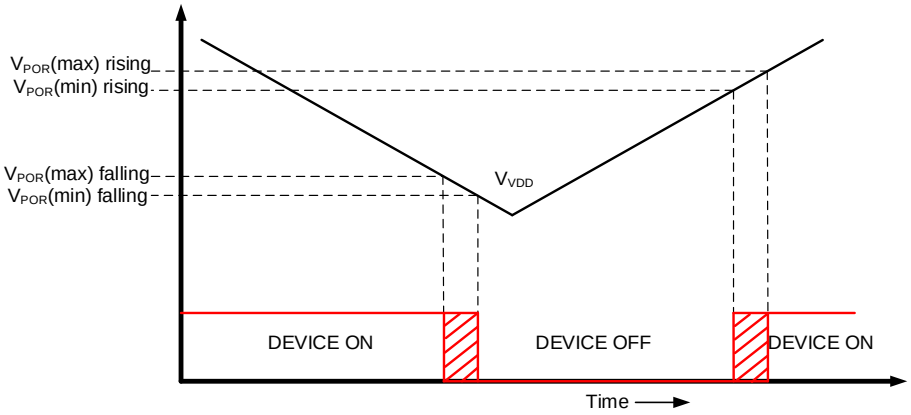


Figure 14. VDD UVLO Operation

Overcurrent Protection (OCP)

The device features overcurrent protection, actively monitoring the current in both the high-side and low-side drivers. If the current exceeds the overcurrent shutdown detection threshold, the affected HS or LS driver is immediately latched off. Simultaneously, the corresponding error bit — either HBx_HS_OCP or HBx_LS_OCP — is set and latched after the specified shutdown time, t_{OC}. To restore normal functionality of the power switch after an overcurrent condition has been resolved, or to check if the fault persists, users can disable the OCP fault indication on the nFAULT pin by activating the OCP_REP bit in the CONFIG_CTRL register.

© 2023 Silergy Corp. All Rights Reserved.

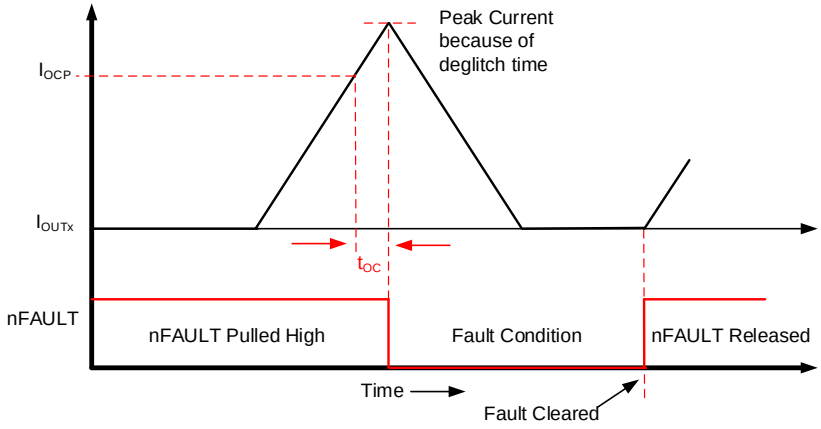


Figure 15. Over Current Protection

Open Load Detection (OLD)

The open-load detection (OLD) function ensures the proper load connection. The device supports active OLD and low-current OLD:

- **Active OLD**

Active OLD can identify an open-load condition on the OUTx pins during load operation. As depicted in Figure 16, if the motor current (I_{OUTx}) falls below the open-load current threshold (IOLD) and the fault condition persists for longer than the open-load deglitch time (t_{OLD}), the device will recognize this as an active open-load fault. Under such circumstances, the nFAULT pin will be driven low. Once the open-load condition is resolved and the CLR_FLT bit is set to 1, the nFAULT pin is released.

Additionally, the controller can determine the presence of an open-load condition by reading the device registers. The OLD bit in the device status register (IC_STAT) and either the HBx_HS_OLD or HBx_LS_OLD bit in the open-load status register (OLD_STAT_x) will be set to 1 to indicate an open-load fault.

Two OLD control registers (OLD_CTRL_1 and OLD_CTRL_2) are used to configure the OLD function. The HBx_OLD_DIS bit in the OLD_CTRL_1 register allows users to disable OLD on the OUTx pins, although OLD is enabled by default on the device. The OLD_REP bit in the OLD_CTRL_2 register determines whether the fault is reported on the nFAULT pin. The OLD_OP bit sets the device's response to an active OLD fault: if OLD_OP = 0, the OUTx pins switch to the Hi-Z state, stopping the output drive. Otherwise, the OUTx pins maintain their previous state and do not respond to the OLD fault.

- **Low-Current OLD**

The device also incorporates a low-current OLD mode, which operates similarly to the active open-load detection. The primary distinction between the low-current open-load and the active open-load lies in the current detection threshold, which is approximately 10 times lower in the low-current open-load mode. Furthermore, this mode is functional only with the low-side MOSFET. Activating the low-current OLD mode simultaneously deactivates the high-side OLD for the respective half-bridge.

As illustrated in Figure 17, if the motor current (I_{OUTx}) drops below the low-current open-load threshold (I_{OLD_LOW}) and the fault condition persists longer than the open-load deglitch time (t_{OLD}), the device will identify a low-current open-load fault. In this event, the nFAULT pin will be driven low. The fault condition can be cleared, and the nFAULT pin released, by resolving the open-load condition and setting the CLR_FLT bit to 1.

Additionally, the host controller can read the register to know whether there is an open-load condition. The OLD bit in the device status register (IC_STAT) and the HBx_LS_OLD bit in the open-load status register (OLD_STAT_x) will be set to 1 to indicate a low-current open-load fault.

© 2023 Silergy Corp. All Rights Reserved.

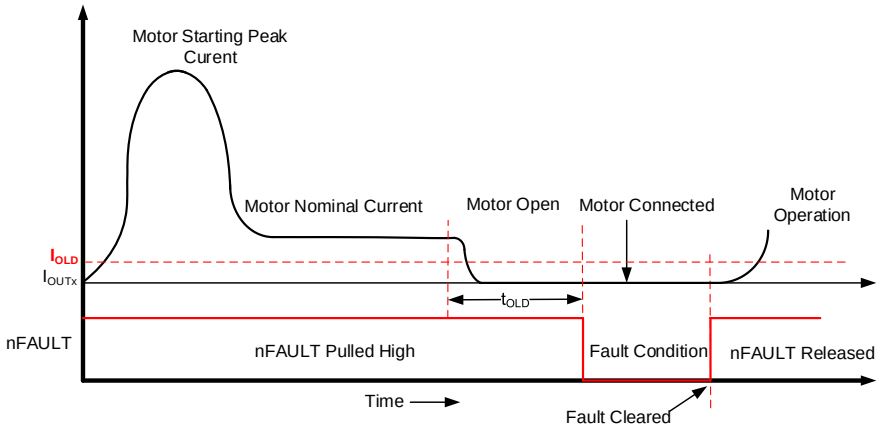


Figure 16. Active Open-Load Detection

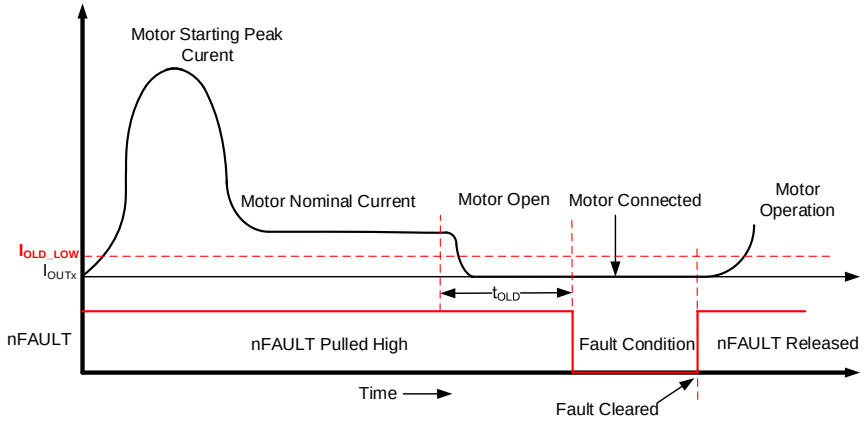


Figure 17. Low-Current OLD

Thermal Warning (OTW)

The device offers overtemperature warning and shutdown protection. If one or more temperature sensors reach the warning temperature, the temperature pre-warning bit, OTW, is set in the device status (IC_START) register. This bit is latched and can only be cleared through the SPI, but the output stages remain activated. The reporting of OTW on the nFAULT pin can be enabled by setting the overtemperature warning reporting (OTW_REP) bit in the configuration control (CONFIG_CTRL) register. The nFAULT pin releases when the die temperature decreases below the hysteresis point of the thermal warning (T_{WARN_HYS}).

Thermal Shutdown (TSD)

If one or more temperature sensors reach the shut-down temperature threshold, all outputs are latched off, and the nFAULT pin is driven low. The OTSD bit is set in the device status (IC_START) register. All outputs will be activated, and the nFAULT pin is released when the die temperature decreases below the hysteresis point of the thermal warning (T_{HYS}). The OTSD bit remains latched high, indicating that a thermal event occurred until a clear fault command is issued through the CLR_FLT bit. This protection feature cannot be disabled.

Programming Configuration

The device can be controlled using a standard 16-bit SPI interface, with data communication initiated by clocking in the Most Significant Bit (MSB) first. The SPI interface operates as a synchronous serial interface, allowing for address and data transfer at bit rates up to 5MHz. It is configured for 8-bit byte transfers, making it compatible with a standard SPI bus. Communication over the SPI utilizes four pins: SCLK (synchronous clock), CSB (chip select, active low), SI (data input to the device for write operations), and SO (data output from the device for read operations), as depicted in Figure 18.

© 2023 Silergy Corp. All Rights Reserved.

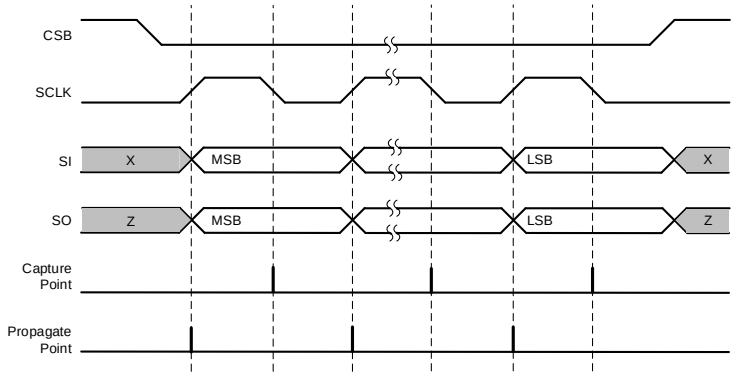


Figure 18. SPI Data Frame

A valid frame on the SPI interface must adhere to the following conditions:

1. When the CSB pin is set to high, the device disregards any signals on the SCLK and SI pins, and the SO pin enters a high impedance (Hi-Z) state.
2. Data is captured on the falling edge of SCLK, and data is propagated on the rising edge of SCLK.
3. The most significant bit (MSB) is always shifted in and out first.
4. A complete transaction requires a full sequence of 16 SCLK cycles.
5. The data word transmitted to the SI pin must consist of exactly 16 bits — neither less nor more.
6. For write commands, the current data in the register being written to is shifted out on the SO pin, following the 8-bit command data.

SPI Format

Each SPI communication sequence with the device initiates with an address byte, followed by a data byte. The device's SPI functionality includes 1 Read/Write (R/W) bit at bit position 14; 6 address bits, and 8 data bits. The control registers are READ/WRITE registers. To set the control register to READ, bit 14 in the address byte must be set to '1'; otherwise, set it to '0' for WRITE. As the microcontroller transmits the address byte via the SI pin, the device Status Register data is simultaneously shifted out through the SO pin. The subsequent data byte, comprising of bits 7 to 0, is used to configure the half-bridges or retrieve the device's status information. The mapping of the SPI Registers is shown in Table 6.

Table 4. SI Input Data Word Format

		R/W	Address						Data							
Bit	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
Data	0	W0	A5	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0

Table 5. SO Output Data Word Format

			Address						Data							
Bit	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
Data	1	1	OTSD	OLD	OCP	UVLO	OVP	NPOR	D7	D6	D5	D4	D3	D2	D1	D0

Daisy Chain

The device is designed to support daisy chain operation with other devices that utilize the same SPI protocol, as demonstrated in Figure 20. In this setup, the controller's output (MO) is connected to the serial input (SI) of the first peripheral device. The serial output (SO) of this device is then connected to the SI of the next peripheral, forming a chain. The SO of the last peripheral in the chain is linked to the controller's input (MI), completing the SPI communication loop.

In a daisy chain configuration, a single chip select (CSB) and a clock signal (SCLK) are distributed in parallel across all peripheral devices. These connections enable the microcontroller to control and access the SPI devices efficiently. Figure 19 illustrates the topology and corresponding waveforms when three devices are interconnected in a series configuration.

© 2023 Silergy Corp. All Rights Reserved.

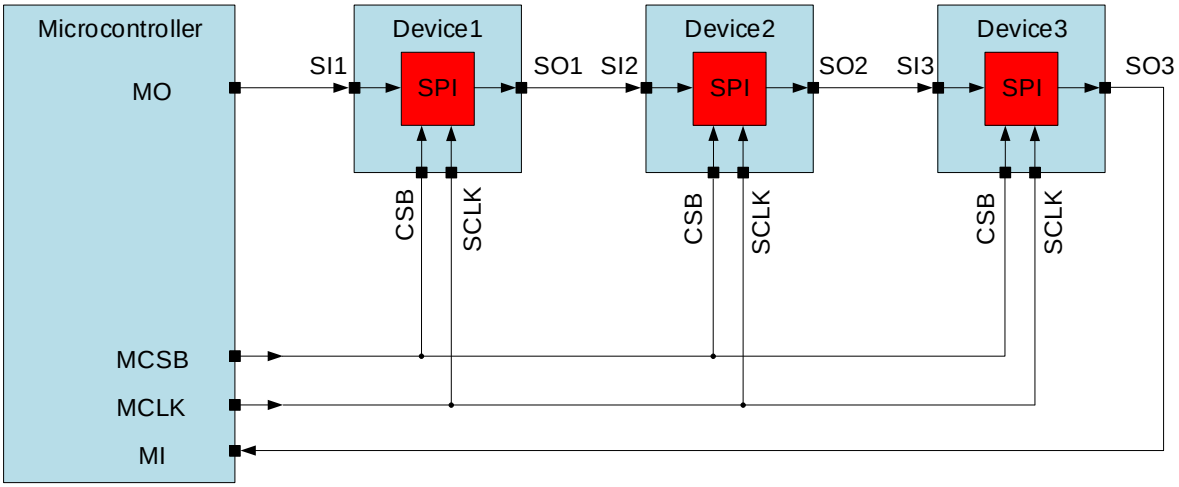


Figure 19. SPI Daisy Chain

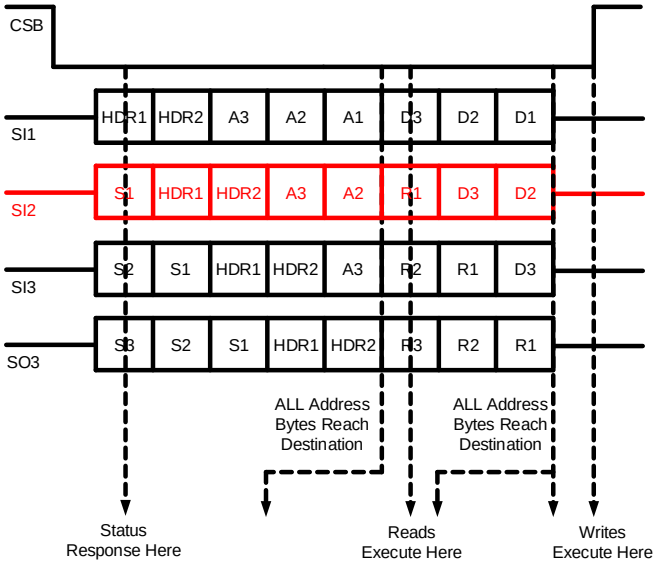


Figure 20. Daisy Chain SPI Operation

In the daisy chain configuration depicted above, the first device in the chain receives data from the controller in the following format, as shown in SI1 of Figure 20:

1) 2 bytes of Header
2) 3 bytes of Address
3) 3 bytes of Data

Once the data has been transmitted through the chain, the controller receives it back in the format illustrated in SO3 of Figure 20:

1) 3 bytes of Status
2) 2 bytes of Header (which should be identical to the information sent by the controller)
3) 3 bytes of Report

The two Header bytes carry critical information, including the number of devices in the chain and a global clear fault command. The N5 to N0 bits in Header1 indicate that up to 63 (2^6-1) devices can be connected in series per daisy chain connection. The CLR bit in Header2 is a global clear fault command that resets the fault registers of all devices in the chain. Both Header bytes must start with 1 and 0.

© 2023 Silergy Corp. All Rights Reserved.

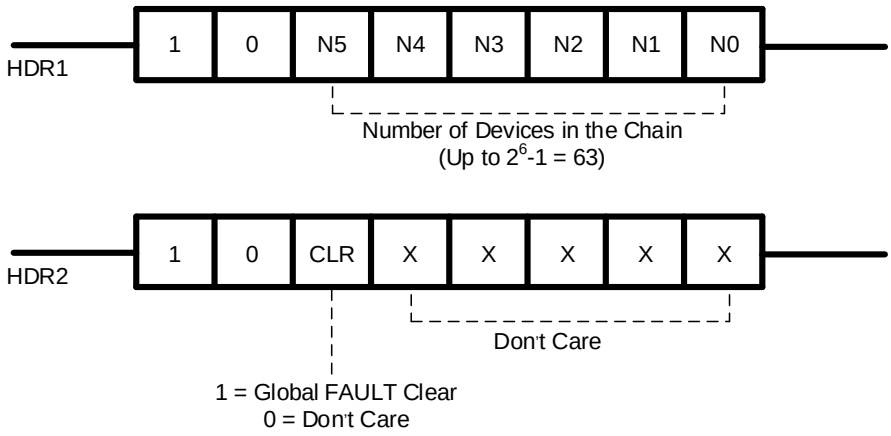


Figure 21. Header Bits

All devices in the configuration will relay their fault status through the status byte, as depicted in Figure 22. This feature allows for convenient and efficient controller fault status monitoring, enhancing the device's overall functionality.

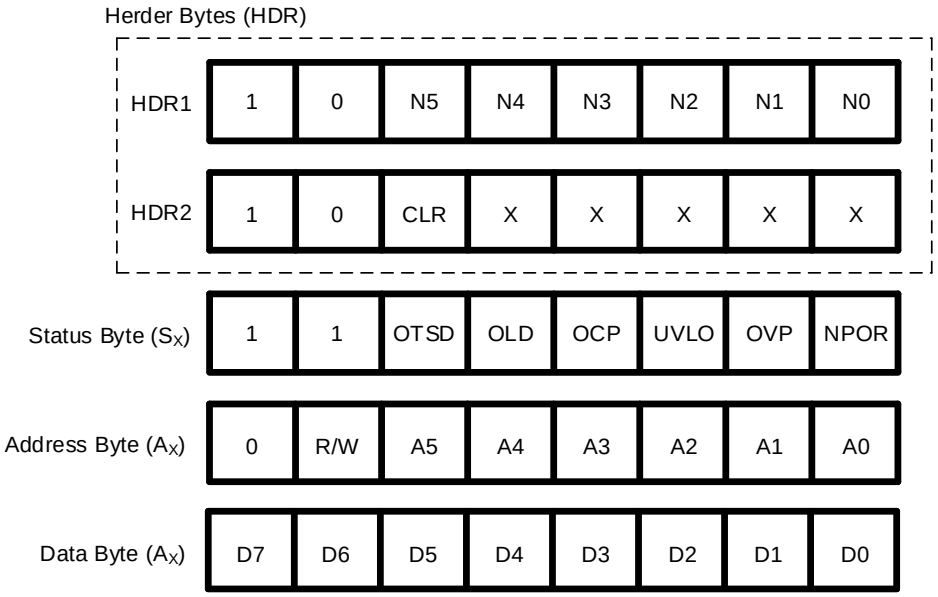


Figure 22. Daisy Chain Read Registers

The device is capable of determining its position in the chain by counting the number of Status bytes that follow the Header byte. As illustrated in Figure 20, Device 2 identifies its position by recognizing one Status byte (S1) following the Header, while Device 3 identifies two Status bytes (S1, S2) behind the Header. When the device determines the position and the total number of devices connected in the chain, each device can load the relevant address and data bytes into its buffer, effectively bypassing irrelevant bits. This method ensures efficient operation, even in a chain comprising up to 63 devices.

© 2023 Silergy Corp. All Rights Reserved.

Table 6. SY2A58152 Register Map

Name	7	6	5	4	3	2	1	0	Type	Address
IC_STAT	Reserved	OTSD	OTW	OLD	OCP	UVLO	OVP	NPOR	R	00h
OCP_STAT_1	HB4_HS_OCP	HB4_LS_OCP	HB3_HS_OCP	HB3_LS_OCP	HB2_HS_OCP	HB2_LS_OCP	HB1_HS_OCP	HB1_LS_OCP	R	01h
OCP_STAT_2	HB8_HS_OCP	HB8_LS_OCP	HB7_HS_OCP	HB7_LS_OCP	HB6_HS_OCP	HB6_LS_OCP	HB5_HS_OCP	HB5_LS_OCP	R	02h
OCP_STAT_3	HB12_HS_OCP	HB12_LS_OCP	HB11_HS_OCP	HB11_LS_OCP	HB10_HS_OCP	HB10_LS_OCP	HB9_HS_OCP	HB9_LS_OCP	R	03h
OLD_STAT_1	HB4_HS_OLD	HB4_LS_OLD	HB3_HS_OLD	HB3_LS_OLD	HB2_HS_OLD	HB2_LS_OLD	HB1_HS_OLD	HB1_LS_OLD	R	04h
OLD_STAT_2	HB8_HS_OLD	HB8_LS_OLD	HB7_HS_OLD	HB7_LS_OLD	HB6_HS_OLD	HB6_LS_OLD	HB5_HS_OLD	HB5_LS_OLD	R	05h
OLD_STAT_3	HB12_HS_OLD	HB12_LS_OLD	HB11_HS_OLD	HB11_LS_OLD	HB10_HS_OLD	HB10_LS_OLD	HB9_HS_OLD	HB9_LS_OLD	R	06h
CONFIG_CTRL	Reserved				OCP_REP		EXT_OVP	CLR_FLT	RW	07h
OP_CTRL_1	HB4_HS_EN	HB4_LS_EN	HB3_HS_EN	HB3_LS_EN	HB2_HS_EN	HB2_LS_EN	HB1_HS_EN	HB1_LS_EN	RW	08h
OP_CTRL_2	HB8_HS_EN	HB8_LS_EN	HB7_HS_EN	HB7_LS_EN	HB6_HS_EN	HB6_LS_EN	HB5_HS_EN	HB5_LS_EN	RW	09h
OP_CTRL_3	HB12_HS_EN	HB12_LS_EN	HB11_HS_EN	HB11_LS_EN	HB10_HS_EN	HB10_LS_EN	HB9_HS_EN	HB9_LS_EN	RW	0Ah
PWM_CTRL_1	HB8_PWM	HB7_PWM	HB6_PWM	HB5_PWM	HB4_PWM	HB3_PWM	HB2_PWM	HB1_PWM	RW	0Bh
PWM_CTRL_2	PWM_CH4_DIS	PWM_CH3_DIS	PWM_CH2_DIS	PWM_CH1_DIS	HB12_PWM	HB11_PWM	HB10_PWM	HB9_PWM	RW	0Ch
FW_CTRL_1	HB8_FW	HB7_FW	HB6_FW	HB5_FW	HB4_FW	HB3_FW	HB2_FW	HB1_FW	RW	0Dh
FW_CTRL_2	Reserved				HB12_FW	HB11_FW	HB10_FW	HB9_FW	RW	0Eh
PWM_MAP_CTRL_1	HB4_PWM_MAP		HB3_PWM_MAP		HB2_PWM_MAP		HB1_PWM_MAP		RW	0Fh
PWM_MAP_CTRL_2	HB8_PWM_MAP		HB7_PWM_MAP		HB6_PWM_MAP		HB5_PWM_MAP		RW	10h
PWM_MAP_CTRL_3	HB12_PWM_MAP		HB11_PWM_MAP		HB10_PWM_MAP		HB9_PWM_MAP		RW	11h
PWM_FREQ_CTRL	PWM_CH4_FREQ		PWM_CH3_FREQ		PWM_CH2_FREQ		PWM_CH1_FREQ		RW	12h
PWM_DUTY_CTRL_1	PWM_DUTY_CH1								RW	13h
PWM_DUTY_CTRL_2	PWM_DUTY_CH2								RW	14h
PWM_DUTY_CTRL_3	PWM_DUTY_CH3								RW	15h
PWM_DUTY_CTRL_4	PWM_DUTY_CH4								RW	16h
SR_CTRL_1	HB8_SR	HB7_SR	HB6_SR	HB5_SR	HB4_SR	HB3_SR	HB2_SR	HB1_SR	RW	17h
SR_CTRL_2	Reserved				HB12_SR	HB11_SR	HB10_SR	HB9_SR	RW	18h
OLD_CTRL_1	HB8_OLD_DIS	HB7_OLD_DIS	HB6_OLD_DIS	HB5_OLD_DIS	HB4_OLD_DIS	HB3_OLD_DIS	HB2_OLD_DIS	HB1_OLD_DIS	RW	19h
OLD_CTRL_2	OLD_REP	OLD_OP	Reserved		HB12_OLD_DIS	HB11_OLD_DIS	HB10_OLD_DIS	HB9_OLD_DIS	RW	1Ah
OLD_CTRL_3	OCP_DEG			Reserved	HB12_LOLD_EN	HB11_LOLD_EN	HB10_LOLD_EN	HB9_LOLD_EN	RW	1Bh
OLD_CTRL_4	HB8_LOLD_EN	HB7_LOLD_EN	HB6_LOLD_EN	HB5_LOLD_EN	HB4_LOLD_EN	HB3_LOLD_EN	HB2_LOLD_EN	HB1_LOLD_EN	RW	24h

© 2023 Silergy Corp. All Rights Reserved.

SPI Status Registers

The Status Register is used to report warning and fault conditions. The status registers are read-only.

IC_STAT

IC_Status Register (Address =0x00) [reset =0x00]

D7	D6	D5	D4	D3	D2	D1	D0
Reserved	OTSD	OTW	OLD	OCP	UVLO	OVP	NPOR
r	r	r	r	r	r	r	r

Field	Bits	Type	Description
Reserved	D7	r	Reserved. Always reads as '0'
OTSD	D6	r	Temperature shutdown error detection 0_B Junction temperature below temperature shutdown threshold 1_B Junction temperature has reached the temperature shutdown threshold
OTW	D5	r	Temperature pre-warning error detection 0_B Junction temperature below temperature pre-warning threshold 1_B Junction temperature has reached the temperature pre-warning threshold.
OLD	D4	r	Open Load error detection 0_B No Open Load 1_B Open load
OCP	D3	r	Over current error detection 0_B No Over current 1_B Over current
UVLO	D2	r	VS Undervoltage error detection 0_B No undervoltage on VS detected 1_B Undervoltage on VS detected
OVP	D1	r	VS Overvoltage error detection 0_B No overvoltage on VS detected 1_B Overvoltage on VS detected
NPOR	D0	r	Not Power on Reset (NPOR) detection 0_B POR on EN or VDD supply rail 1_B No POR

OCP_STAT_1

Overcurrent Error Status of Half-bridge Outputs 1-4 (Address =0x01) [reset =0x00]

D7	D6	D5	D4	D3	D2	D1	D0
HB4_HS_OC	HB4_LS_OC	HB3_HS_OC	HB3_LS_OC	HB2_HS_OC	HB2_LS_OC	HB1_HS_OC	HB1_LS_OC
r	r	r	r	r	r	r	r

Field	Bits	Type	Description
HB4_HS_OC	D7	r	High-side (HS) switch of half-bridge 4 overcurrent detection 0_B No error on HS4 switch 1_B Overcurrent detected on HS4 switch
HB4_LS_OC	D6	r	Low-side (LS) switch of half-bridge 4 overcurrent detection 0_B No error on LS4 switch 1_B Overcurrent detected on LS4 switch
HB3_HS_OC	D5	r	High-side (HS) switch of half-bridge 3 overcurrent detection 0_B No error on HS3 switch 1_B Overcurrent detected on HS3 switch
HB3_LS_OC	D4	r	Low-side (LS) switch of half-bridge 3 overcurrent detection 0_B No error on LS3 switch 1_B Overcurrent detected on LS3 switch
HB2_HS_OC	D3	r	High-side (HS) switch of half-bridge 2 overcurrent detection 0_B No error on HS2 switch 1_B Overcurrent detected on HS2 switch
HB2_LS_OC	D2	r	Low-side (LS) switch of half-bridge 2 overcurrent detection 0_B No error on LS2 switch 1_B Overcurrent detected on LS2 switch
HB1_HS_OC	D1	r	High-side (HS) switch of half-bridge 1 overcurrent detection 0_B No error on HS1 switch 1_B Overcurrent detected on HS1 switch

© 2023 Silergy Corp. All Rights Reserved.

HB1_LS_OC	D0	r	Low-side (LS) switch of half-bridge 1 overcurrent detection 0_B No error on LS1 switch 1_B Overcurrent detected on LS1 switch

OCP_STAT_2

Overcurrent Error Status of Half-bridge Outputs 5-8 (Address =0x02) [reset =0x00]

D7	D6	D5	D4	D3	D2	D1	D0
HB8_HS_OC	HB8_LS_OC	HB7_HS_OC	HB7_LS_OC	HB6_HS_OC	HB6_LS_OC	HB5_HS_OC	HB5_LS_OC
r	r	r	r	r	r	r	r

Field	Bits	Type	Description
HB8_HS_OC	D7	r	High-side (HS) switch of half-bridge 8 overcurrent detection 0_B No error on HS8 switch 1_B Overcurrent detected on HS8 switch
HB8_LS_OC	D6	r	Low-side (LS) switch of half-bridge 8 overcurrent detection 0_B No error on LS8 switch 1_B Overcurrent detected on LS8 switch
HB7_HS_OC	D5	r	High-side (HS) switch of half-bridge 7 overcurrent detection 0_B No error on HS7 switch 1_B Overcurrent detected on HS7 switch
HB7_LS_OC	D4	r	Low-side (LS) switch of half-bridge 7 overcurrent detection 0_B No error on LS7 switch 1_B Overcurrent detected on LS7 switch
HB6_HS_OC	D3	r	High-side (HS) switch of half-bridge 6 overcurrent detection 0_B No error on HS6 switch 1_B Overcurrent detected on HS6 switch
HB6_LS_OC	D2	r	Low-side (LS) switch of half-bridge 6 overcurrent detection 0_B No error on LS6 switch 1_B Overcurrent detected on LS6 switch
HB5_HS_OC	D1	r	High-side (HS) switch of half-bridge 5 overcurrent detection 0_B No error on HS5 switch 1_B Overcurrent detected on HS5 switch
HB5_LS_OC	D0	r	Low-side (LS) switch of half-bridge 5 overcurrent detection 0_B No error on LS5 switch 1_B Overcurrent detected on LS5 switch

OCP_STAT_3

Overcurrent Error Status of Half-bridge Outputs 9-12 (Address =0x03) [reset =0x00]

D7	D6	D5	D4	D3	D2	D1	D0
HB12_HS_OC	HB12_LS_OC	HB11_HS_OC	HB11_LS_OC	HB10_HS_OC	HB10_LS_OC	HB9_HS_OC	HB9_LS_OC
r	r	r	r	r	r	r	r

Field	Bits	Type	Description
HB12_HS_OC	D7	r	High-side (HS) switch of half-bridge 12 overcurrent detection 0_B No error on HS12 switch 1_B Overcurrent detected on HS12 switch
HB12_LS_OC	D6	r	Low-side (LS) switch of half-bridge 12 overcurrent detection 0_B No error on LS12 switch 1_B Overcurrent detected on LS12 switch
HB11_HS_OC	D5	r	High-side (HS) switch of half-bridge 11 overcurrent detection 0_B No error on HS11 switch 1_B Overcurrent detected on HS11 switch
HB11_LS_OC	D4	r	Low-side (LS) switch of half-bridge 11 overcurrent detection 0_B No error on LS11 switch 1_B Overcurrent detected on LS11 switch
HB10_HS_OC	D3	r	High-side (HS) switch of half-bridge 10 overcurrent detection 0_B No error on HS10 switch 1_B Overcurrent detected on HS10 switch
HB10_LS_OC	D2	r	Low-side (LS) switch of half-bridge 10 overcurrent detection 0_B No error on LS10 switch

© 2023 Silergy Corp. All Rights Reserved.

			1_B Overcurrent detected on LS10 switch
HB9_HS_OC	D1	r	High-side (HS) switch of half-bridge 9 overcurrent detection 0_B No error on HS9 switch 1_B Overcurrent detected on HS9 switch
HB9_LS_OC	D0	r	Low-side (LS) switch of half-bridge 9 overcurrent detection 0_B No error on LS9 switch 1_B Overcurrent detected on LS9 switch

OLD_STAT_1

Open Load Error Status of Half-bridge Outputs 1-4 (Address =0x04) [reset =0x00]

D7	D6	D5	D4	D3	D2	D1	D0
HB4_HS_OL	HB4_LS_OL	HB3_HS_OL	HB3_LS_OL	HB2_HS_OL	HB2_LS_OL	HB1_HS_OL	HB1_LS_OL
r	r	r	r	r	r	r	r

Field	Bits	Type	Description
HB4_HS_OL	D7	r	High-side (HS) switch of half-bridge 4 open load detection 0_B No error on HS4 switch (default value) 1_B Open load detected on HS4 switch
HB4_LS_OL	D6	r	Low-side (LS) switch of half-bridge 4 open load detection 0_B No error on LS4 switch (default value) 1_B Open load detected on LS4 switch
HB3_HS_OL	D5	r	High-side (HS) switch of half-bridge 3 open load detection 0_B No error on HS3 switch (default value) 1_B Open load detected on HS3 switch
HB3_LS_OL	D4	r	Low-side (LS) switch of half-bridge 3 open load detection 0_B No error on LS3 switch (default value) 1_B Open load detected on LS3 switch
HB2_HS_OL	D3	r	High-side (HS) switch of half-bridge 2 open load detection 0_B No error on HS2 switch (default value) 1_B Open load detected on HS2 switch
HB2_LS_OL	D2	r	Low-side (LS) switch of half-bridge 2 open loadt detection 0_B No error on LS2 switch (default value) 1_B Open load detected on LS2 switch
HB1_HS_OL	D1	r	High-side (HS) switch of half-bridge 1 open load detection 0_B No error on HS1 switch (default value) 1_B Open load detected on HS1 switch
HB1_LS_OL	D0	r	Low-side (LS) switch of half-bridge 1 open load detection 0_B No error on LS1 switch (default value) 1_B Open load detected on LS1 switch

OLD_STAT_2

Open Load Error Status of Half-bridge Outputs 5-8 (Address =0x05) [reset =0x00]

D7	D6	D5	D4	D3	D2	D1	D0
HB8_HS_OL	HB8_LS_OL	HB7_HS_OL	HB7_LS_OL	HB6_HS_OL	HB6_LS_OL	HB5_HS_OL	HB5_LS_OL
r	r	r	r	r	r	r	r

Field	Bits	Type	Description
HB8_HS_OL	D7	r	High-side (HS) switch of half-bridge 8 open load detection 0_B No error on HS8 switch 1_B Open load detected on HS8 switch
HB8_LS_OL	D6	r	Low-side (LS) switch of half-bridge 8 open load detection 0_B No error on LS8 switch 1_B Open load detected on LS8 switch
HB7_HS_OL	D5	r	High-side (HS) switch of half-bridge 7 open load detection 0_B No error on HS7 switch 1_B Open load detected on HS7 switch
HB7_LS_OL	D4	r	Low-side (LS) switch of half-bridge 7 open load detection 0_B No error on LS7 switch 1_B Open load detected on LS7 switch
HB6_HS_OL	D3	r	High-side (HS) switch of half-bridge 6 open load detection 0_B No error on HS6 switch

© 2023 Silergy Corp. All Rights Reserved.

			1_B Open load detected on HS6 switch
HB6_LS_OL	D2	r	Low-side (LS) switch of half-bridge 6 open load detection 0_B No error on LS6 switch 1_B Open load detected on LS6 switch
HB5_HS_OL	D1	r	High-side (HS) switch of half-bridge 5 open load detection 0_B No error on HS5 switch 1_B Open load detected on HS5 switch
HB5_LS_OL	D0	r	Low-side (LS) switch of half-bridge 5 open load detection 0_B No error on LS5 switch 1_B Open load detected on LS5 switch

OLD_STAT_3

Open Load Error Status of Half-bridge Outputs 9-12 (Address =0x06) [reset =0x00]

D7	D6	D5	D4	D3	D2	D1	D0
HB12_HS_OL	HB12_LS_OL	HB11_HS_OL	HB11_LS_OL	HB10_HS_OL	HB10_LS_OL	HB9_HS_OL	HB9_LS_OL
r	r	r	r	r	r	r	r

Field	Bits	Type	Description
HB12_HS_OL	D7	r	High-side (HS) switch of half-bridge 12 open load detection 0_B No error on HS12 switch 1_B Open load detected on HS12 switch
HB12_LS_OL	D6	r	Low-side (LS) switch of half-bridge 12 open load detection 0_B No error on LS12 switch 1_B Open load detected on LS12 switch
HB11_HS_OL	D5	r	High-side (HS) switch of half-bridge 11 open load detection 0_B No error on HS11 switch 1_B Open load detected on HS11 switch
HB11_LS_OL	D4	r	Low-side (LS) switch of half-bridge 11 open load detection 0_B No error on LS11 switch 1_B Open load detected on LS11 switch
HB10_HS_OL	D3	r	High-side (HS) switch of half-bridge 10 open load detection 0_B No error on HS10 switch 1_B Open load detected on HS10 switch
HB10_LS_OL	D2	r	Low-side (LS) switch of half-bridge 10 open load detection 0_B No error on LS10 switch 1_B Open load detected on LS10 switch
HB9_HS_OL	D1	r	High-side (HS) switch of half-bridge 9 open load detection 0_B No error on HS9 switch 1_B Open load detected on HS9 switch
HB9_LS_OL	D0	r	Low-side (LS) switch of half-bridge 9 open load detection 0_B No error on LS9 switch 1_B Open load detected on LS9 switch

SPI Control Registers

The Control Register are used to configure the device. The control registers are read and write capable.

CONFIG_CTRL

Configuration Register (Address =0x07) [reset =0x00]

D7	D6	D5	D4	D3	D2	D1	D0
Reserved	Reserved	Reserved	Reserved	OCP_REG	OTW_REG	EXT_OVP	CLR_FLT
r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w

Field	Bits	Type	Description
Reserved	D7	r/w	Reserved. Always reads as ‘0’
Reserved	D6	r/w	Reserved. Always reads as ‘0’
Reserved	D5	r/w	Reserved. Always reads as ‘0’
Reserved	D4	r/w	Reserved. Always reads as ‘0’
OCP_REG	D3	r/w	0_B Overcurrent condition is reported in nFAULT pin 1_B Overcurrent condition warning is not reported in nFAULT pin
OTW_REG	D2	r/w	0_B Overtemperature warning is not reported in nFAULT pin

© 2023 Silergy Corp. All Rights Reserved.

			1_B Overtemperature warning is reported in nFAULT pin
EXT_OVP	D1	r/w	0_B Overvoltage protection threshold is at 21V min. 1_B Overvoltage protection threshold is at 32.7V min.
CLR_FLT	D0	r/w	0_B Faults not cleared 1_B Clear all faults

OP_CTRL_1

Half-bridge Output Control 1(Address =0x08) [reset =0x00]

D7	D6	D5	D4	D3	D2	D1	D0
HB4_HS_EN	HB4_LS_EN	HB3_HS_EN	HB3_LS_EN	HB2_HS_EN	HB2_LS_EN	HB1_HS_EN	HB1_LS_EN
r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w

Field	Bits	Type	Description
HB4_HS_EN	D7	r/w	Half-bridge output 4 High side switch enable 0_B HS4 OFF 1_B HS4 ON
HB4_LS_EN	D6	r/w	Half-bridge output 4 Low side switch enable 0_B LS4 OFF 1_B LS4 ON
HB3_HS_EN	D5	r/w	Half-bridge output 3 High side switch enable 0_B HS3 OFF 1_B HS3 ON
HB3_LS_EN	D4	r/w	Half-bridge output 3 Low side switch enable 0_B LS3 OFF 1_B LS3 ON
HB2_HS_EN	D3	r/w	Half-bridge output 2 High side switch enable 0_B HS2 OFF 1_B HS2 ON
HB2_LS_EN	D2	r/w	Half-bridge output 2 Low side switch enable 0_B LS2 OFF 1_B LS2 ON
HB1_HS_EN	D1	r/w	Half-bridge output 1 High side switch enable 0_B HS1 OFF 1_B HS1 ON
HB1_LS_EN	D0	r/w	Half-bridge output 1 Low side switch enable 0B LS1 OFF 1B LS1 ON

OP_CTRL_2

Half-bridge output control 2 (Address =0x09) [reset =0x00]

D7	D6	D5	D4	D3	D2	D1	D0
HB8_HS_EN	HB8_LS_EN	HB7_HS_EN	HB7_LS_EN	HB6_HS_EN	HB6_LS_EN	HB5_HS_EN	HB5_LS_EN
r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w

Field	Bits	Type	Description
HB8_HS_EN	D7	r/w	Half-bridge output 8 High side switch enable 0_B HS8 OFF 1_B HS8 ON
HB8_LS_EN	D6	r/w	Half-bridge output 8 Low side switch enable 0_B LS8 OFF 1_B LS8 ON
HB7_HS_EN	D5	r/w	Half-bridge output 7 High side switch enable 0_B HS7 OFF 1_B HS7 ON
HB7_LS_EN	D4	r/w	Half-bridge output 7 Low side switch enable 0_B LS7 OFF 1_B LS7 ON
HB6_HS_EN	D3	r/w	Half-bridge output 6 High side switch enable 0_B HS6 OFF 1_B HS6 ON
HB6_LS_EN	D2	r/w	Half-bridge output 6 Low side switch enable

© 2023 Silergy Corp. All Rights Reserved.

			0_B LS6 OFF 1_B LS6 ON
HB5_HS_EN	D1	r/w	Half-bridge output 5 High side switch enable 0_B HS5 OFF 1_B HS5 ON
HB5_LS_EN	D0	r/w	Half-bridge output 5 Low side switch enable 0_B LS5 OFF 1_B LS5 ON

OP_CTRL_3

Half-bridge output control 3 (Address =0x0A) [reset =0x00]

D7	D6	D5	D4	D3	D2	D1	D0
HB12_HS_EN	HB12_LS_EN	HB11_HS_EN	HB11_LS_EN	HB10_HS_EN	HB10_LS_EN	HB9_HS_EN	HB9_LS_EN
r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w

Field	Bits	Type	Description
HB12_HS_EN	D7	r/w	Half-bridge output 12 High side switch enable 0_B HS12 OFF 1_B HS12 ON
HB12_LS_EN	D6	r/w	Half-bridge output 12 Low side switch enable 0_B LS12 OFF 1_B LS12 ON
HB11_HS_EN	D5	r/w	Half-bridge output 11 High side switch enable 0_B HS11 OFF 1_B HS11 ON
HB11_LS_EN	D4	r/w	Half-bridge output 11 Low side switch enable 0_B LS11 OFF 1_B LS11 ON
HB10_HS_EN	D3	r/w	Half-bridge output 10 High side switch enable 0_B HS10 OFF 1_B HS10 ON
HB10_LS_EN	D2	r/w	Half-bridge output 10 Low side switch enable 0_B LS10 OFF 1_B LS10 ON
HB9_HS_EN	D1	r/w	Half-bridge output 9 High side switch enable 0_B HS9 OFF 1_B HS9 ON
HB9_LS_EN	D0	r/w	Half-bridge output 9 Low side switch enable 0_B LS9 OFF 1_B LS9 ON

PWM_CTRL_1

Half-bridge PWM Control 1 (Address =0x0B) [reset =0x00]

D7	D6	D5	D4	D3	D2	D1	D0
HB8_PWM	HB7_PWM	HB6_PWM	HB5_PWM	HB4_PWM	HB3_PWM	HB2_PWM	HB1_PWM
r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w

Field	Bits	Type	Description
HB8_PWM	D7	r/w	0_B Half-bridge 8 is operating in continuous mode 1_B Half-bridge 8 is operating in PWM mode
HB7_PWM	D6	r/w	0_B Half-bridge 7 is operating in continuous mode 1_B Half-bridge 7 is operating in PWM mode
HB6_PWM	D5	r/w	0_B Half-bridge 6 is operating in continuous mode 1_B Half-bridge 6 is operating in PWM mode
HB5_PWM	D4	r/w	0_B Half-bridge 5 is operating in continuous mode 1_B Half-bridge 5 is operating in PWM mode
HB4_PWM	D3	r/w	0_B Half-bridge 4 is operating in continuous mode 1_B Half-bridge 4 is operating in PWM mode
HB3_PWM	D2	r/w	0_B Half-bridge 3 is operating in continuous mode 1_B Half-bridge 3 is operating in PWM mode

© 2023 Silergy Corp. All Rights Reserved.

HB2_PWM	D1	r/w	0_B Half-bridge 2 is operating in continuous mode 1_B Half-bridge 2 is operating in PWM mode
HB1_PWM	D0	r/w	0_B Half-bridge 1 is operating in continuous mode 1_B Half-bridge 1 is operating in PWM mode

PWM_CTRL_2

Half-bridge PWM Control 2 (Address =0x0C) [reset =0x00]

D7	D6	D5	D4	D3	D2	D1	D0
PWM_CH4_DIS	PWM_CH3_DIS	PWM_CH2_DIS	PWM_CH1_DIS	HB12_PWM	HB11_PWM	HB10_PWM	HB9_PWM
r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w

Field	Bits	Type	Description
PWM_CH4_DIS	D7	r/w	0_B PWM Generator-4 is enabled 1_B PWM Generator-4 is disabled
PWM_CH3_DIS	D6	r/w	0_B PWM Generator-3 is enabled 1_B PWM Generator-3 is disabled
PWM_CH2_DIS	D5	r/w	0_B PWM Generator-2 is enabled 1_B PWM Generator-2 is disabled
PWM_CH1_DIS	D4	r/w	0_B PWM Generator-1 is enabled 1_B PWM Generator-1 is disabled
HB12_PWM	D3	r/w	0_B Half-bridge 12 is operating in continuous mode 1_B Half-bridge 12 is operating in PWM mode
HB11_PWM	D2	r/w	0_B Half-bridge 11 is operating in continuous mode 1_B Half-bridge 11 is operating in PWM mode
HB10_PWM	D1	r/w	0_B Half-bridge 10 is operating in continuous mode 1_B Half-bridge 10 is operating in PWM mode
HB9_PWM	D0	r/w	0_B Half-bridge 9 is operating in continuous mode 1_B Half-bridge 9 is operating in PWM mode

FW _CTRL_1

Free-wheeling Configuration 1 (Address =0x0D) [reset =0x00]

D7	D6	D5	D4	D3	D2	D1	D0
FW_HB8	FW_HB7	FW_HB6	FW_HB5	FW_HB4	FW_HB3	FW_HB2	FW_HB1
r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w

Field	Bits	Type	Description
FW_HB8	D7	r/w	HB8 free-wheeling configuration 0_B Passive free-wheeling 1_B Active free-wheeling
FW_HB7	D6	r/w	HB7 free-wheeling configuration 0_B Passive free-wheeling 1_B Active free-wheeling
FW_HB6	D5	r/w	HB6 free-wheeling configuration 0_B Passive free-wheeling 1_B Active free-wheeling
FW_HB5	D4	r/w	HB5 free-wheeling configuration 0_B Passive free-wheeling 1_B Active free-wheeling
FW_HB4	D3	r/w	HB4 free-wheeling configuration 0_B Passive free-wheeling 1_B Active free-wheeling
FW_HB3	D2	r/w	HB3 free-wheeling configuration 0_B Passive free-wheeling 1_B Active free-wheeling
FW_HB2	D1	r/w	HB2 free-wheeling configuration 0_B Passive free-wheeling 1_B Active free-wheeling
FW_HB1	D0	r/w	HB1 free-wheeling configuration 0_B Passive free-wheeling

© 2023 Silergy Corp. All Rights Reserved.

			1_B Active free-wheeling

FW _CTRL_2

Free-wheeling Configuration 2 (Address =0x0E) [reset =0x00]

D7	D6	D5	D4	D3	D2	D1	D0
Reserved	Reserved	Reserved	Reserved	FW_HB12	FW_HB11	FW_HB10	FW_HB9
r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w

Field	Bits	Type	Description
Reserved	D7	r/w	Reserved. Always reads as '0'
Reserved	D6	r/w	Reserved. Always reads as '0'
Reserved	D5	r/w	Reserved. Always reads as '0'
Reserved	D4	r/w	Reserved. Always reads as '0'
FW_HB12	D3	r/w	HB12 free-wheeling configuration 0_B Passive free-wheeling 1_B Active free-wheeling
FW_HB11	D2	r/w	HB11 free-wheeling configuration 0_B Passive free-wheeling 1_B Active free-wheeling
FW_HB10	D1	r/w	HB10 free-wheeling configuration 0_B Passive free-wheeling 1_B Active free-wheeling
FW_HB9	D0	r/w	HB9 free-wheeling configuration 0_B Passive free-wheeling 1_B Active free-wheeling

PWM_MAP_CTRL_1

Half-bridge Output PWM Map Control 1 (Address =0x0F) [reset =0x00]

D7	D6	D5	D4	D3	D2	D1	D0
HB4_PWM_MAP		HB3_PWM_MAP		HB2_PWM_MAP		HB1_PWM_MAP	
r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w

Field	Bits	Type	Description
HB4_PWM_MAP	D7:D6	r/w	Half-bridge output 4 mode select 00_B PWM control with PWM Channel 1 01_B PWM control with PWM Channel 2 10_B PWM control with PWM Channel 3 11_B PWM control with PWM Channel 4
HB3_PWM_MAP	D5:D4	r/w	Half-bridge output 3 mode select 00_B PWM control with PWM Channel 1 01_B PWM control with PWM Channel 2 10_B PWM control with PWM Channel 3 11_B PWM control with PWM Channel 4
HB2_PWM_MAP	D3:D2	r/w	Half-bridge output 2 mode select 00_B PWM control with PWM Channel 1 01_B PWM control with PWM Channel 2 10_B PWM control with PWM Channel 3 11_B PWM control with PWM Channel 4
HB1_PWM_MAP	D1:D0	r/w	Half-bridge output 1 mode select 00_B PWM control with PWM Channel 1 01_B PWM control with PWM Channel 2 10_B PWM control with PWM Channel 3 11_B PWM control with PWM Channel 4

PWM_MAP_CTRL_2

Half-bridge Output PWM Map Control 2 (Address =0x10) [reset =0x00]

D7	D6	D5	D4	D3	D2	D1	D0
HB8_PWM_MAP		HB7_PWM_MAP		HB6_PWM_MAP		HB5_PWM_MAP	
r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w

© 2023 Silergy Corp. All Rights Reserved.

Field	Bits	Type	Description
HB8_PWM_MAP	D7:D6	r/w	Half-bridge output 8 mode select 00_B PWM control with PWM Channel 1 01_B PWM control with PWM Channel 2 10_B PWM control with PWM Channel 3 11_B PWM control with PWM Channel 4
HB7_PWM_MAP	D5:D4	r/w	Half-bridge output 7 mode select 00_B PWM control with PWM Channel 1 01_B PWM control with PWM Channel 2 10_B PWM control with PWM Channel 3 11_B PWM control with PWM Channel 4
HB6_PWM_MAP	D3:D2	r/w	Half-bridge output 6 mode select 00_B PWM control with PWM Channel 1 01_B PWM control with PWM Channel 2 10_B PWM control with PWM Channel 3 11_B PWM control with PWM Channel 4
HB5_PWM_MAP	D1:D0	r/w	Half-bridge output 5 mode select 00_B PWM control with PWM Channel 1 01_B PWM control with PWM Channel 2 10_B PWM control with PWM Channel 3 11_B PWM control with PWM Channel 4

PWM_MAP_CTRL_3

Half-bridge Output PWM Map Control 3 (Address =0x11) [reset =0x00]

D7	D6	D5	D4	D3	D2	D1	D0
HB12_PWM_MAP		HB11_PWM_MAP		HB10_PWM_MAP		HB9_PWM_MAP	
r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w

Field	Bits	Type	Description
HB12_PWM_MAP	D7:D6	r/w	Half-bridge output 12 mode select 00_B PWM control with PWM Channel 1 01_B PWM control with PWM Channel 2 10_B PWM control with PWM Channel 3 11_B PWM control with PWM Channel 4
HB11_PWM_MAP	D5:D4	r/w	Half-bridge output 11 mode select 00_B PWM control with PWM Channel 1 01_B PWM control with PWM Channel 2 10_B PWM control with PWM Channel 3 11_B PWM control with PWM Channel 4
HB10_PWM_MAP	D3:D2	r/w	Half-bridge output 10 mode select 00_B PWM control with PWM Channel 1 01_B PWM control with PWM Channel 2 10_B PWM control with PWM Channel 3 11_B PWM control with PWM Channel 4
HB9_PWM_MAP	D1:D0	r/w	Half-bridge output 9 mode select 00_B PWM control with PWM Channel 1 01_B PWM control with PWM Channel 2 10_B PWM control with PWM Channel 3 11_B PWM control with PWM Channel 4

PWM_ FREQ_CTRL

PWM Channel Frequency Select (Address =0x12) [reset =0x00]

D7	D6	D5	D4	D3	D2	D1	D0
PWM_CH4_FREQ		PWM_CH3_FREQ		PWM_CH2_FREQ		PWM_CH1_FREQ	
r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w

Field	Bits	Type	Description
PWM_CH4_FREQ	D7:D6	r/w	PWM Channel 4 frequency select 00_B PWM frequency: 80Hz 01_B PWM frequency: 100Hz

© 2023 Silergy Corp. All Rights Reserved.

			10_B PWM frequency: 200Hz 11_B PWM frequency: 2000Hz
PWM_CH3_FREQ	D5:D4	r/w	PWM Channel 3 frequency select 00_B PWM frequency: 80Hz 01_B PWM frequency: 100Hz 10_B PWM frequency: 200Hz 11_B PWM frequency: 2000Hz
PWM_CH2_FREQ	D3:D2	r/w	PWM Channel 2 frequency select 00_B PWM frequency: 80Hz 01_B PWM frequency: 100Hz 10_B PWM frequency: 200Hz 11_B PWM frequency: 2000Hz
PWM_CH1_FREQ	D1:D0	r/w	PWM Channel 1 frequency select 00_B PWM frequency: 80Hz 01_B PWM frequency: 100Hz 10_B PWM frequency: 200Hz 11_B PWM frequency: 2000Hz

PWM_DUTY_CTRL_1

PWM Channel 1 Duty Cycle Configuration (Address =0x13) [reset =0x00]

D7	D6	D5	D4	D3	D2	D1	D0
PWM_DUTY_CH1							
r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w

Field	Bits	Type	Description
PWM_DUTY_CH1	D7:D0	r/w	PWM Channel 1 Duty Cycle configuration 0000 0000_B 100% OFF xxxx $xxxx_B$ parts of 255 ON 1111 1111_B 100% ON

PWM1_DUTY_CTRL_2

PWM Channel 2 Duty Cycle Configuration (Address =0x14) [reset =0x00]

D7	D6	D5	D4	D3	D2	D1	D0
PWM_DUTY_CH2							
r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w

Field	Bits	Type	Description
PWM_DUTY_CH2	D7:D0	r/w	PWM Channel 2 Duty Cycle configuration 0000 0000_B 100% OFF xxxx $xxxx_B$ parts of 255 ON 1111 1111_B 100% ON

PWM1_DUTY_CTRL_3

PWM Channel 3 Duty Cycle Configuration (Address =0x15) [reset =0x00]

D7	D6	D5	D4	D3	D2	D1	D0
PWM_DUTY_CH3							
r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w

Field	Bits	Type	Description
PWM_DUTY_CH3	D7:D0	r/w	PWM Channel 3 Duty Cycle configuration 0000 0000_B 100% OFF xxxx $xxxx_B$ parts of 255 ON 1111 1111_B 100% ON

PWM1_DUTY_CTRL_4

PWM Channel 4 Duty Cycle Configuration (Address =0x16) [reset =0x00]

D7	D6	D5	D4	D3	D2	D1	D0
PWM_DUTY_CH4							

© 2023 Silergy Corp. All Rights Reserved.

r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w

Field	Bits	Type	Description
PWM_DUTY_CH4	D7:D0	r/w	PWM Channel 4 Duty Cycle configuration 0000 0000$_B$ 100% OFF xxxx xxxx$_B$ parts of 255 ON 1111 1111$_B$ 100% ON

SR _CTRL_1

The Slew Rate Configuration 1 (Address =0x17) [reset =0x00]

D7	D6	D5	D4	D3	D2	D1	D0
HB8_SR	HB7_SR	HB6_SR	HB5_SR	HB4_SR	HB3_SR	HB2_SR	HB1_SR
r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w

Field	Bits	Type	Description
HB8_SR	D7	r/w	HB8 slew rate configuration 0$_B$ 1V/μs 1$_B$ 3.7V/μs
HB7_SR	D6	r/w	HB7 slew rate configuration 0$_B$ 1V/μs 1$_B$ 3.7V/μs
HB6_SR	D5	r/w	HB6 slew rate configuration 0$_B$ 1V/μs 1$_B$ 3.7V/μs
HB5_SR	D4	r/w	HB5 slew rate configuration 0$_B$ 1V/μs 1$_B$ 3.7V/μs
HB4_SR	D3	r/w	HB4 slew rate configuration 0$_B$ 1V/μs 1$_B$ 3.7V/μs
HB3_SR	D2	r/w	HB3 slew rate configuration 0$_B$ 1V/μs 1$_B$ 3.7V/μs
HB2_SR	D1	r/w	HB2 slew rate configuration 0$_B$ 1V/μs 1$_B$ 3.7V/μs
HB1_SR	D0	r/w	HB1 slew rate configuration 0$_B$ 1V/μs 1$_B$ 3.7V/μs

SR _CTRL_2

The Slew Rate Configuration 2 (Address =0x18) [reset =0x00]

D7	D6	D5	D4	D3	D2	D1	D0
HB8_SR	HB7_SR	HB6_SR	HB5_SR	HB4_SR	HB3_SR	HB2_SR	HB1_SR
r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w

Field	Bits	Type	Description
Reserved	D7	r/w	Reserved. Always reads as ‘0’
Reserved	D6	r/w	Reserved. Always reads as ‘0’
Reserved	D5	r/w	Reserved. Always reads as ‘0’
Reserved	D4	r/w	Reserved. Always reads as ‘0’
HB12_SR	D3	r/w	HB12 slew rate configuration 0$_B$ 1V/μs 1$_B$ 3.7V/μs
HB11_SR	D2	r/w	HB11 slew rate configuration 0$_B$ 1V/μs 1$_B$ 3.7V/μs
HB10_SR	D1	r/w	HB10 slew rate configuration 0$_B$ 1V/μs 1$_B$ 3.7V/μs

© 2023 Silergy Corp. All Rights Reserved.

HB9_SR	D0	r/w	HB9 slew rate configuration 0_B 1V/μs 1_B 3.7V/μs

OLD _CTRL_1

The Open Load Detect Control 1 (Address =0x19) [reset =0x00]

D7	D6	D5	D4	D3	D2	D1	D0
HB8_OLD_DIS	HB7_OLD_DIS	HB6_OLD_DIS	HB5_OLD_DIS	HB4_OLD_DIS	HB3_OLD_DIS	HB2_OLD_DIS	HB1_OLD_DIS
r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w

Field	Bits	Type	Description
HB8_OLD_DIS	D7	r/w	HB8 open load detect configuration 0_B Open-load detection on half-bridge 8 is enable 1_B Open-load detection on half-bridge 8 is disable
HB7_OLD_DIS	D6	r/w	HB7 open load detect configuration 0_B Open-load detection on half-bridge 7 is enable 1_B Open-load detection on half-bridge 7 is disable
HB6_OLD_DIS	D5	r/w	HB6 open load detect configuration 0_B Open-load detection on half-bridge 6 is enable 1_B Open-load detection on half-bridge 6 is disable
HB5_OLD_DIS	D4	r/w	HB5 open load detect configuration 0_B Open-load detection on half-bridge 5 is enable 1_B Open-load detection on half-bridge 5 is disable
HB4_OLD_DIS	D3	r/w	HB4 open load detect configuration 0_B Open-load detection on half-bridge 4 is enable 1_B Open-load detection on half-bridge 4 is disable
HB3_OLD_DIS	D2	r/w	HB3 open load detect configuration 0_B Open-load detection on half-bridge 3 is enable 1_B Open-load detection on half-bridge 3 is disable
HB2_OLD_DIS	D1	r/w	HB2 open load detect configuration 0_B Open-load detection on half-bridge 2 is enable 1_B Open-load detection on half-bridge 2 is disable
HB1_OLD_DIS	D0	r/w	HB1 open load detect configuration 0_B Open-load detection on half-bridge 1 is enable 1_B Open-load detection on half-bridge 1 is disable

OLD _CTRL_2

The Open Load Detect Control 2 (Address =0x1A) [reset =0x00]

D7	D6	D5	D4	D3	D2	D1	D0
OLD_REP	OLD_OP	Reserved		HB12_OLD_DIS	HB11_OLD_DIS	HB10_OLD_DIS	HB9_OLD_DIS
r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w

Field	Bits	Type	Description
OLD_REP	D7	r/w	0_B Report on nFAULT pin during OLD condition 1_B No report on nFAULT pin during OLD condition
OLD_OP	D6	r/w	0_B Half-bridge are not active after OLD condition detect 1_B Half-bridge are active after OLD condition detect
Reserved	D5	r/w	Reserved. Always reads as '0'
Reserved	D4	r/w	Reserved. Always reads as '0'
HB12_OLD_DIS	D3	r/w	HB12 open load detect configuration 0_B Open-load detection on half-bridge 12 is enable 1_B Open-load detection on half-bridge 12 is disable
HB11_OLD_DIS	D2	r/w	HB11 open load detect configuration 0_B Open-load detection on half-bridge 11 is enable 1_B Open-load detection on half-bridge 11 is disable
HB10_OLD_DIS	D1	r/w	HB10 open load detect configuration 0_B Open-load detection on half-bridge 10 is enable 1_B Open-load detection on half-bridge 10 is disable
HB9_OLD_DIS	D0	r/w	HB9 open load detect configuration

© 2023 Silergy Corp. All Rights Reserved.

			0_B Open-load detection on half-bridge 9 is enable 1_B Open-load detection on half-bridge 9 is disable

OLD _CTRL_3

The Open Load Detect Control 3 (Address =0x1B) [reset =0x00]

D7	D6	D5	D4	D3	D2	D1	D0
OCP_DEG			Reserved	HB12_OLD_ EN	HB11_OLD_ EN	HB10_OLD_ EN	HB9_OLD_E N
r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w

Field	Bits	Type	Description
OCP_DEG	D7:D5	r/w	000_B OCP deglitch time is 10μs 001_B OCP deglitch time is 5μs 010_B OCP deglitch time is 2.5μs 011_B OCP deglitch time is 1μs 100_B OCP deglitch time is 60μs 101_B OCP deglitch time is 40μs 110_B OCP deglitch time is 30μs 111_B OCP deglitch time is 20μs
Reserved	D4	r/w	Reserved. Always reads as '0'
HB12_OLD_EN	D3	r/w	HB12 low-current OLD detect configuration 0_B Low-current OLD detection on half-bridge 12 is disable 1_B Low-current OLD detection on half-bridge 12 is enable
HB11_OLD_ EN	D2	r/w	HB11 low-current OLD detect configuration 0_B Low-current OLD detection on half-bridge 11 is disable 1_B Low-current OLD detection on half-bridge 11 is enable
HB10_OLD_ EN	D1	r/w	HB10 low-current OLD detect configuration 0_B Low-current OLD detection on half-bridge 10 is disable 1_B Low-current OLD detection on half-bridge 10 is enable
HB9_OLD_ EN	D0	r/w	HB9 low-current OLD detect configuration 0_B Low-current OLD detection on half-bridge 9 is disable 1_B Low-current OLD detection on half-bridge 9 is enable

OLD _CTRL_4

The Open Load Detect Control 4 (Address =0x24) [reset =0x00]

D7	D6	D5	D4	D3	D2	D1	D0
HB8_OLD_E N	HB7_OLD_E N	HB6_OLD_E N	HB5_OLD_E N	HB4_OLD_E N	HB3_OLD_E N	HB2_OLD_E N	HB1_OLD_E N
r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w

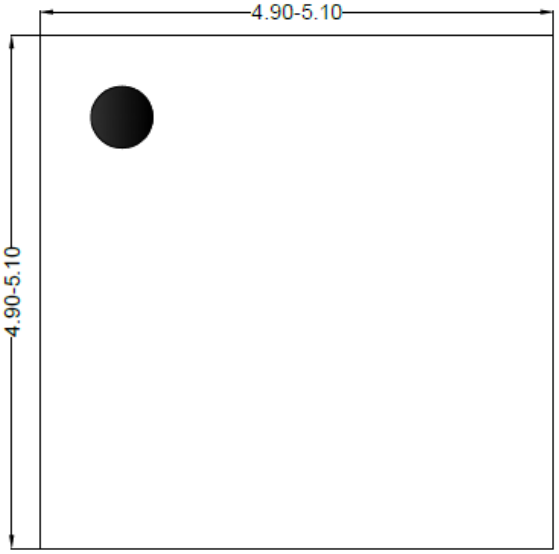
Field	Bits	Type	Description
HB8_OLD_ EN	D7	r/w	HB8 low-current OLD detect configuration 0_B Low-current OLD detection on half-bridge 8 is disable 1_B Low-current OLD detection on half-bridge 8 is enable
HB7_OLD_ EN	D6	r/w	HB7 low-current OLD detect configuration 0_B Low-current OLD detection on half-bridge 7 is disable 1_B Low-current OLD detection on half-bridge 7 is enable
HB6_OLD_EN	D5	r/w	HB6 low-current OLD detect configuration 0_B Low-current OLD detection on half-bridge 6 is disable 1_B Low-current OLD detection on half-bridge 6 is enable
HB5_OLD_ EN	D4	r/w	HB5 low-current OLD detect configuration 0_B Low-current OLD detection on half-bridge 5 is disable 1_B Low-current OLD detection on half-bridge 5 is enable
HB4_OLD_ EN	D3	r/w	HB4 low-current OLD detect configuration 0_B Low-current OLD detection on half-bridge 4 is disable 1_B Low-current OLD detection on half-bridge 4 is enable
HB3_OLD_ EN	D2	r/w	HB3 low-current OLD detect configuration 0_B Low-current OLD detection on half-bridge 3 is disable 1_B Low-current OLD detection on half-bridge 3 is enable
HB2_OLD_ EN	D1	r/w	HB2 low-current OLD detect configuration 0_B Low-current OLD detection on half-bridge 2 is disable

© 2023 Silergy Corp. All Rights Reserved.

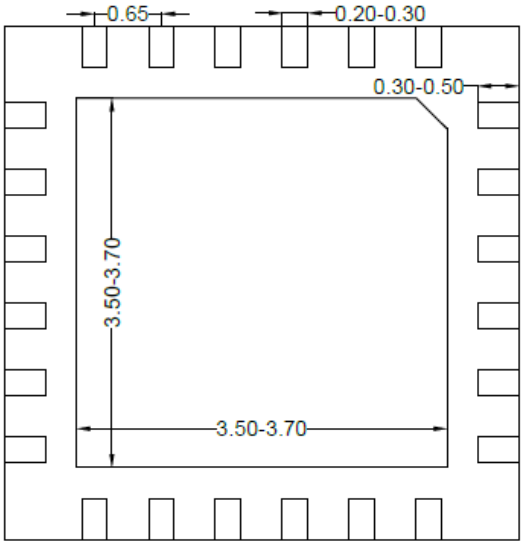
			1_B Low-current OLD detection on half-bridge 2 is enable
HB1_OLD_ EN	D0	r/w	HB1 low-current OLD detect configuration 0_B Low-current OLD detection on half-bridge 1 is disable 1_B Low-current OLD detection on half-bridge 1 is enable

© 2023 Silergy Corp. All Rights Reserved.

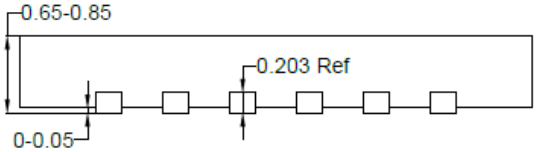
QFN5×5-24 Package Outline Drawing



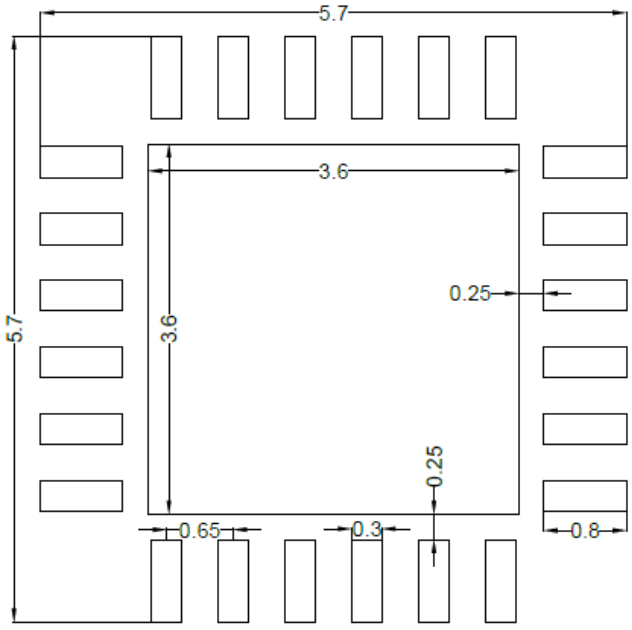
Top View



Bottom View



Front View



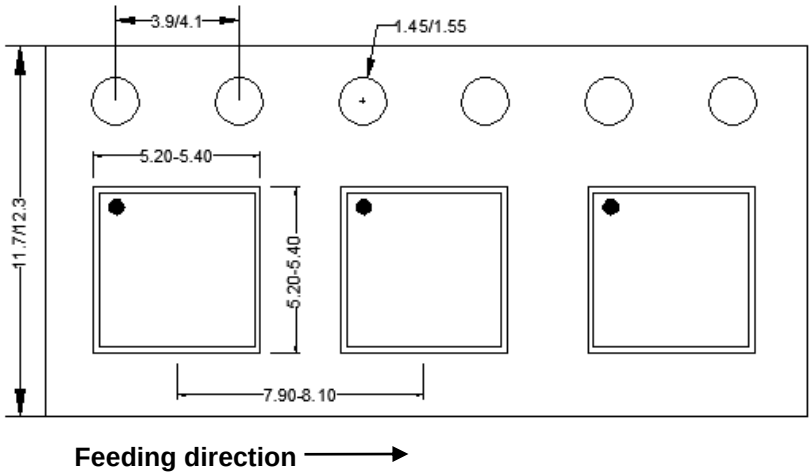
Recommended PCB Layout
(Reference Only)

Note: All dimensions are in millimeters and exclude mold flash & metal burr.

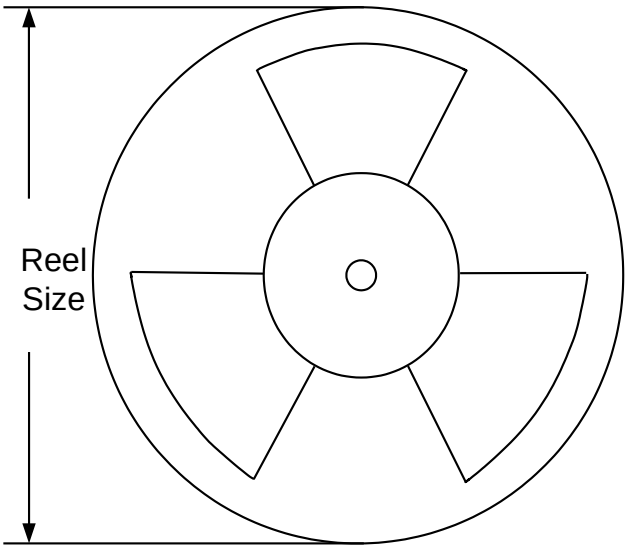
© 2023 Silergy Corp. All Rights Reserved.

Taping & Reel Specification

QFN5×5 Taping Orientation



Carrier Tape & Reel Specification for Packages



Package type	Tape width (mm)	Pocket pitch (mm)	Reel size (Inch)	Trailer length (mm)	Leader length (mm)	Qty per reel
QFN5×5	12	8	13"	400	400	5000

© 2023 Silergy Corp. All Rights Reserved.

Revision History

The revision history provided is for informational purpose only and is believed to be accurate, however, not warrantied. Please make sure that you have the latest revision.

Revision Number	Revision Date	Description
1.0	Nov 30, 2023	Initial Release

© 2023 Silergy Corp. All Rights Reserved.

IMPORTANT NOTICE

1. **Right to make changes.** Silergy and its subsidiaries (hereafter Silergy) reserve the right to change any information published in this document, including but not limited to circuitry, specification and/or product design, manufacturing or descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products are sold subject to Silergy's standard terms and conditions of sale.

2. Applications. Application examples that are described herein for any of these products are for illustrative purposes only. Silergy makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification. Buyers are responsible for the design and operation of their applications and products using Silergy products. Silergy or its subsidiaries assume no liability for any application assistance or designs of customer products. It is customer's sole responsibility to determine whether the Silergy product is suitable and fit for the customer's applications and products planned. To minimize the risks associated with customer's products and applications, customer should provide adequate design and operating safeguards. Customer represents and agrees that it has all the necessary expertise to create and implement safeguards which anticipate dangerous consequences of failures, monitor failures and their consequences, lessen the likelihood of failures that might cause harm and take appropriate remedial actions. Silergy assumes no liability related to any default, damage, costs or problem in the customer's applications or products, or the application or use by customer's third-party buyers. Customer will fully indemnify Silergy, its subsidiaries, and their representatives against any damages arising out of the use of any Silergy components in safety-critical applications. It is also buyers' sole responsibility to warrant and guarantee that any intellectual property rights of a third party are not infringed upon when integrating Silergy products into any application. Silergy assumes no responsibility for any said applications or for any use of any circuitry other than circuitry entirely embodied in a Silergy product.

3. **Limited warranty and liability.** Information furnished by Silergy in this document is believed to be accurate and reliable. However, Silergy makes no representation or warranty, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information. In no event shall Silergy be liable for any indirect, incidental, punitive, special or consequential damages, including but not limited to lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges, whether or not such damages are based on tort or negligence, warranty, breach of contract or any other legal theory. Notwithstanding any damages that customer might incur for any reason whatsoever, Silergy' aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the Standard Terms and Conditions of Sale of Silergy.

4. **Suitability for use.** Customer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of Silergy components in its applications, notwithstanding any applications-related information or support that may be provided by Silergy. Silergy products are not designed, authorized or warranted to be suitable for use in life support, life-critical or safety-critical systems or equipment, nor in applications where failure or malfunction of a Silergy product can reasonably be expected to result in personal injury, death or severe property or environmental damage. Silergy assumes no liability for inclusion and/or use of Silergy products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

5. **Terms and conditions of commercial sale**. Silergy products are sold subject to the standard terms and conditions of commercial sale, as published at http://www.silergy.com, unless otherwise agreed in a valid written individual agreement specifically agreed to in writing by an authorized officer of Silergy. In case an individual agreement is concluded only the terms and conditions of the respective agreement shall apply. Silergy hereby expressly objects to and denies the application of any customer's general terms and conditions with regard to the purchase of Silergy products by the customer.

6. **No offer to sell or license**. Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights. Silergy makes no representation or warranty that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right. Information published by Silergy regarding third-party products or services does not constitute a license to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from Silergy under the patents or other intellectual property of Silergy.

For more information, please visit: www.silergy.com

© 2023 Silergy Corp. **All Rights Reserved**

© 2023 Silergy Corp. All Rights Reserved.