SY2A54508

Analog Class-D Audio IC for Automotive Application

General Description

The SY2A54508 is a high efficiency mono Class-D audio power amplifier for automotive emergency call (e-Call), telematics, instrument cluster, and acoustic vehicle alerting system (AVAS) applications. It can output 8W into a 4Ω load at less than 0.1% THD+N from a 14.4V supply. The product can operate on a wide voltage range with battery supply. The adjustable power limit function allows user to set a virtual voltage rail lower than supply voltage to limit the amount of current through the speaker. Output DC detection circuit prevents speaker damage from long-time current stress if the input capacitors are damaged or shorts exist on the inputs.

The SY2A54508 can drive a mono speaker as low as 2Ω. The high efficiency of the amplifier allows eliminating an external heat sink when playing music.

Overcurrent protection can protect amplifier from output short to GND, PVDD, and output-to-output. The overcurrent protection, DC protection, and overtemperature protection include an auto-recovery feature. The amplifier also has a built-in load diagnostic function designed for detecting the status of output connections at start. It supports the following diagnostics: speaker wire shorted to GND or PVDD, speaker cross-shorted, and speaker open. The diagnostics result is reported by the I²C registers and the FAULTZ pin.

The SY2A54508 is available in a compact TSSOP16E package.

Features

- Wide Voltage Range
  - 4.5V to 28V with Under and Overvoltage Protection
  - 40V Load-dump Protection per ISO-16750-2
- High Output Power Capability
  - 8W/4 Ω, 0.1% THD+N at 14.4V
  - 12W/4Ω, <1% THD+N at 12V
- Excellent Audio performance
  - 0.03% THD+N at 1W/4 Ω 12V
  - 102dB A-weighted SNR
- Comprehensive Protection
  - Undervoltage, Overvoltage, Overtemperature, Overcurrent, and DC Detection Protection with Auto Recovery
  - Selectable Power Limit Function for Speaker Protection
- Load Diagnostic Functions
  - Open and Shorted Output Load
  - Output-to-ground, Output-to-PVDD Shorts, and Shorted Output Indicator
- AEC-Q100 Qualified with the Following Results
  - Device Temperature Grade 1: -40°C to 125°C Ambient Operating Temperature Range
  - Device HBM ESD Classification Level H2
  - Device CDM ESD Classification Level C3
- Differential/Single-ended Input
- I²C Deglitch
- Spread Spectrum and Programmable Edge Rate to Optimize EMC Performance

Applications

- Automotive Clusters
- Automotive Emergency Call Systems (eCall)
- Automotive Telematics
- Automotive Acoustic Vehicle Alerting System (AVAS)

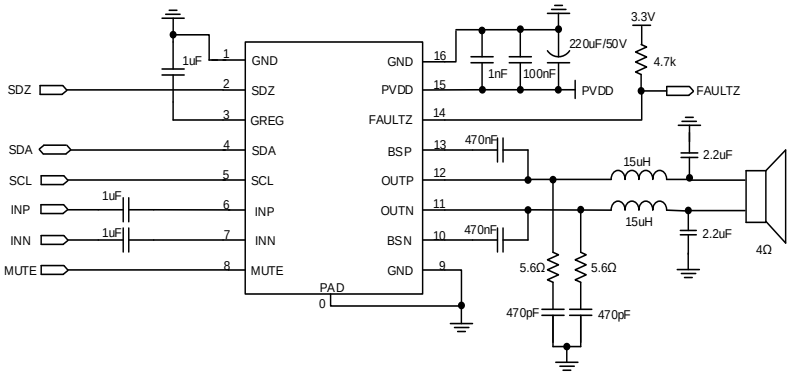


Figure 1. Typical Application Circuit

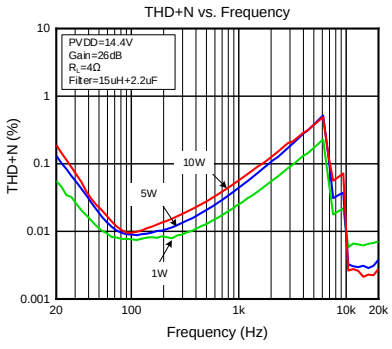


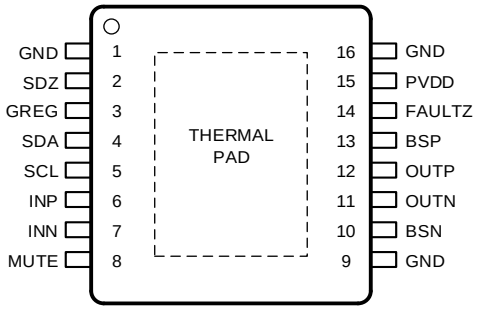
Figure 2. THD+N vs. Frequency

Ordering Information

Ordering Part Number	Package Type	Top Mark
SY2A54508HFP	TSSOP16E RoHS Compliant and Halogen Free	**EUM*xyz***

x=year code, y=week code, z= lot number code

Pinout (Top View)



Pin Name	Pin No	Type (1)	Pin Description
SDZ	2	DI	Hardware shutdown pin, active low. Can be pulled up to PVDD with resistor.
FAULTZ	14	DO	Open drain output used to display fault status, active low.
GREG	3	P	Internal regulator output. Decouple to GND with at least a 1μF capacitor as close to the pin as possible. This pin must not be used to drive external circuit.
INP	6	AI	Positive audio input. Biased at 2.4V, a DC blocking capacitor should be used on this pin.
INN	7	AI	Negative audio input. Biased at 2.4V, a DC blocking capacitor should be used on this pin.
MUTE	8	DI	Hardware mute input, active high. Can be pulled up to PVDD with resistor.
PVDD	15	P	Power supply. Decouple to GND with a 0.1μF and a 1nF capacitors, with the smallest capacitor placed as close to the pin as possible. Add a 220μF or greater capacitor for low frequency noise filtering.
BSP	13	AI	Bootstrap supply for positive high-side FET. Connect a 470nF ceramic capacitor between the BSP and the OUTP pins.
OUTP	12	PO	Class-D H-bridge positive output.
GND	1,9,16	P	Power Ground.
BSN	10	AI	Bootstrap supply for negative high-side FET. Connect a 470nF ceramic capacitor between the BSN and the OUTN pins.
OUTN	11	PO	Class-D H-bridge negative output.
SDA	4	DIO	I²C serial control data input and output.
SCL	5	DI	I²C serial clock input.
Thermal Pad	—	—	Should be soldered to ground with multiple vias for the best heat dissipation and electrical performance.

Note 1: Type: A =analog; D =digital; P =power/ground/decoupling; I =input; O =output; IO=inout

Block Diagram

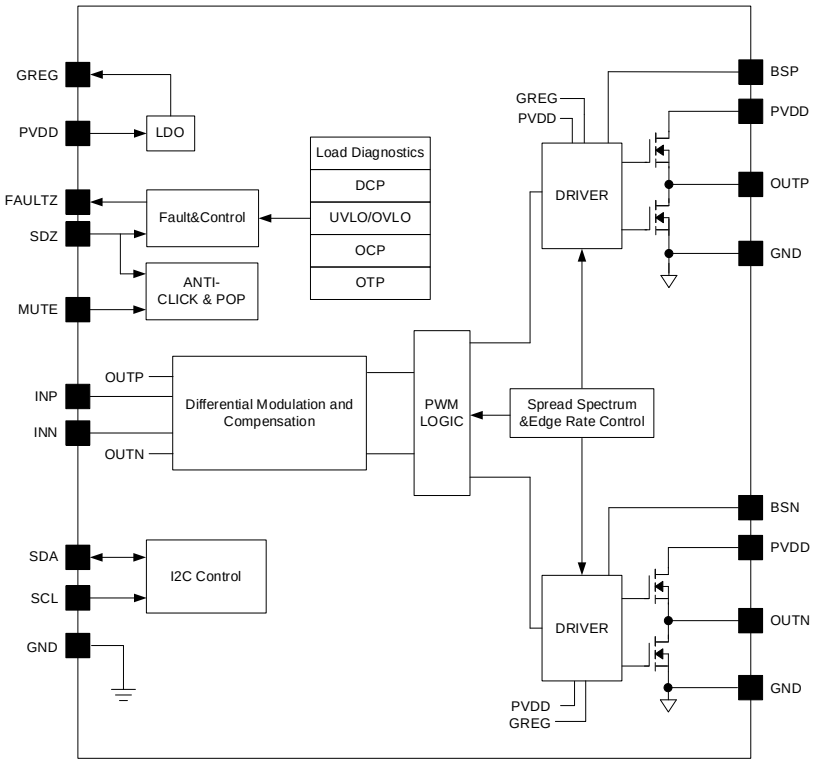


Figure 3. Block Diagram

Absolute maximum Ratings (1)

Parameter	Min	Max	Unit
V_{DD}, Supply Voltage PVDD	-0.3	34	V
$V_{DD,MAX}$, Transient supply voltage: PVDD (t ≤ 400ms exposure)	-1	40	
OUTx	-1	34	
BSx to OUTx	-0.3	4	
V_I, Interface Pin Voltage SDZ, MUTE, FAULTZ	-0.3	PVDD +0.3	
INP, INN	-0.3	3.6	
SDA, SCL	-0.3	GREG +0.3	
T_J, Operating Junction Temperature	-40	150	℃
T_{stg}, Operating Storage Temperature	-65	150	

Thermal Information (2)

Parameter	Value	Unit
θ_{JA}	28.4	°C/W
θ_{JC} (top)	20	
θ_{JC} (bottom)	2.6	
θ_{JB}	15.3	
Ψ_{JT}	0.3	

Recommended Operating Conditions (3)

Parameter	Min	Max	Unit
V_{DD}, Supply Voltage PVDD	4.5	28	V
V_{IH}, High-Level Input Voltage SDZ, MUTE	1.25	3.3	
V_{IL}, Low-Level Input Voltage SDZ, MUTE	0	0.5	
R_L, Minimum Load Resistance Output Configuration	1.8	-	Ω
T_A, Operating Ambient Temperature Range	-40	125	℃

Electrical Characteristics

T_A = -40°C to 125°C, PVDD=12V, R_L=4Ω, default I²C setting, typical values are test at T_A=25°C unless otherwise specified (4)

Parameter		Symbol	Test Condition	Min	Typ	Max	Unit
DC Characteristics	PVDD	V_{DD}		4.5		28	V
	Quiescent Supply Current	I_Q	SDZ=high, no load, no snubber	-	12	-	mA
			SDZ=high, with 4Ω load, 5.6Ω+470pF snubber, 15uH+2.2uF filter (5)	-	18.4	-	
			SDZ=low, no load, no snubber	-	5.2	-	μA
	High-Level Input Voltage	V_{IH}	SDZ, MUTE	1.3	-	-	V
	Low-Level Input Voltage	V_{IL}	SDZ, MUTE		-	0.5	V
	Low-Level Output Voltage	V_{OL}	FAULTZ, $R_{PULL-UP}$=100kΩ	-	-	0.5	V
	High-Level Input Current	I_{IH}	V_I= 12V, V_{DD}=18V	-	-	1	μA
	Low-Level Input Current	I_{IL}	V_I= 0V, V_{DD}=18V	-	-	1	μA
	Drain-Source on-State Resistance	R_{DSON}	V_{DD}=12V, Id=200mA, T_J=25°C, includes bonding wire and metallization resistance	-	180	-	mΩ
	Gain	G	No load	19	20	21	dB
				25	26	27	
				31	32	33	
				35	36	37	
	Turn-on Time	t_{ON}	From SDZ high to PWM on (5)	-	300	-	ms

	Turn-off Time	t_{OFF}	From SDZ low to PWM off (5)	-	58	-	ns
	Class-D Output Offset Voltage (Measured Differentially)	$\|V_{OS}\|$	T_J=25°C, no input signal, Gain=26dB	-	1.5	10	mV
	Gate Drive Supply	GREG	SDZ=high, no input signal	3.2	3.4	3.6	V
	PWM Frequency	f_{PWM}	Selectable for AM avoidance	-	400	-	kHz
				-	500	-	
AC Characteristics	Power Supply Ripple Rejection	PSRR	V_{ripple}=200mV_{PP}, Gain=20dB, 1kHz, inputs AC-coupled to GND	-	-65	-	dB
	Output Power	P_O	PVDD=6V, R_L=2Ω, f=1kHz, <=1%THD+N	-	4.4	-	W
			PVDD=10V, R_L =2Ω, f=1kHz, <=1%THD+N	-	11.9	-	
			PVDD=14.4V, R_L =4Ω, f=1kHz, <=0.1%THD+N	-	8	-	
			f=1kHz, <=1%THD+N	-	12.3	-	
			PVDD=12V, R_L =8Ω, f=1kHz, <=10%THD+N	-	9.4	-	
	Total Harmonic Distortion + Noise	THD+N	f=1 kHz, Po=1W	-	0.03	-	%
	Output Integrated Noise Floor	V_n	T_J=25°C,20Hz to 20kHz, A-weighted filter, Gain=20dB	-	62	-	μV
	Signal to Noise Ratio	SNR	Max output at THD+N<1%, f=1kHz, Gain=20dB, A-weighted, PVDD=12V	-	102	-	dB
Protection	V_{DD} Undervoltage Lockout Threshold	V_{UVLO_RISE}	V_{DD} Rising to exit UVLO		3.9	4.3	V
		V_{UVLO_FALL}	V_{DD} Falling to enter UVLO	3.2	3.6	-	V
	V_{DD} Overvoltage Lockout Threshold	V_{OVLO_RISE}	V_{DD} Rising to enter OVLO	-	35.5	36.6	V
		V_{OVLO_FALL}	V_{DD} Falling to exit OVLO	32.4	33.8	-	V
	Thermal Shutdown Temperature	T_{SD}	(5)	-	150	-	°C
	Thermal Shutdown Hysteresis	T_{HYS}	(5)	-	15	-	°C
	Short Circuit Protection	I_{SC}	T_J=25°C (5)	-	6.8	-	A
	Overcurrent Protection	I_{OC}	T_J=25°C, full-bridge overload (5)	-	5	-	A
	DC Detection Time	t_{DCDET}	(5)	-	605	-	ms
	DC Detection Threshold (Output Differential Duty-cycle)		(5)	-	19	-	%
Load Diagnostics	Voltage to Detect a Short from OUT Pin(s) to Power			6	-	-	V
	Resistance to Detect a Short from OUT Pin(s) to Ground			-	-	50	Ω
	Open Load Detection Threshold		Including speaker wires	70	100	180	Ω
	Short Load Detection Threshold		Including speaker wires	0.6	1.2	1.8	Ω
I²C	SDA/SCL High-level Input Voltage			1.3	-	-	V
	SDA/SCL Low-level Input Voltage			-	-	0.5	V
	SDA High-level Output Voltage		$R_{PULL-UP}$=100kΩ to 3.3V	3	-	-	V
	SDA Low-level Output Voltage		3mA sink current	-	-	0.3	V

Note 1: Stresses beyond the “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: θ_{JA} is measured in the natural convection at T_A = 25°C on a high effective four layers thermal conductivity test board of JEDEC 51-7.

Note 3: The device is not guaranteed to function outside its operating conditions.

Note 4: Unless otherwise stated, limits are 100% production tested under pulsed load conditions such that $T_A \cong T_J$ = 25°C. Limits over the operating temperature range (See recommended operating conditions) and relevant voltage range(s) are guaranteed by design, test, or statistical correlation.

Note 5: Guaranteed by design or statistical correlation and not production tested.

I²C Timing Requirements for Control Port

Parameter	Symbol	Test Condition	Min	Max	Unit
SCL Frequency	f_{SCL}	No wait states		400	kHz
SCL and SDA Rise Time	t_r			300	ns
SCL and SDA Fall Time	t_f			300	ns
SCL High Duration Time	t_{WH}		0.6		μs
SCL Low Duration Time	t_{WL}		1.3		μs
SDA to SCL Setup Time	t_{S1}		250		ns
SCL to SDA Hold Time	t_{h1}(1)		0		ns
Free Time between Stop and Start Condition	t_{buf}		1.3		μs
SCL to Start Condition	t_{S2}		0.6		μs
Start Condition to SCL Hold Time	t_{h2}		0.6		μs
SCL to Stop Condition	t_{S3}		0.6		μs

Note 1: A device must internally provide a hold time of at least t_f for the SDA signal to bridge the undefined region of the falling edge of SCL.

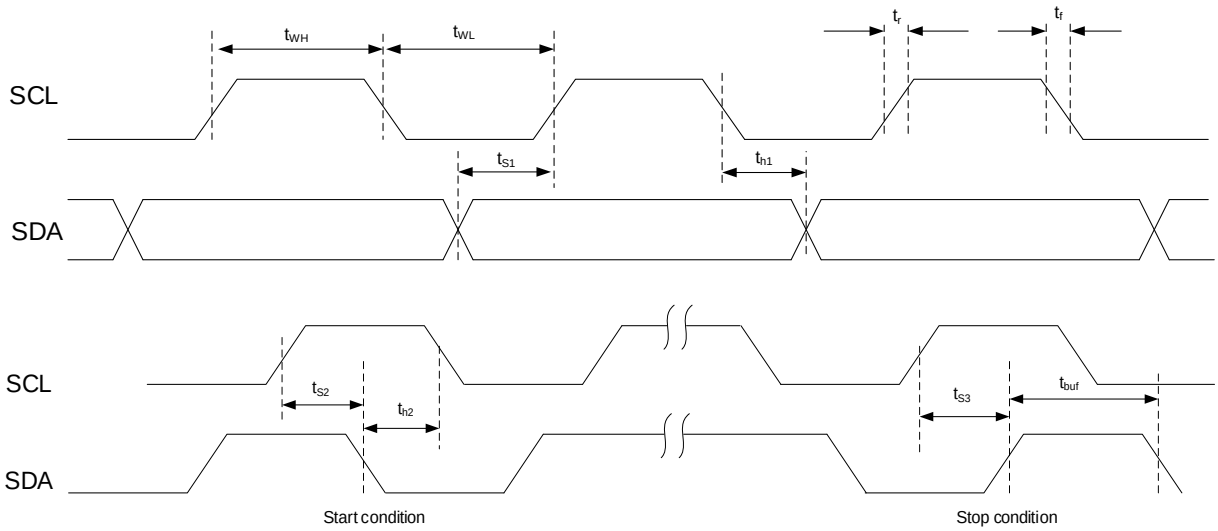
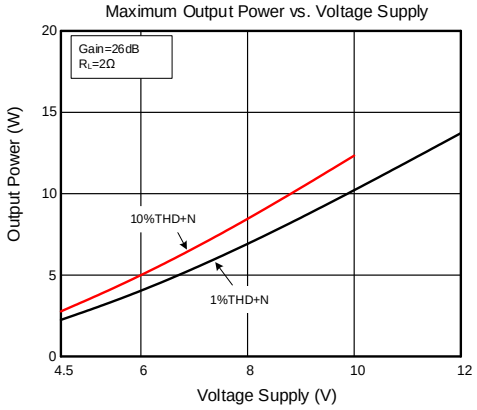
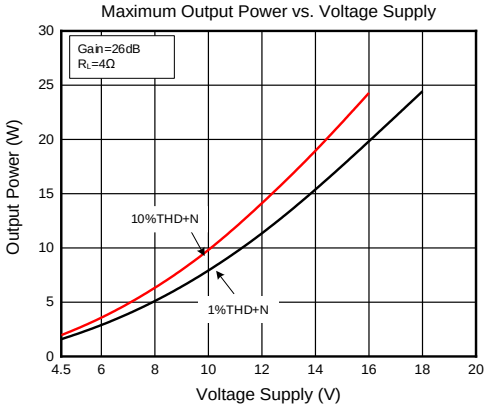


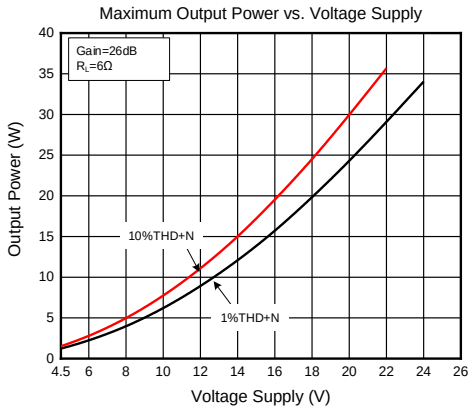
Figure 4. I²C Timing Diagram

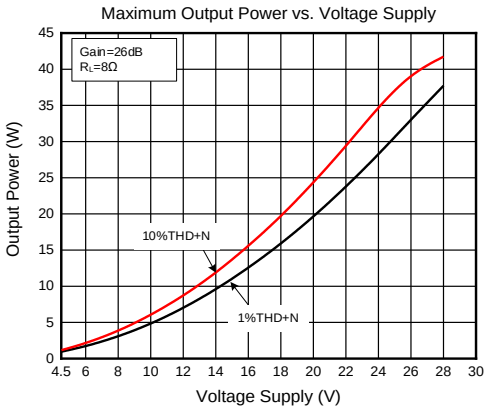
Typical Performance Characteristics

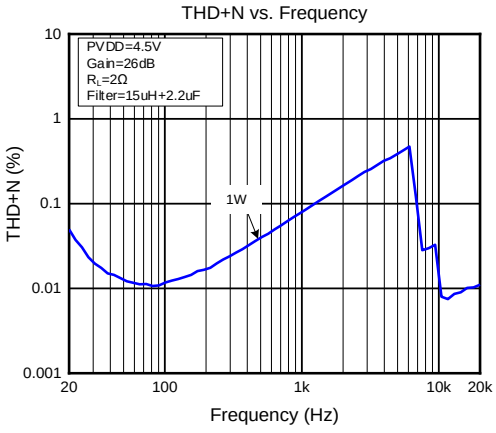
(All measurements taken at 1 kHz, unless otherwise noted.)

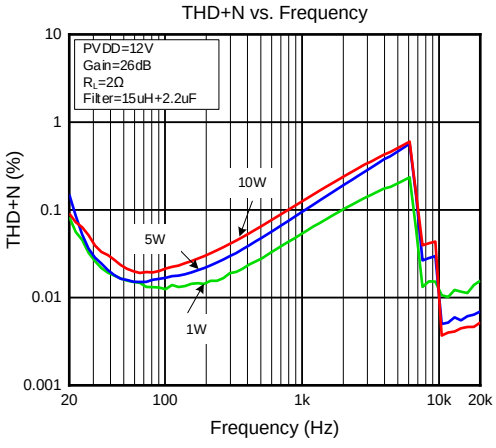


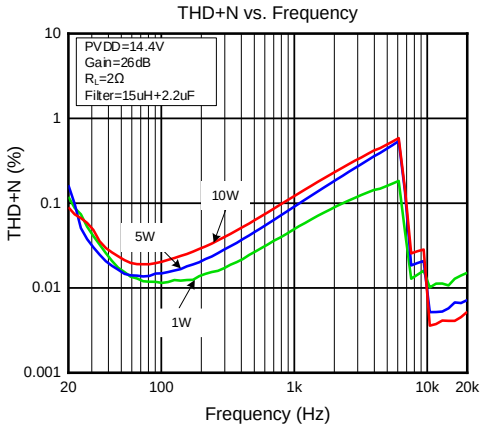


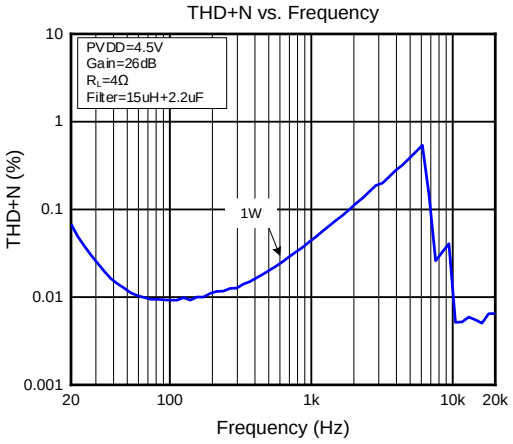


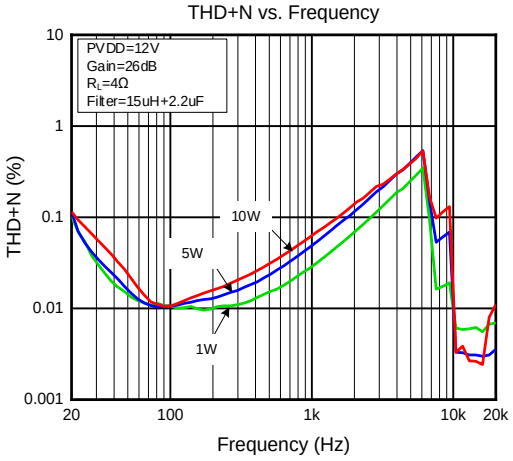


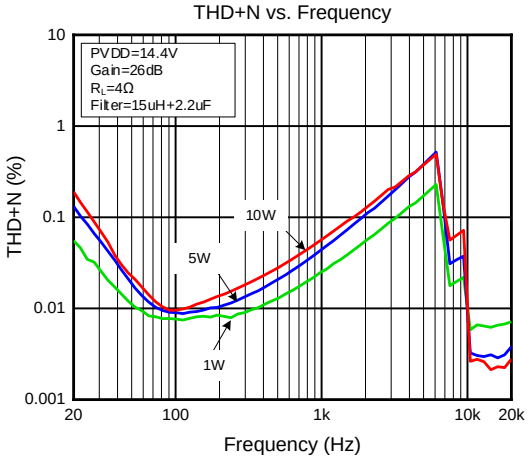


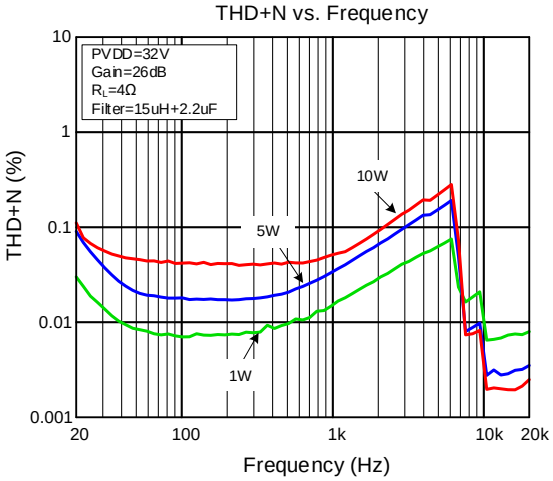


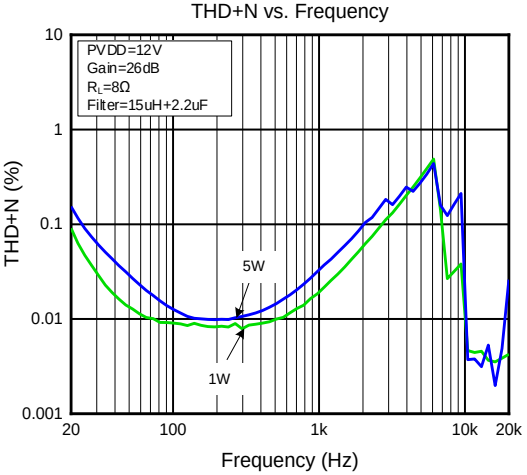




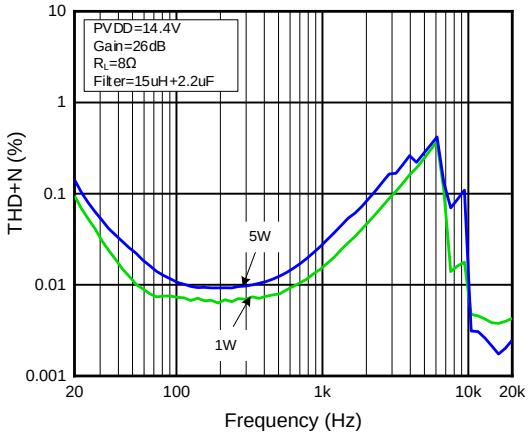








THD+N vs. Frequency



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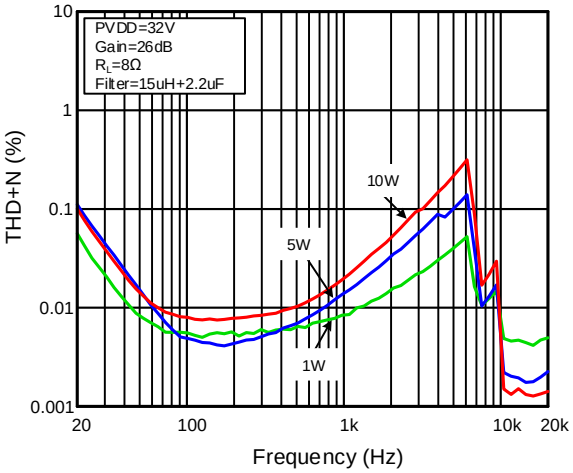
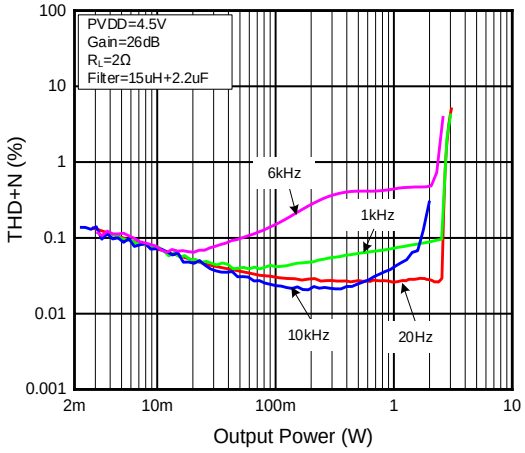


THD+N vs. Output Power



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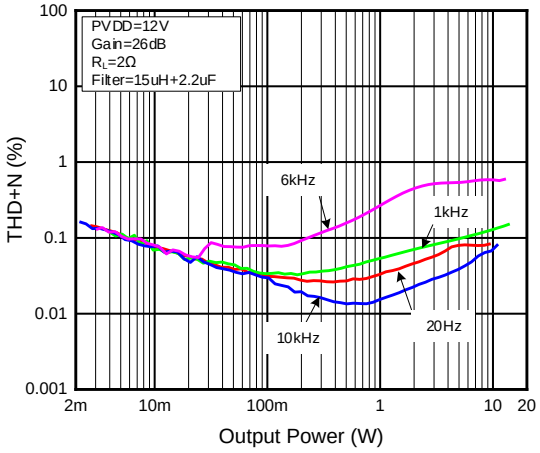

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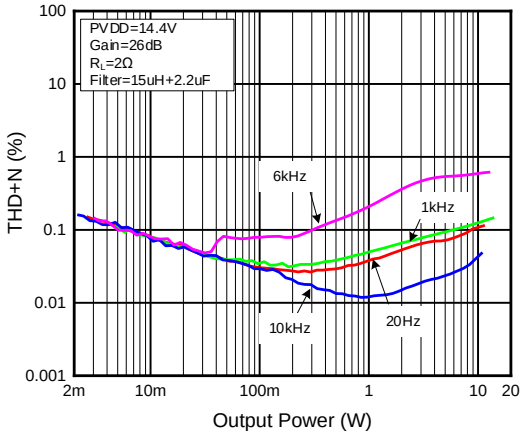

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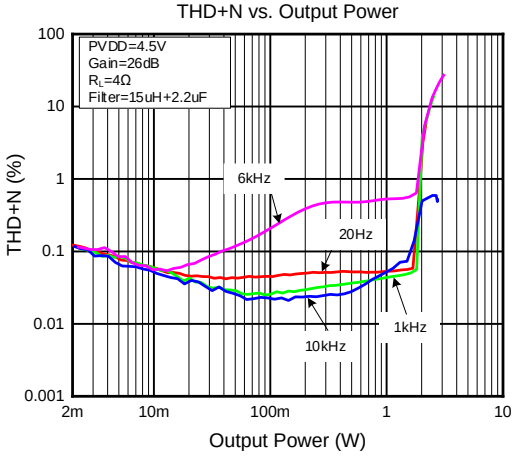

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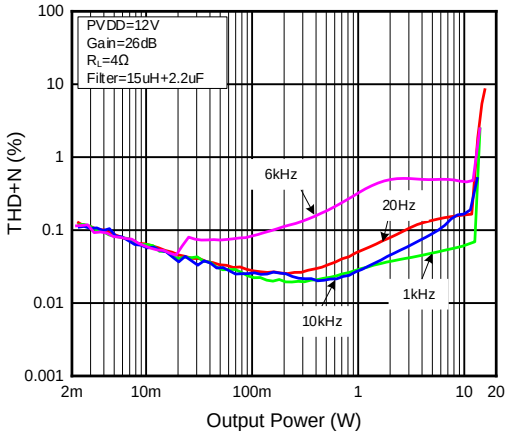

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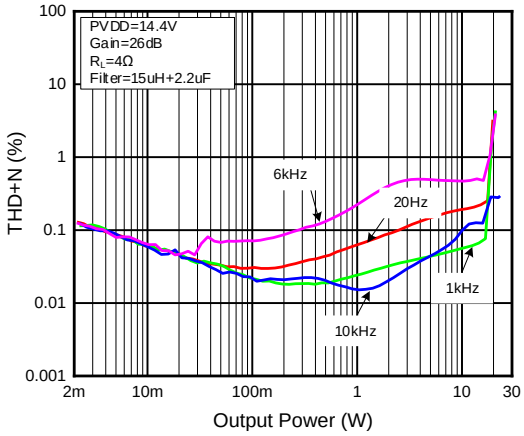

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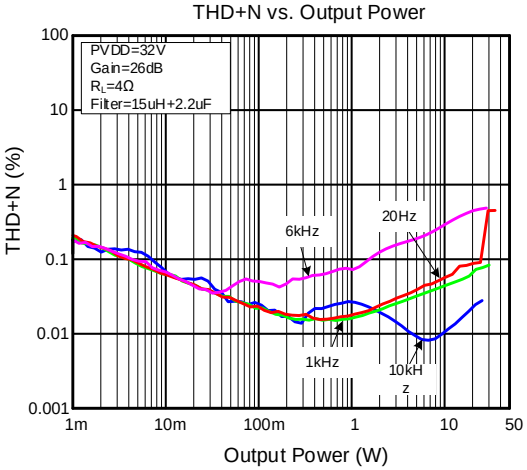

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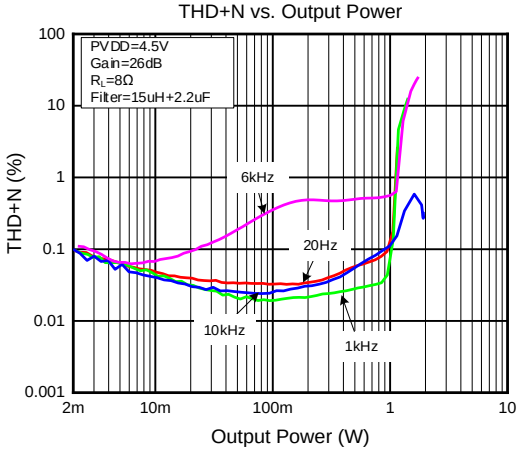

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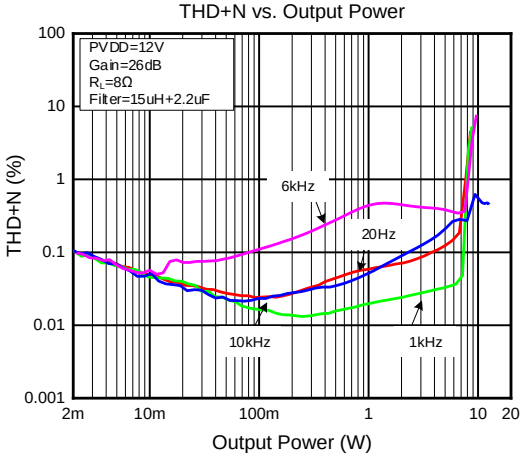

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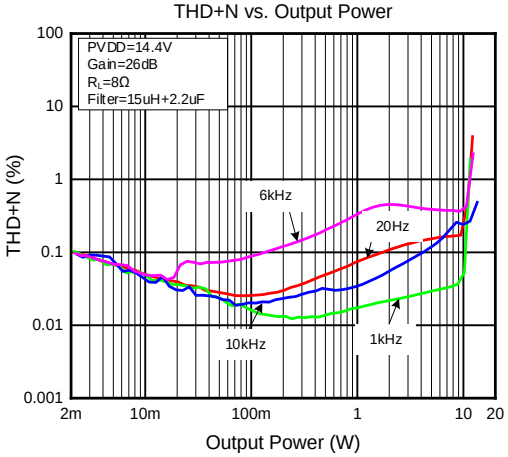

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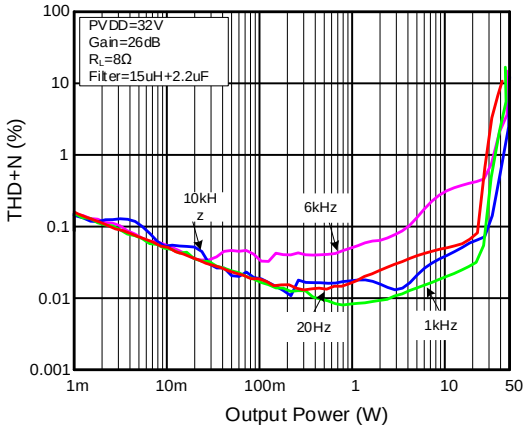
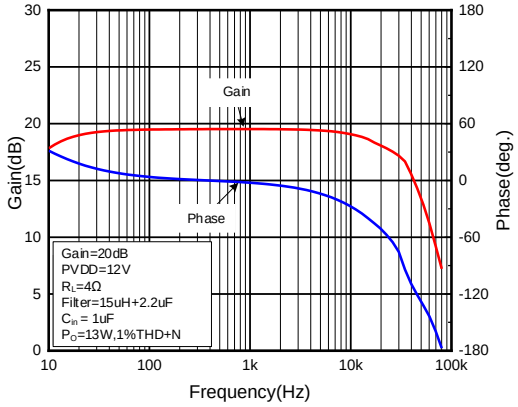


Gain/Phase vs. Frequency



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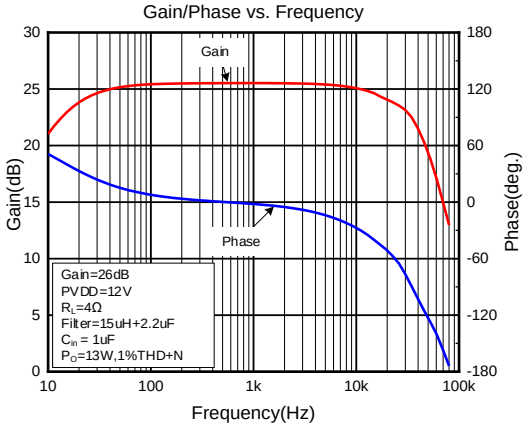
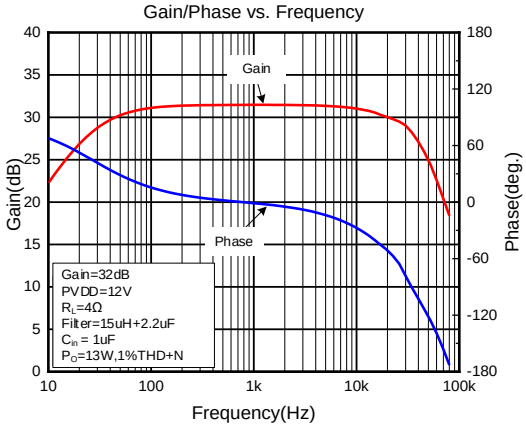
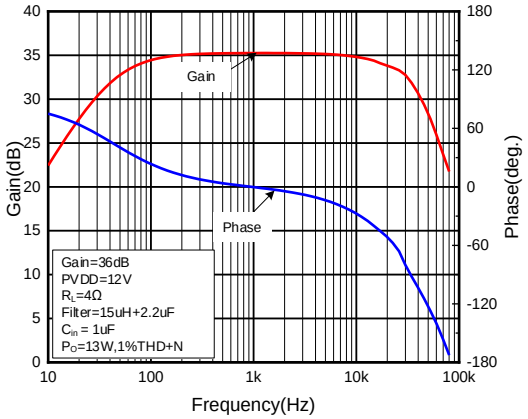


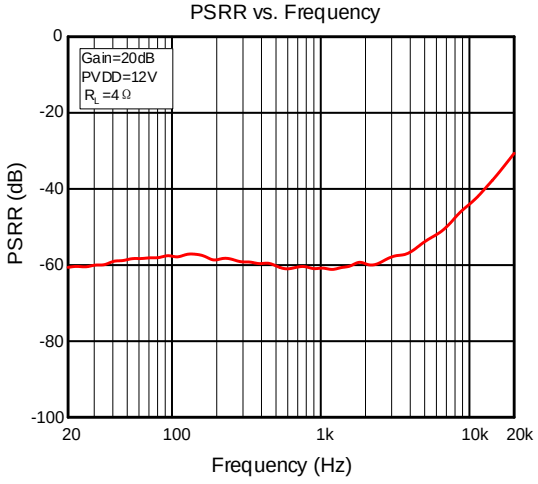
Gain/Phase vs. Frequency

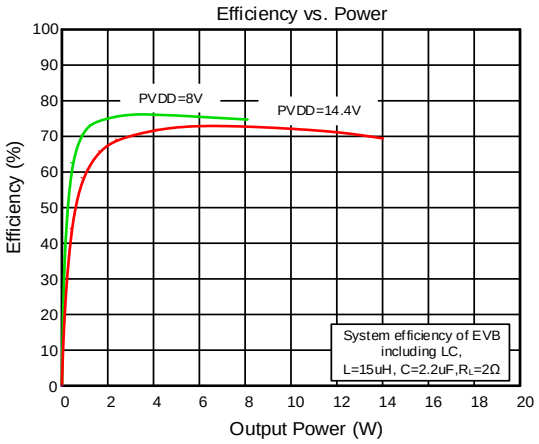


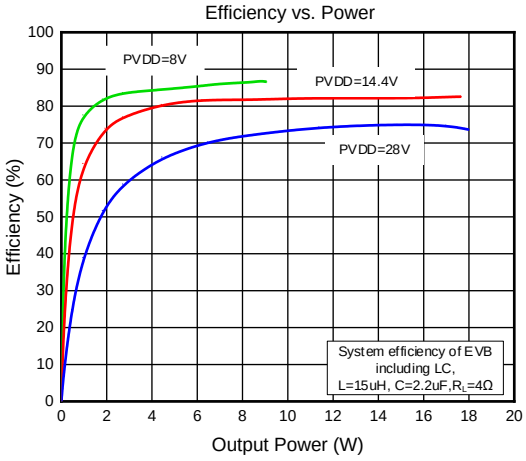
Gain/Phase vs. Frequency

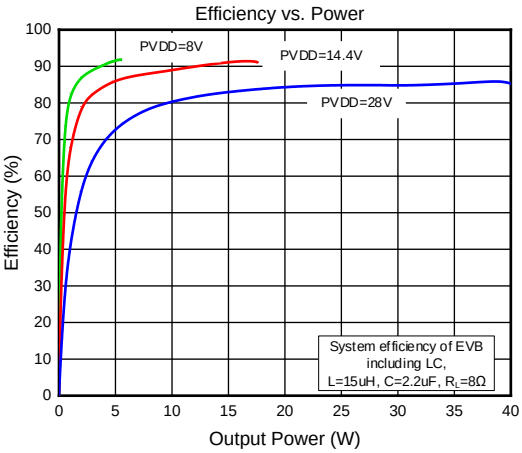


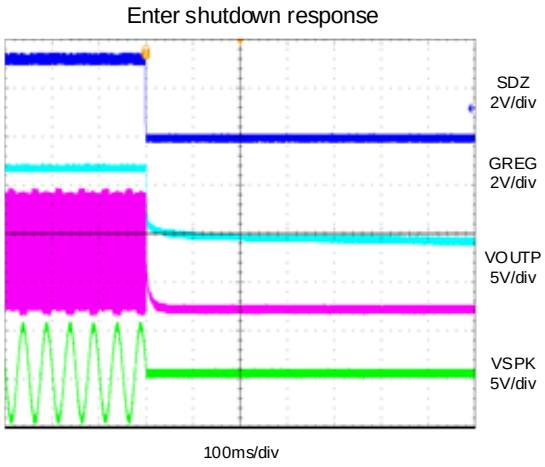
PSRR vs. Frequency

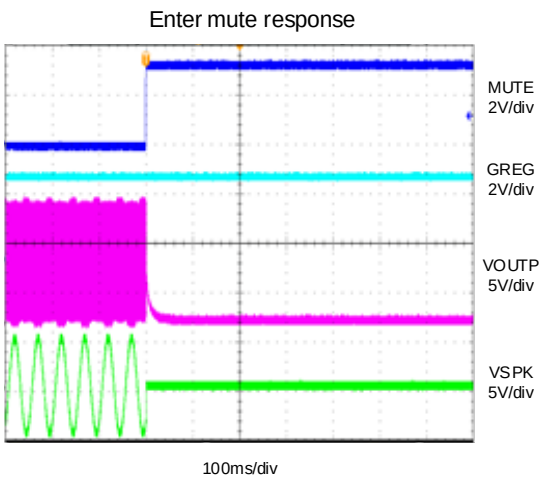


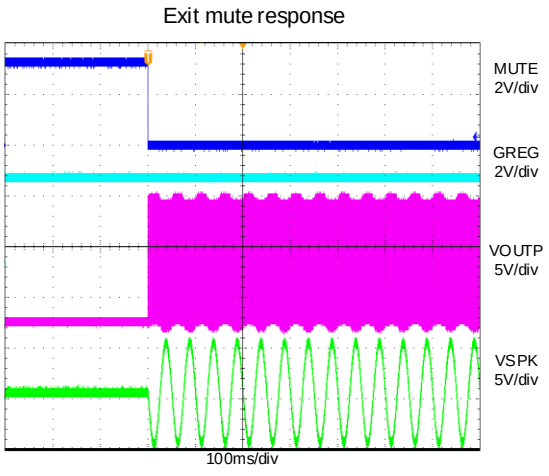












Detailed Description

The SY2A54508 is a high-performance mono analog audio amplifier IC used in the automotive applications which is AEC-Q100 qualified with temperature grade 1 (-40°C to 125°C), HBM ESD classification level H2, and CDM ESD classification level C3 per AEC-Q100-011 Rev.D.

Gain Setting and Input Resistance

The gain of the SY2A54508 is set by bit 7 and bit 6 of Control register (0x03). Configuring the amplifier gain can be achieved by varying the input resistors inside the amplifier. The gains and the corresponding input resistance are listed in Table 1. There is ±10% variation in input resistance from production variation. The input resistance of the amplifier varies from a minimum of 4.6kΩ±10% to a maximum of 30kΩ±10% when the gain is changed. As a result, if a single capacitor is used in the input high-pass filter, the –3 dB cutoff frequency may change when changing gain steps.

Table 1. Gain and Input Impedance

Amplifier Gain (dB)	Input Impedance (kΩ)
20	30
26	15
32	7.5
36	4.6

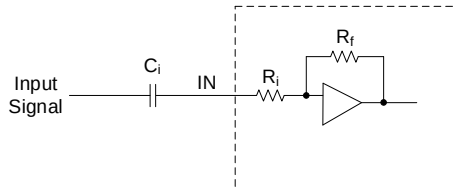


Figure 5. Input Impedance

Use formula 1 to calculate the –3dB frequency. Use the values listed in Table 1 for Ri.

$$f_c = \frac{1}{2\pi \cdot R_i \cdot C_i} \quad (1)$$

Input Capacitor, Ci

The performance at low frequency (bass) is affected by the corner frequency (fc) of the high-pass filter composed of input resistor (Ri) and input capacitor (Ci), as determined by the formula (1). The AC-coupling capacitor allows the amplifier to automatically bias the input signal to an optimum DC level.

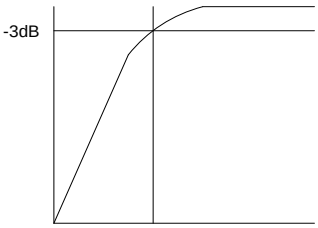


Figure 6. -3dB Frequency of HPF

The resistance of input resistors is different at different gain settings. Consider the specification calls for a flat bass response down to 20Hz. Formula 1 is reconfigured as formula 2.

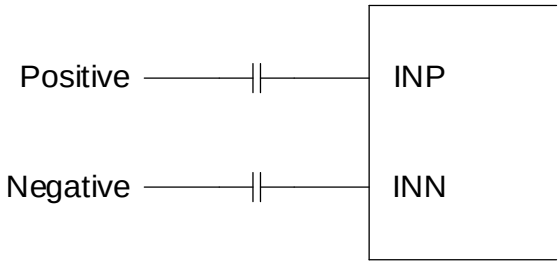
$$C_i = \frac{1}{2\pi \cdot R_i \cdot f_c} \quad (2)$$

Choose Ci such that the filter corner frequency s well below the lowest frequency of interest. Typically, a 1μF ceramic capacitor is suggested. For best audio quality, use capacitors with low-voltage coefficient dielectrics, such as tantalum or ceramic.

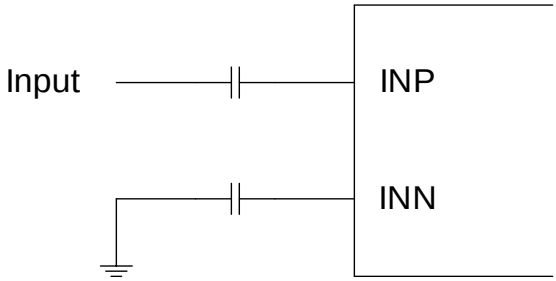
Differential Input

The SY2A54508 has an internal fully differential input structure which can provide an improved common mode rejection ratio. When using the SY2A54508 with a differential input source, connect the positive lead of the audio source to the INP input and the negative lead of the audio source to the INN input.

The SY2A54508 can also be used with a single-ended source. Connect AC-ground to the INP or INN inputs through a capacitor equal in value to the input capacitors used on INN or INP and apply the audio source to either input. The input signal connections are shown in Figure 7.



(a) Differential Input



(b) Single-ended Input

Figure 7. Input Signal Connection

SDZ and Mute Operation

The SY2A54508 offers a shutdown mode designed to reduce supply current during idle periods for power conservation. Pulling down the SDZ pin, the amplifier enters shutdown mode, and the internal LDO is disabled. The power MOSFETs are set to Hi-Z state for low power dissipation. The peripheral I^2C device can't be accessed in this mode. Pulling the SDZ pin high, the amplifier will exit shutdown mode, perform load diagnostics, and start driving the speaker, as shown in Figure 9.

The SY2A54508 has a mute mode to silence the amplifier output. This mode is enabled when the MUTE pin is set high. Pulling down the MUTE pin returns to normal play mode after less than 20μs.

Modulation Scheme

The SY2A54508 uses BD mode modulation scheme, as shown in Figure 8. In BD mode, the two half-bridges switch in phase, but the input signal for the modulators is inverted. Each output is switching from 0V to the power supply voltage. When the OUTP and OUTN are in phase and there is no input signal, there is almost no current into the speaker. When output voltages are positive, the duty-cycle of OUTP is greater than 50% and OUTN is less than 50%. When output voltages are negative, the duty cycle of OUTP is less than 50% and OUTN is greater than 50%. The voltage across the speaker is at 0V throughout most of the switching period, reducing the switching current, which reduces any I^2R losses in the load.

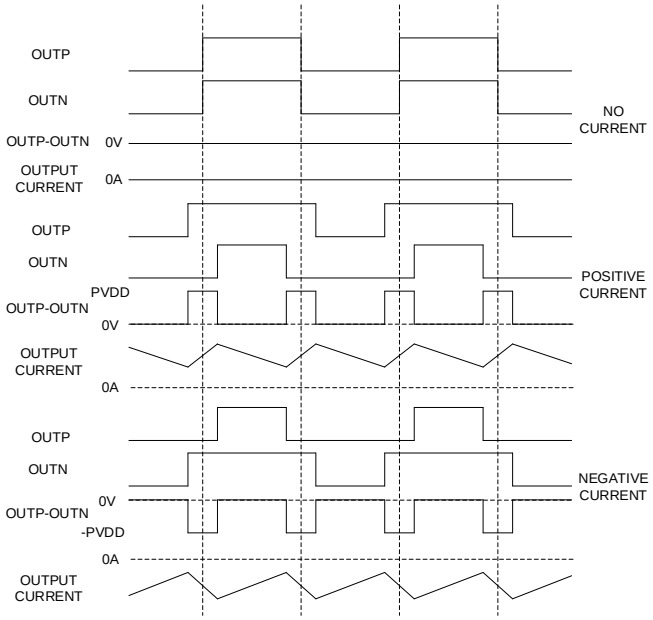


Figure 8. BD Mode Modulation

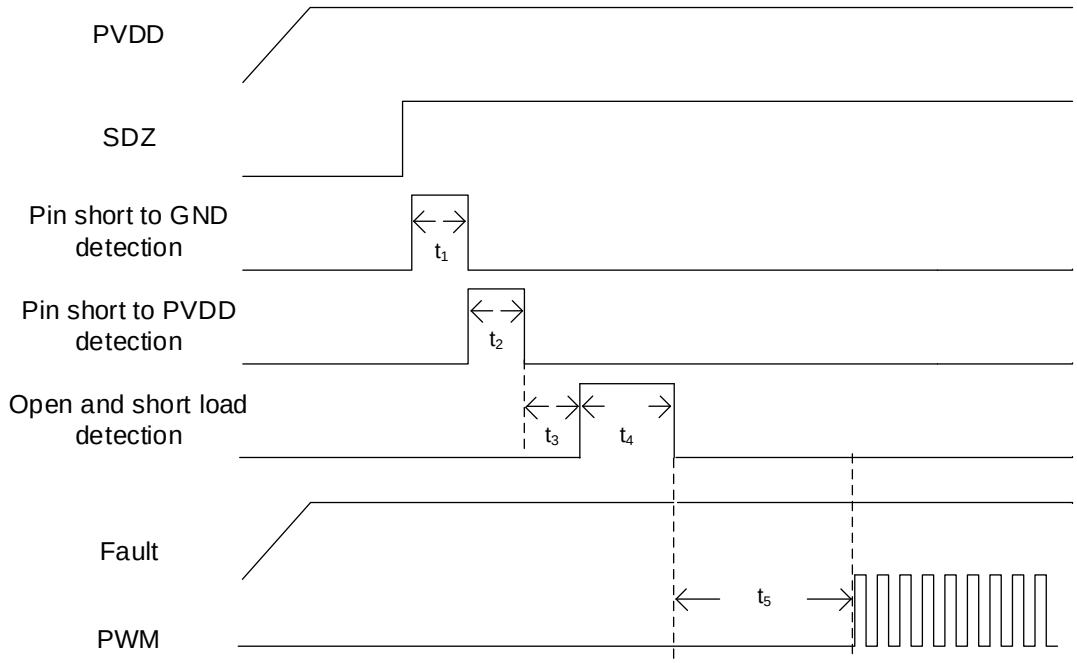
Load Diagnostics and Timing

The SY2A54508 has a built-in load diagnostic function designed for detecting the status of output connections at power up. It includes the following diagnostics:

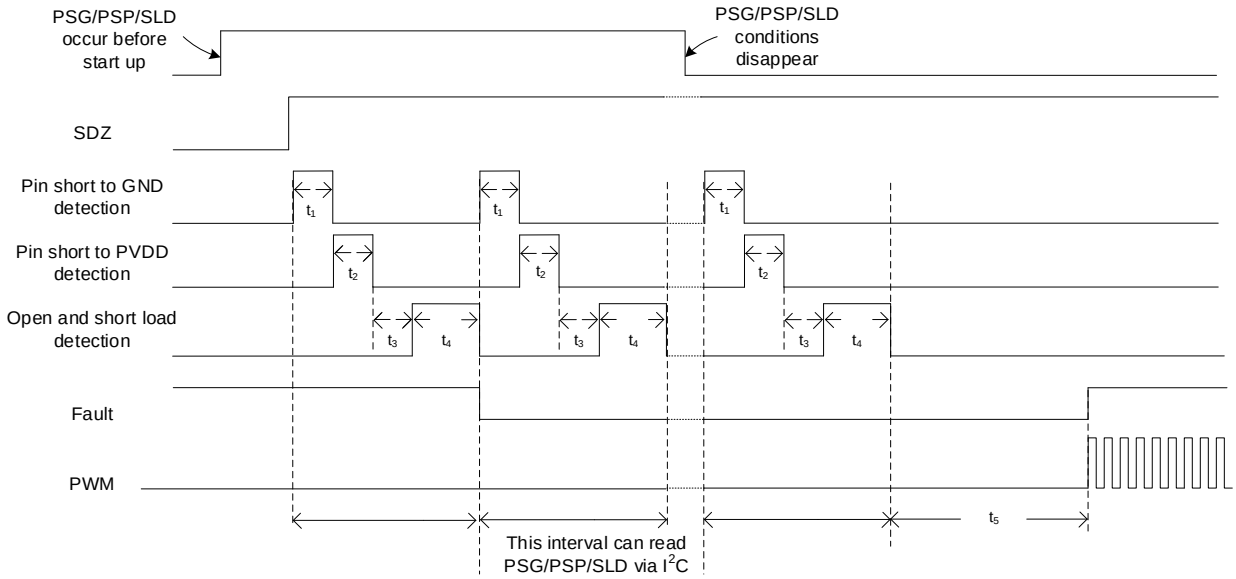
- Output short to Ground (PSG)
- Output short to Power (PSP)
- Shorted load (SLD)
- Open load (OLD)

The diagnostics result is reported by the Fault register (0x01) and the Status and Load Diagnostic register (0x02). The load diagnostic function will run after pulling SDZ pin high or after auto recovery from overcurrent, direct current, overtemperature, undervoltage, or overvoltage errors. The device will diagnose sequentially whether the output is a short to GND, short to PVDD, the load is shorted, and the load is open. If a fault is diagnosed, subsequent detection will be skipped until next cycle. The load diagnostic biases the output, which therefore requires limiting the capacitance value for proper functioning. The load diagnostic takes approximately 150ms (typical) to detect the four-fault states, and then wait 150ms (typical) for the control system to acquire an LD result. Except for open load error, any other fault conditions will put the output in a Hi-Z state and the FAULTZ pin be pulled down. If there is no error in load diagnostics, the amplifier will start to output PWM based on the audio signal. With the default I^2C settings, bit 5 of Control register 2 (0x04) is 0. The I^2C report of PSG (PSP) of OUTP and OUTN is provided. Independent of a PSG or PSP error being detected, bit 1 (bit 0) of register 0x02 will be 1. The PSG (PSP) detection of OUTP and OUTN is independent, so the I^2C report of these two errors can be separated when bit 5 of Control register 2 (0x04) is 1. Bit1 (bit 0) of register 0x02 represents a PSG (PSP) error on OUTP, and bit 6 (bit 7) of register 0x04 will represent PSG (PSP) error of OUTN, respectively.

The timing sequence of load diagnostics is shown in Figure 9.



(a) Normal or OLD



(b) PSG/PSP/SLD Continuous Detection

t_1: PSG detection time, typical 3ms;

t_2: PSP detection time, typical 3ms;

t_3: interval time, typical 3ms;

t_4: OLD/SLD detection time, typical 141ms;

t_5: wait time, typical 150ms.

Figure 9. Load Diagnostics Timing

In addition, if the SY2A54508 is used in an eCall system, where load diagnostic will run all the time unless an emergency happens, to account for the timing variation, the recommended SDZ pull down time is at 215ms±15ms, after the SDZ is pulled up, which is appropriate to avoid entering play mode.

PLIMIT

The PLIMIT circuit can limit the output peak-to-peak voltage to a set level which is lower than supply voltage. Limiting the amount of speaker current will limit the output power. Limiting the duty-cycle to a fixed maximum value can achieve this function. The limited output voltage can be set using bits 3-5 in the Control register (0x03). This control scheme provides seven selectable output voltages.

I²C Serial Control Interface

The SY2A54508 uses the I²C bus transfer protocol to communicate with the system. Two wires, serial data and serial clock, carry information between the devices connected to the bus. Each device is recognized by a unique 7-bit address and can operate as either a transmitter or a receiver. The controller device initiates a data transfer and provides the serial clock on the bus. The SY2A54508 is always an I²C peripheral device.

The following functions can be controlled by the I²C interface:

- Changing gain setting to 20 dB, 26 dB, 32 dB, or 36 dB
- Controlling PLIMIT peak voltage value
- Reporting load diagnostic results
- Reporting fault protection
- Changing switching frequency for AM radio interference avoidance

The I²C bus can support 100kHz and 400kHz data transfer rates for a single-byte and multi-byte read/write transactions. Multiple controllers and wait state insertion are not possible. The device address of the SY2A54508 is 0xD8.

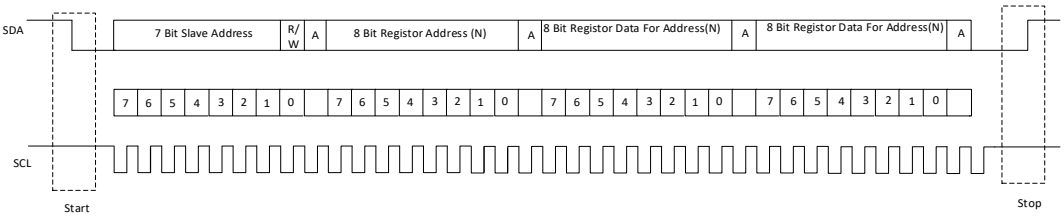


Figure 10. Typical I²C Sequence

Single and Multiple Byte Transfers

From register addresses 0x01 to 0x04, the I²C serial port control interface offers single-byte and multi-byte read/write operations.

Only when the controller device continues to acknowledge a data byte, the DAP responds to the command one byte at a time during multi-byte read operations, incrementing the read/write address pointer. If a particular register address does not contain 8*N bits, the unused bits will be read as logical 0.

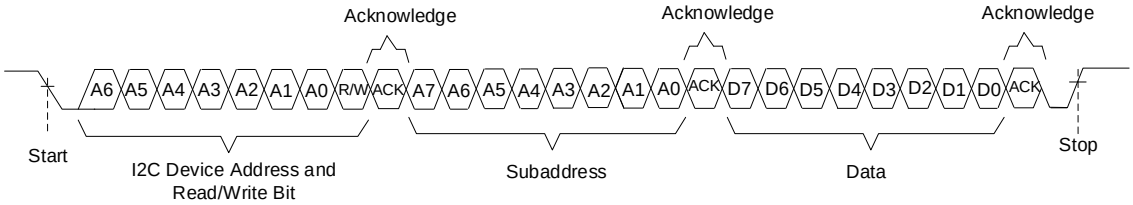


Figure 11. Single Byte Write Transfer

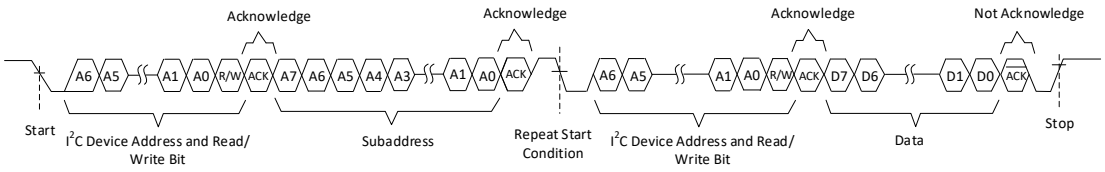


Figure 12. Single Byte Read Transfer

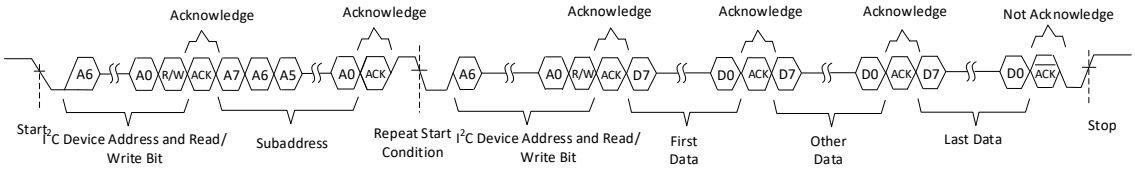


Figure 13. Multiple-Byte Read Transfer

BSN and BSP

The power output stage uses NMOSFETs for both high-side and low-side of the two half-bridges driving the outputs. Bootstrap capacitors are required to provide power for the high side MOSFETs of each output during normal operation. Typically, a 470nF ceramic capacitor, with a rated voltage of at least 16V, should be connected from OUTx to its corresponding bootstrap pin BSx. During each switching cycle, the bootstrap capacitors hold the gate-to-source voltage high enough to keep the high-side MOSFETs on.

GREG Supply

The GREG supply powers the gates of the output full bridge transistors. A 1μF capacitor connected between this pin and ground is recommended.

Spread Spectrum

The SY2A54508 supports spread spectrum clock to improve EMC performance. Spread spectrum is a technique of modulating the oscillator frequency with a slowly varying signal to broaden the switching spectrum, thereby reducing the spectral density of the EMI. The spread spectrum can be enabled using bit 4 and bit3 in the Control Register 2 (0x04). The frequency range Δf is ±25kHz (375kHz to 425kHz for PWM frequency 400kHz) and frequency of modulation profile (fm) can be set to 25.4kHz (0x04[4:3] = 2b'01), 12.7kHz (0x04[4:3] = 2b'10), and 6.4kHz (0x04[4:3] = 2b'11).

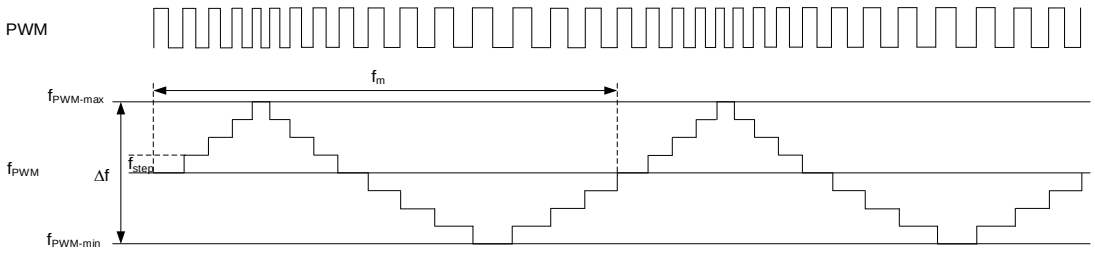
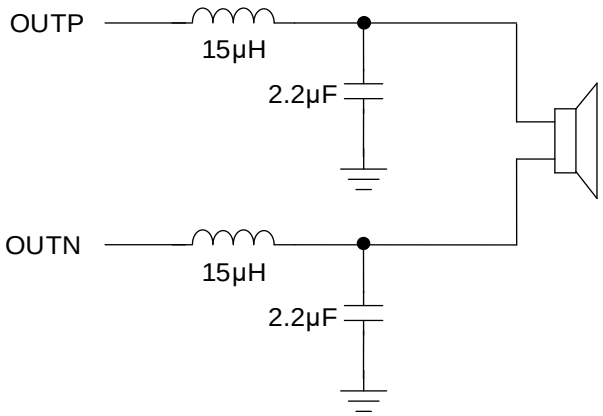


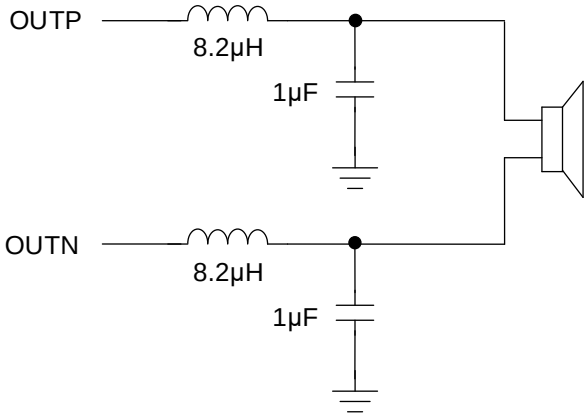
Figure 14. Spread Spectrum Operation

Output LC Filter

If the connections from the SY2A54508 to the speaker are not short or to satisfy the EMI requirements, it is recommended to add an output LC filter to eliminate the high-frequency emissions. The cutoff frequency of the LC filter must be less than the Class-D switching frequency to filter out switching frequency and its harmonics. The filter can be chosen according to a desired cutoff frequency and quality factor Q. Figure 15 shows two typical filter structures.



(a) Cutoff Frequency is 27kHz, Q=0.766, Speaker Impedance = 4Ω



(b) Cutoff Frequency is 55kHz, Q=0.698, Speaker Impedance = 4Ω

Figure 15. Typical LC Output Filter

Protection Circuits

The device is fully protected against short circuit, overtemperature, DC-detection, overvoltage, and undervoltage.

Overcurrent Protection (OCP)

To protect speaker drivers from overcurrent damage, the SY2A54508 has a built-in short-circuit protection circuit. When the wires connected to speakers are shorted to each other, shorted to GND, or to PVDD, overcurrent detectors will be activated. Once the overcurrent detectors are active, the amplifier outputs will enter a Hi-Z state, and the protection latch is engaged. The overcurrent fault is reported on the FAULTZ pin as a low state and in the I²C register. The latch will be cleared after 775ms, and the device will auto-recover if the short condition disappears.

Undervoltage Lockout (UVLO) and Overvoltage Lockout (OVLO)

When the PVDD voltage is lower than the undervoltage threshold or rises above the overvoltage lockout threshold voltage, the device will enter shutdown mode and internal logic resets. UVLO and OVLO events are be reported on the FAULTZ pin and in the Fault Register. Operation resumes when PVDD rises above the UVLO threshold with hysteresis or falls below OVLO threshold with hysteresis.

Overtemperature Protection (OTP)

If the internal junction temperature of the SY2A54508 becomes higher than 150°C, the device will enter shutdown mode and internal logic resets. This is not a latched fault. The overtemperature fault is cleared, and the amplifier returns to normal operation when the junction temperature falls by 15°C.

DC Detection

The SY2A54508 has a DC detection circuit to protect the speakers from DC current which might occur if the input capacitor fails or inputs are shorted on the printed circuit board. The detection circuit measures the difference of the PWM duty-cycle. If it exceeds 20% (for example, 60%, –40%) for more than 605ms at the same polarity, the amplifier will enter a Hi-Z state and the protection latch is engaged. A DC-detected fault is reported on the FAULTZ pin as a low state and in the I²C register. The device will auto-recover after 775ms, if the condition disappears.

Fault and Actions

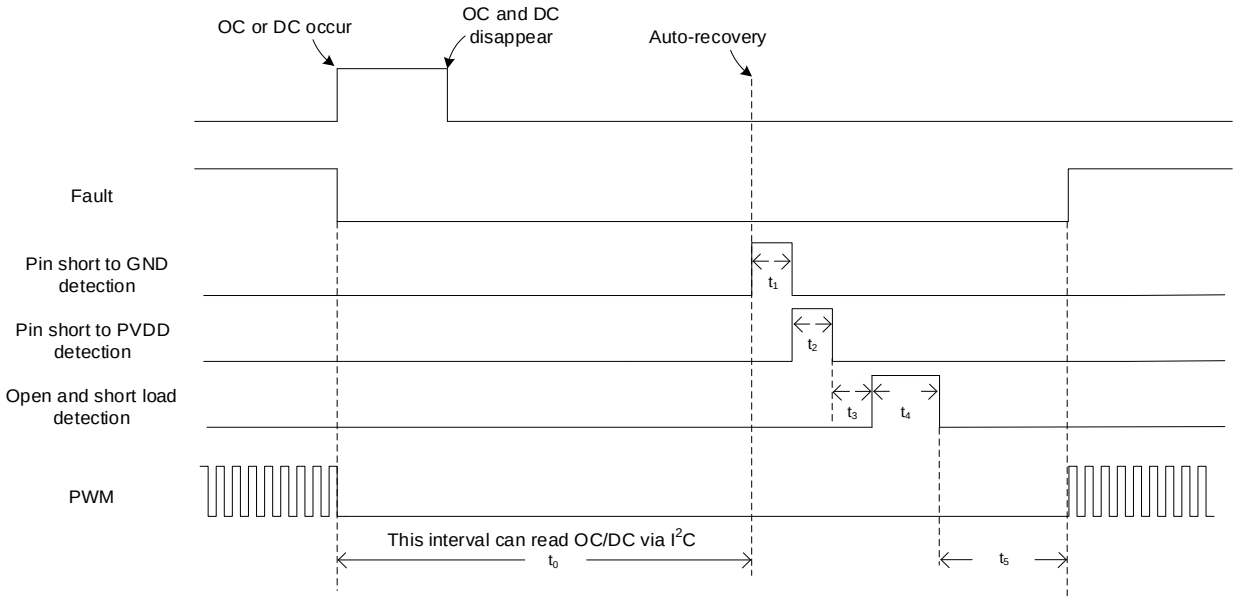
The following table lists all the faults and actions.

Fault Event	Fault Event Category	Monitoring Modes	Reporting Method	Action Result	Clearing
UV	Voltage fault	Except shutdown	I²C + FAULTZ pin	Hi-Z	Auto recovery when fault condition disappears
OV					
OTP	Thermal				
OC fault	Output channel fault	play			Auto recovery after 775ms and repeat load diagnostic until pass,
DC detect					

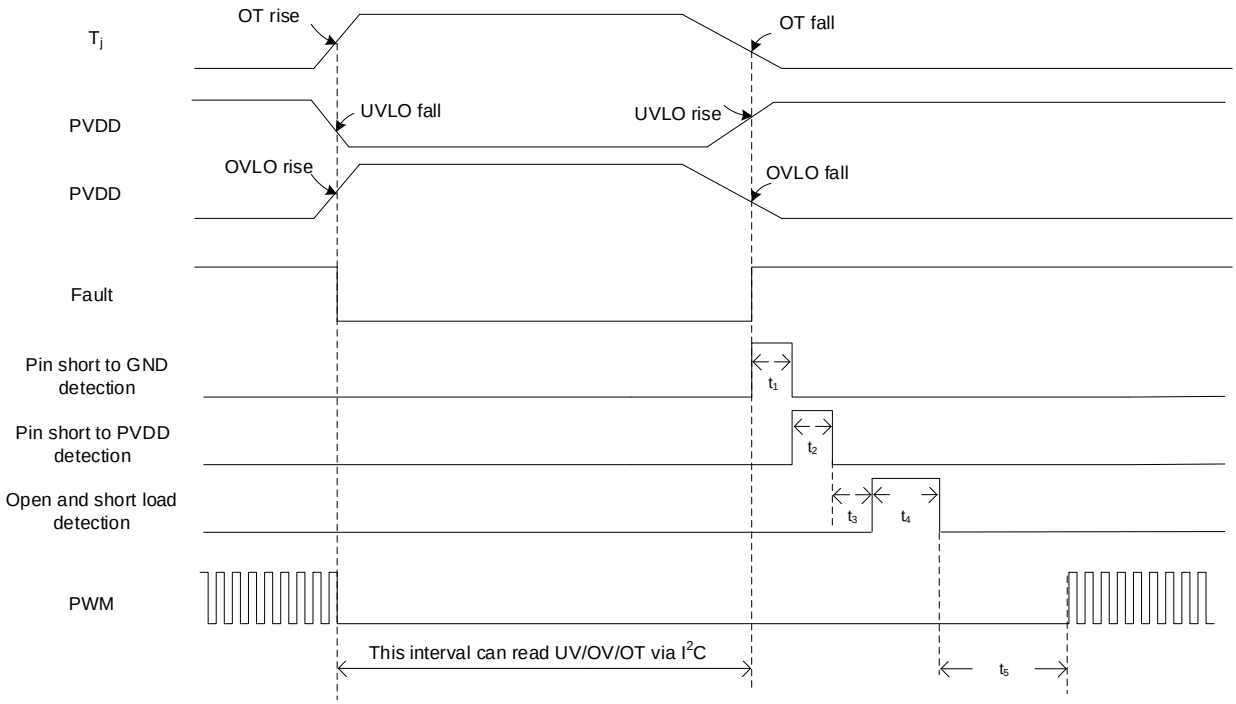
					then PWM out after 150ms
PSG PSP SLD	Diagnostic	Perform on start up or auto-recovery			Repeat load diagnostic until pass
OLD			I²C	Output normally	Cycle power or pull down SDZ

Auto-recovery

The timing of auto-recovery for overcurrent, direct current, overtemperature, undervoltage and overvoltage is shown in Figure 16.



(a) Auto-recovery from OCP/DCP



(b) Auto-recovery from OTP/UVLO/OVLO

t_0: auto-recovery time from OCP and DCP, typical 775ms;

t_1: PSG detection time, typical 3ms;

t_2: PSP detection time, typical 3ms;

t_3: interval time, typical 3ms;

t_4: OLD/SLD detection time, typical 141ms;

t_5: wait time, typical 150ms.

Figure 16. Auto-recovery

Register Map

I²C Address									
Description	Fixed Address							Read/Write Bit	I²C Address
	MSB	6	5	4	3	2	1	LSB	
I²C Write	1	1	0	1	1	0	0	0	0xD8
I²C Read	1	1	0	1	1	0	0	1	0xD9

I²C Address Register Summary		
Description	R/W	Register Description
0x01	R	Latched Fault Register
0x02	R	Status and Load Diagnostic Register
0x03	R/W	Control Register
0x04	R/W	Control Register 2

Fault Register (0x01)								
D7	D6	D5	D4	D3	D2	D1	D0	Function Description
0	0	0	0	0	0	0	0	No faults, default value
-	-	-	-	-	-	-	1	Reserved
-	-	-	-	-	-	1	-	Reserved
-	-	-	-	-	1	-	-	A load-diagnostics faults has occurred
-	-	-	-	1	-	-	-	Overcurrent shutdown has occurred
-	-	-	1	-	-	-	-	PVDD undervoltage has occurred
-	-	1	-	-	-	-	-	PVDD overvoltage has occurred
-	1	-	-	-	-	-	-	DC offset protection has occurred
1	-	-	-	-	-	-	-	Overtemperature shutdown has occurred

Status and Load Diagnostic Register (0x02)								
D7	D6	D5	D4	D3	D2	D1	D0	Function Description
0	0	0	0	0	0	0	0	No diagnostic faults, default value
-	-	-	-	-	-	-	1	Output short to PVDD when 0x04 D5 is 0 OUTP short to PVDD when 0x04 D5 is 1
-	-	-	-	-	-	1	-	Output short to Ground when 0x04 D5 is 0 OUTP short to Ground when 0x04 D5 is 1
-	-	-	-	-	1	-	-	Open load
-	-	-	-	1	-	-	-	Shorted load
-	-	-	1	-	-	-	-	In a fault condition (OC/OT/DC/UV/OV)
-	-	1	-	-	-	-	-	Performing load
-	1	-	-	-	-	-	-	In mute mode
1	-	-	-	-	-	-	-	In play mode

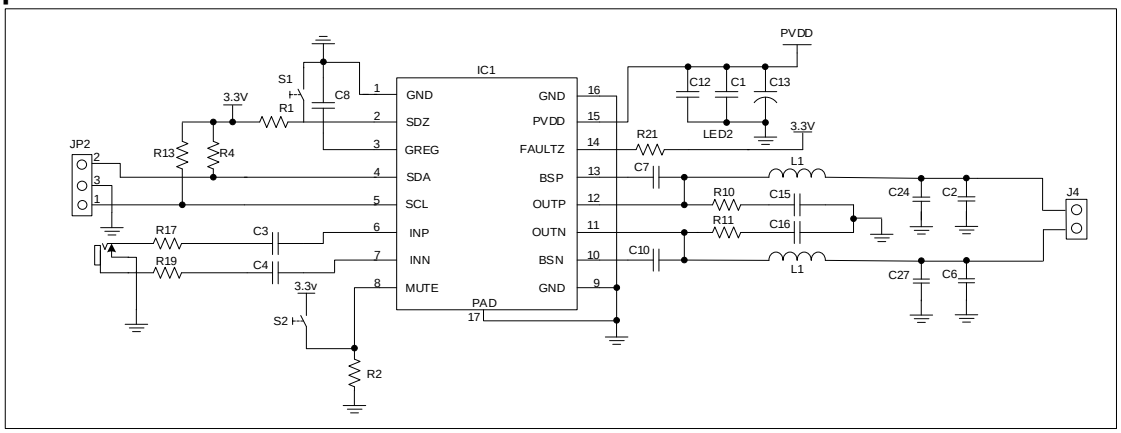
Control Register (0x03)								
D7	D6	D5	D4	D3	D2	D1	D0	Function Description
0	1	1	1	1	0	0	0	Default value. 26dB gain, switching frequency is 400kHz. Power limit function disable
-	-	-	-	-	-	-	1	Switching frequency set to 500kHz
-	-	-	-	-	1	1	-	reserved
-	-	1	1	0	-	-	-	Power limit to 14V peak output
-	-	1	0	1	-	-	-	Power limit to 11.8V peak output
-	-	1	0	0	-	-	-	Power limit to 9.8V peak output
-	-	0	1	1	-	-	-	Power limit to 8.4V peak output
-	-	0	1	0	-	-	-	Power limit to 7V peak output
-	-	0	0	1	-	-	-	Power limit to 5.9V peak output
-	-	0	0	0	-	-	-	Power limit to 5V peak output
0	0	-	-	-	-	-	-	20dB gain

1	0	-	-	-	-	-	-	32dB gain
1	1	-	-	-	-	-	-	36dB gain

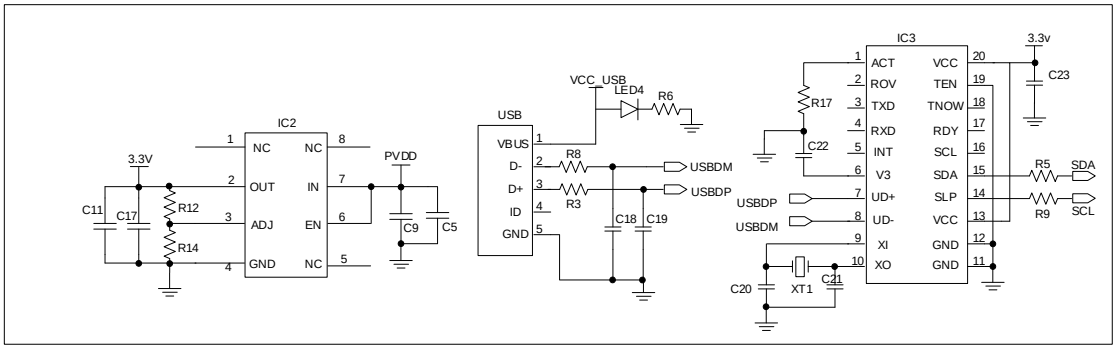
Control Register 2 (0x04)								
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Function Description**
0	0	0	0	0	0	1	0	Default. Not check PSG_N/PSP_N, no spread spectrum, fast edge
1	-	-	-	-	-	-	-	OUTN short to Ground when 0x04 D5 is 1
-	1	-	-	-	-	-	-	OUTN short to PVDD when 0x04 D5 is 1
-	-	1	-	-	-	-	-	Enable of PSG/PSP of OUTP and OUTN separation
-	-	-	-	-	-	-	1	reserved
-	-	-	-	-	0	0	-	Medium fast edge
-	-	-	-	-	1	0	-	Slow edge
-	-	-	-	-	1	1	-	Medium slow edge
-	-	-	0	1	-	-	-	25.5kHz fm with ±25kHz range
-	-	-	1	0	-	-	-	12.7kHz fm with ±25kHz range
-	-	-	1	1	-	-	-	6.4kHz fm with ±25kHz range

Schematic, BOM, and Layout

Typical Application Schematic



(a). SY2A54508 Peripheral Circuit



(b). USB to I²C Circuit (Optional)

Figure 17. SY2A54508 EVM Schematic

BOM List

Designator	Description	Part Number	Manufacturer
IC1	Analog class-D audio amplifier for automotive, TSSOP16E	SY2A54508HFP	Silergy
IC2	36V 300mA LDO Regulator, SO8E	SA21345AFCA	Silergy
IC3	USB Bus Convert chip, SSOP20	CH341T	
J1,J4	Connector, B2PS-VH(LF)(SN)		
J2	Header, XH2.54-3P		
J5	JACK-PJ307G		
LIN	JACK-RCA		
USB	MUSB-05-F-AB-SM-A		
LED4	LED, Green, SMD(0805)		
XT1	Oscillator, 12MHz		
C1,C5	Ceramic Capacitor, 10uF/50V(1206)		
C11	Ceramic Capacitor, 10uF/10V(0603)		
C3,C4	Ceramic Capacitor, 1uF/16V(0603)		
C7,C10	Ceramic Capacitor, 470nF/16V(0603)		
C8	Ceramic Capacitor, 2.2uF/10V(0805)		
C9,C12	Ceramic Capacitor, 100nF/50V(0603)		
C17,C22,C23	Ceramic Capacitor, 100nF/10V(0603)		
C15,C16	Ceramic Capacitor, 470pF/50V(0603)		
C18,C19,C20,C21	Ceramic Capacitor, 33pF/10V(0603)		
C24,C26	Configuration1:2.2uF/50V(0805)		
	Configuration2:1uF/50V(0805)		
C2,C6	NC		
C13	Electrolytic capacitor, 220μF/50V		

R1,R21	Resistor,100k(0603)		
R5,R7,R17,R19	Resistor,0Ω(0603)		
R3,R8	Resistor,10Ω(0603)		
R2,R4,R6,R7,R13	Resistor,4.7k(0603)		
R10,R11	Resistor,5.6Ω(0805)		
R16	Resistor,360K(0805)		
R23,R24	NC		
L1	Configuration1:15μH		
	Configuration2:8.2μH		
S1,S2	Light Touch Switches, SMD, 3.5mmx2.9mm	EVPAA202K	

Power Supply Recommendations

Because of the power loss on the traces between the device and the decoupling capacitors, the decoupling capacitors should be placed closely to PVDD and GND to reduce any parasitic resistance or inductance. A low ESR ceramic capacitor, typically 1nF, is suggested for high frequency noise rejection. For mid-frequency noise filtering, placing a capacitor with a value range between 0.1μF and 1μF as close as possible to the device PVDD pins is recommended. For low frequency noise filtering, a 220μF or greater value (tantalum or electrolytic type) is suggested.

PCB Layout Guidelines

To obtain optimal thermal dissipation and EMC performance of the SY2A54508, the PCB layout must follow the following guidelines:

- Use a separate short and thick power trace to the SY2A54508 to decrease voltage drop.
- The high-frequency decoupling capacitors of PVDD and GREG should be placed as close to the PVDD pin and GREG pin as possible. These capacitors can be connected to the thermal pad directly for good ground connection. These capacitors should be low ESR ceramic capacitors.
- The input capacitors should be placed as close as possible to the SY2A54508 INN and INP input pins. The input should be routed on the PCB as a differential trace to minimize noise coupling.
- The output LC filter should be placed as close to the output terminals as possible for the best EMI performance. Keep the current loop from each of the outputs through the inductor and the small filter cap, then back to GND as small and tight as possible. The size of this current loop determines its effectiveness as an antenna.
- The thermal pad must be soldered to the PCB for proper thermal performance and optimal reliability. The dimensions of the thermal pad and thermal land should be large enough for the application. Vias should be connected to a solid copper plane, either on an internal layer or on the bottom layer of the PCB.

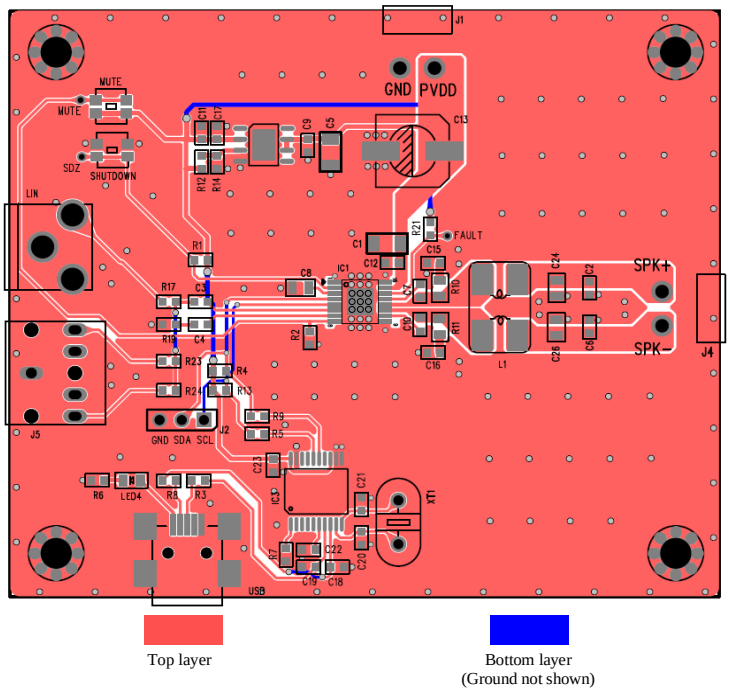
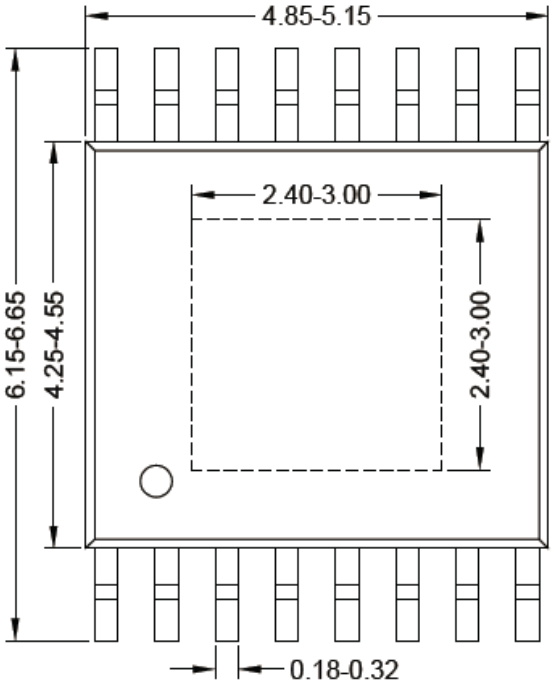
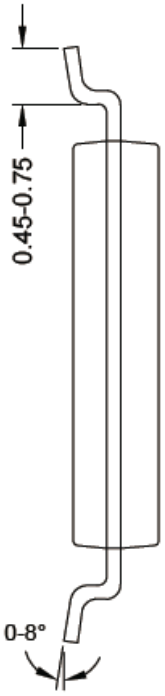


Figure 18. PCB Layout Example

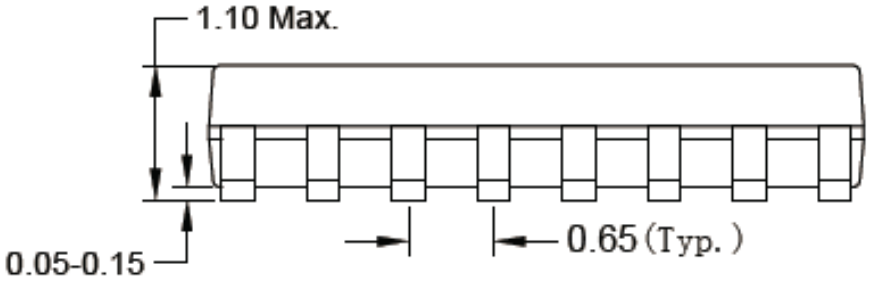
TSSOP16E Package Outline Drawing



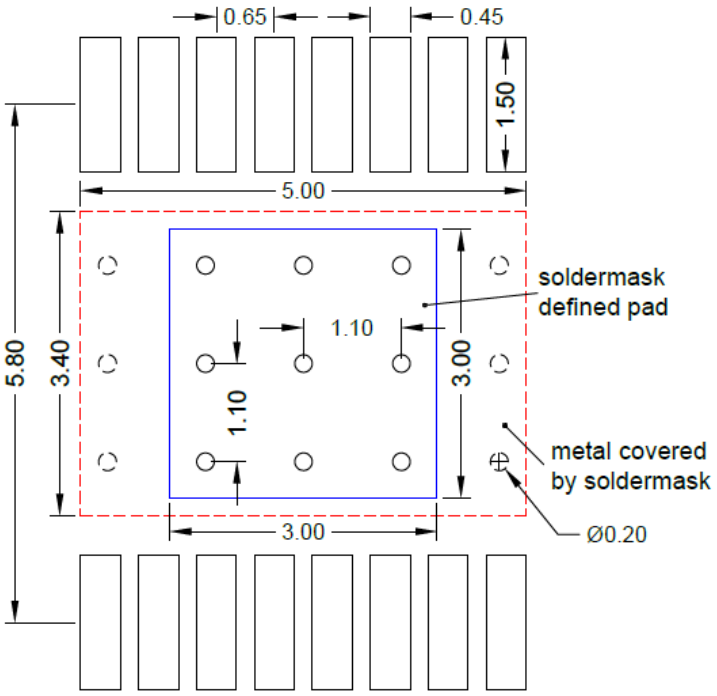
Top View



Side View A



Side View B



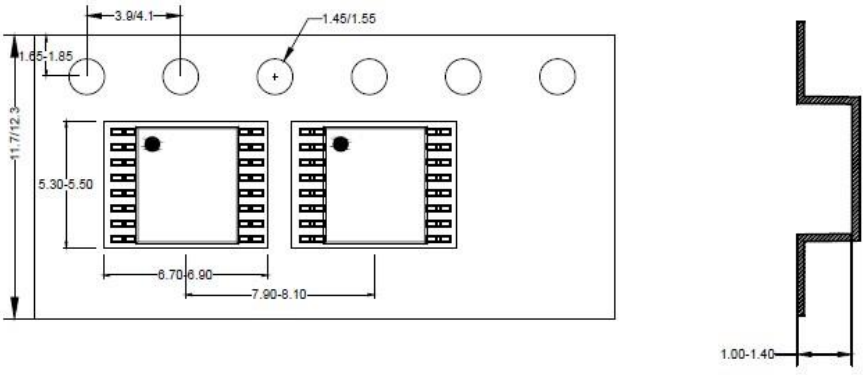
Recommended PCB Layout

(Reference only)

Notes: All dimensions in millimeters and exclude mold flash & metal burr.

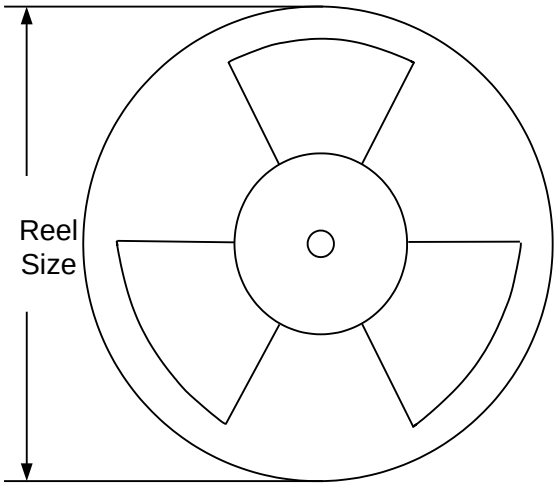
Tape and Reel Specification

TSSOP16E Tape Orientation



Feeding direction ▸

Reel Dimensions



Package Types	Tape Width (mm)	Pocket Pitch(mm)	Reel Size (Inch)	Trailer Length(mm)	Leader Length (mm)	Qty per Reel
TSSOP16E	12	8	13"	400	400	3000

Revision History

The revision history provided is for informational purposes only and is believed to be accurate; however, not warrantied. Please make sure that you have the latest revision.

Revision Number	Revision Date	Description	Pages changed
Rev 1.0	08/11/2024	Language improvements for clarity	
Rev 0.9A	07/08/2023	In Bom list, designator C7, C10 is changed from 220nF/50V to 470nF/16V	26
Rev 0.9	24/05/2023	Initial Release	

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