# SY2A23006

## 5.5V, 6A Single Synchronous Buck Converter

## General Description

The SY2A23006 synchronous buck converter has integrated power MOSFETs, an input voltage range of 2.8V to 5.5V, a configurable output voltage from 0.6V to $V_{IN}$, and a maximum load current capability of 6A. Under light load conditions, it can operate in either pulse width modulation (PWM) mode or pulse frequency modulation (PFM) mode. The soft-start time and 1.8MHz-3MHz switching frequency can be adjusted using external components.

The SY2A23006 also provides power good indication, undervoltage lockout (UVLO), short-circuit protection, cycle-by-cycle current limit protection, and thermal shutdown.

The SY2A23006 is available in a 2mm×3mm-9 pin QFN package.

## Key Features

- 2.8V to 5.5V Input Voltage Range
- Up to 6A Output Current
- External Adjustable Output Voltage with ±1.2% Reference Voltage Accuracy
- 1μA Shutdown Current (Typical)
- 38 μA Quiescent Current (Typical)
- Adjustable Switching Frequency of 1.8MHz to 3MHz
- PWM or PFM Operation Selectable in Light Load
- Adjustable Soft-Start Time
- 100% Duty-Cycle for Lowest Dropout
- Optional Frequency Spread Spectrum
- Cycle-by-Cycle Current Limit Protection
- Hiccup Mode Short-Circuit Protection
- Power Good Indicator
- Thermal Shutdown
- Compact QFN2×3-9 Package
- Automotive AEC-Q100 Grade 1 Certified

## Applications

- Digital Cockpit
- Advanced Driver Assistance System (ADAS)
- Surround View ECU
- Other Automotive Electronic Equipment

## Typical Application Circuit

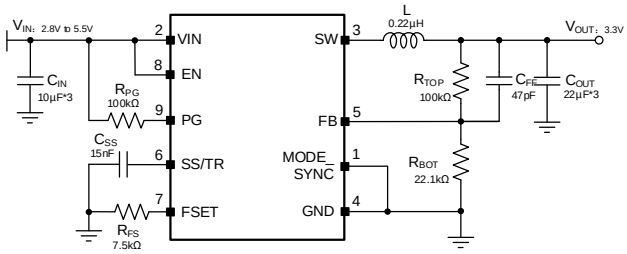


*Figure 1. Schematic Diagram*

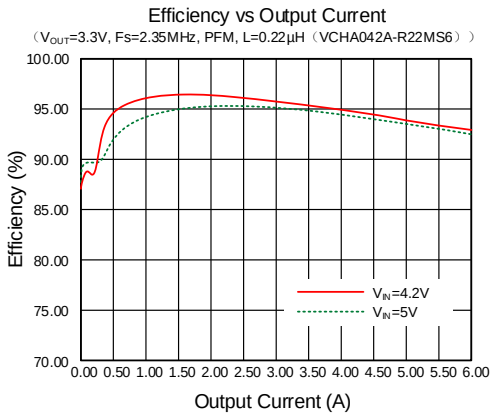


*Figure 2. Efficiency vs Output Current*


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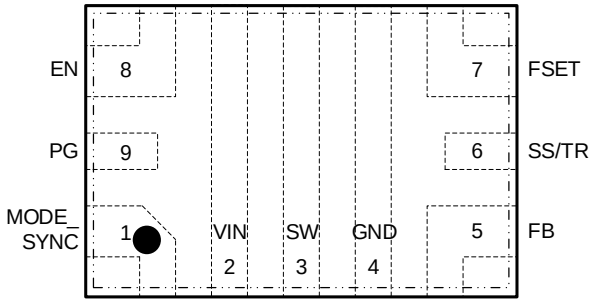
## Ordering Information

| Ordering Part Number | Package Type | Top Mark |
|---|---|---|
| SY2A23006XHQ | QFN2×3-9<br>RoHS-Compliant and Halogen-Free | **FHD*xyz*** |

***x = year code, y = week code, z = lot number code***

## Pinout (top view)




(QFN2×3-9)

## Pin Description

| Pin No | Pin Name | Pin Description |
|---|---|---|
| 1 | MODE_SYNC | Mode control and frequency synchronization pin. Under light load conditions, the device is in forced CCM mode when the pin is pulled high and in PFM mode when this pin is pulled low. The switching frequency can also be synchronized to an external clock applied to this pin. There is no internal pulldown resistor. Do not leave this pin floating. |
| 2 | VIN | Power input pin. |
| 3 | SW | Switching node. |
| 4 | GND | Ground. |
| 5 | FB | Output voltage feedback pin. The output voltage reference is 0.6V. |
| 6 | SS/TR | This is a dual-purpose pin.<br>SS: Soft-start time control pin. Connect this pin to GND with a ceramic capacitor to define the output voltage rise time.<br>TR: Tracking and sequencing. Allows output voltage to follow the voltage applied at this pin in both directions (up and down) in forced PWM mode. |
| 7 | FSET | Switching frequency, compensation of the control loop, and internal clock frequency modulation configuration pin. Connect this pin to GND with a resistor to configure these parameters. There is no internal pulldown resistor. Do not leave this pin floating. |
| 8 | EN | Device enable pin. There is no internal pulldown resistor. Do not leave this pin floating. |
| 9 | PG | Power good pin. Open-drain output. A pullup resistor is required (100kΩ, for example). Can be connected to GND or left floating if not used. |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## Block Diagram

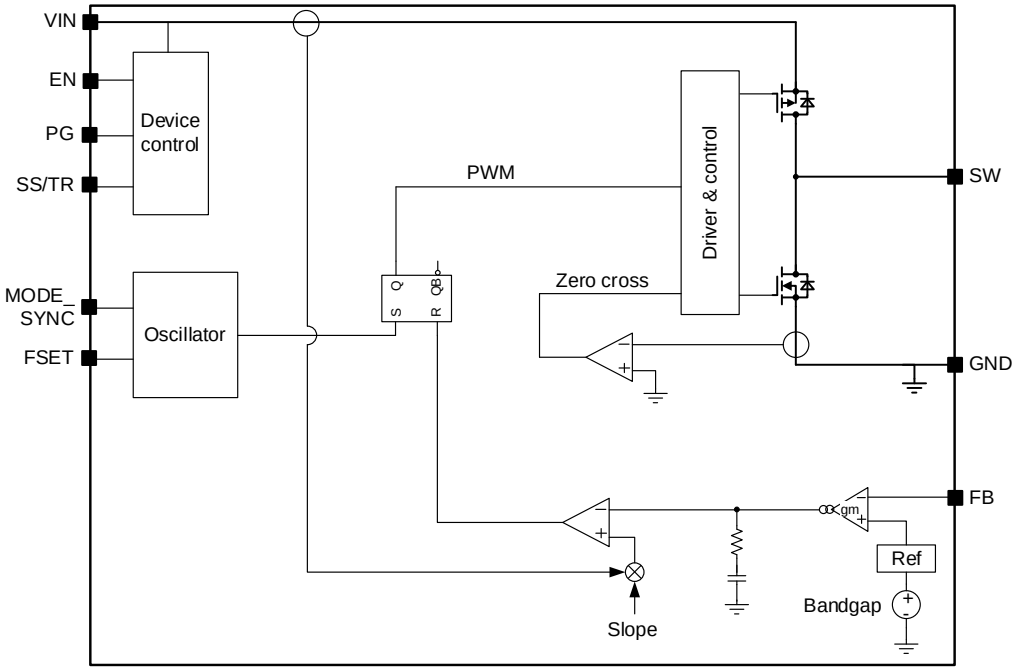


*Figure 3. Functional Block Diagram*

## Absolute Maximum Ratings

| Parameter (Note 1) | Min | Max | Unit |
|---|---|---|---|
| VIN, SW | -0.3 | 6.5 | V |
| MODE_SYNC, FB, SS/TR, FSET, EN, PG | -0.3 | VIN + 0.3 | |
| Dynamic SW to GND voltage in 10ns Duration | -3 | VIN + 2 | |
| Dynamic SW to GND voltage in 20ns Duration | -3 | VIN + 1.5 | |
| Junction Temperature, Operating | -40 | 150 | °C |
| Lead Temperature (Soldering, 10 sec.) | | 260 | |
| Storage Temperature | -65 | 150 | |
| **ESD Susceptibility** | | | |
| HBM (Human Body Mode) | | 2000 | V |
| CDM (Charge Device Mode) All pins | | 500 | |

## Thermal Information

| Parameter (Note 2) | Typ | Unit |
|---|---|---|
| $\theta_{JA}$ Junction-to-Ambient Thermal Resistance | 39 | °C/W |
| $\theta_{JB}$ Junction-to-Board Thermal Resistance | 18 | |
| $\theta_{JC_top}$ Junction-to-Case (top) Thermal Resistance | 16 | |
| $\Psi_{JT}$ Junction-to-Top Characterization Parameter | 0.9 | |
| $P_D$ Power Dissipation $T_A$ = 25°C | 3.2 | W |

## Recommended Operating Conditions

| Parameter (Note 3) | Min | Max | Unit |
|---|---|---|---|
| VIN, SW | 2.8 | 5.5 | V |
| Ambient Temperature | -40 | 125 | °C |
| Junction Temperature | -40 | 150 | |


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## Electrical Characteristics

(2.8V ≤ $V_{IN}$ ≤ 5.5V, -40°C ≤ $T_J$ ≤ 125°C. typical values at $V_{IN}$ = 5V and $T_J$ = 25°C, unless otherwise noted)

| Parameter | | Symbol | Test Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| VIN | UVLO Rising Threshold | $V_{UVLO_R}$ | | 2.6 | 2.7 | 2.8 | V |
| | UVLO Falling Threshold | $V_{UVLO_F}$ | | 2.45 | 2.55 | 2.65 | V |
| | Shut Down Current | $I_{SD}$ | EN = 0V, $T_J$ = 25°C | | 1 | 2 | μA |
| | Shut Down Current | $I_{SD}$ | EN = 0V, $T_J$ = 125°C | | 10 | 30 | μA |
| | Quiescent Current | $I_Q$ | EN = VIN, no load, PFM | | 36 | 80 | μA |
| EN | EN Logic High Threshold | $V_{EN_H}$ | | 1.05 | 1.1 | 1.15 | V |
| | EN Logic Low Threshold | $V_{EN_L}$ | | 0.96 | 1.0 | 1.05 | V |
| Power Stage | Switching Frequency | $f_{SW}$ | | 1.8 | | 3 | MHz |
| | Switching Frequency Accuracy | $\%f_{SW}$ | | -15 | | 15 | % |
| | Frequency Tolerance | $f_{SW}$ | FSET pin tied to GND | 2 | 2.35 | 2.7 | MHz |
| | High Side MOSFET $R_{DS(ON)}$ | $R_{DS(ON)_HS}$ | VIN = 5V | | 28 | 45 | mΩ |
| | Low Side MOSFET $R_{DS(ON)}$ | $R_{DS(ON)_LS}$ | VIN = 5V | | 10 | 18 | mΩ |
| | Discharge Resistance | $R_{DISCHARGE}$ | | 20 | 35 | 60 | Ω |
| FB | Output Feedback Reference | $V_{REF}$ | | | 600 | | mV |
| | Output Feedback Reference Accuracy | $\%V_{REF}$ | $T_J$=25°C | -1 | | 1 | % |
| | Output Feedback Reference Accuracy | $\%V_{REF}$ | 40°C ≤ $T_J$ ≤ 125°C | -1.2 | | 1.2 | % |
| SS | Soft-Start Time | $t_{ss}$ | SS open | 70 | 150 | 300 | μs |
| | Soft-Start Current | $I_{SS}$ | | 8.5 | 10.5 | 12.5 | μA |
| | Soft-Start Discharge Resistor | $R_{DIS_SS}$ | EN = 0 | 0.7 | 1.1 | 1.5 | kΩ |
| MODE_SYNC | Synchronization Clock High Level Pulse Width (Note 4) | $t_{ON_MIN}$ | | 100 | | | ns |
| | Synchronization Clock Low Level Pulse Width (Note 4) | $t_{OFF_MIN}$ | | 100 | | | ns |
| | Sync Frequency | | SYNC Frequency ≥ 1.1× $f_{OSC}$ | 1.8 | | 3 | MHz |
| | Logic High Threshold | $V_H$ | | 1.2 | | | V |
| | Logic Low Threshold | $V_L$ | | | | 0.4 | V |
| FSET | Logic Low Threshold | $R_{FSET_L}$ | Resistance from FSET to GND, internal frequency (2.35MHz) is used | 0 | | 2 | kΩ |
| | Logic High Threshold | $R_{FSET_H}$ | Internal frequency (2.35MHz) is used | 250 | | | kΩ |
| PG | Falling (Fault) Voltage | $V_{PGTH_FF}$ | $V_{FB}$ as percent of $V_{REF}$ | 87 | 90 | 93 | $\%V_{REF}$ |
| | Rising (Good) Voltage | $V_{PGTH_RG}$ | $V_{FB}$ as percent of $V_{REF}$ | 92 | 95 | 98 | $\%V_{REF}$ |
| | Rising (Fault) Voltage | $V_{PGTH_RF}$ | $V_{FB}$ as percent of $V_{REF}$ | 107 | 110 | 113 | $\%V_{REF}$ |
| | Falling (Good) Voltage | $V_{PGTH_FG}$ | $V_{FB}$ as percent of $V_{REF}$ | 104 | 107 | 110 | $\%V_{REF}$ |


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| | | | | | | | |
|---|---|---|---|---|---|---|---|
| Thermal Shutdown | Thermal Shutdown Threshold | $T_{SD}$ | | 150 | 165 | 180 | ºC |
| | Thermal Shutdown Hysteresis | $T_{SDHYS}$ | | 10 | 15 | 20 | ºC |
| Current Limit | Peak Current Limit | $I_{LIMIT_P}$ | | 7.2 | 9 | 10.8 | A |
| | Valley Foldback Current Limit | | | 5.7 | 7.2 | 8.6 | A |
| | Negative Valley Current Limit | $I_{LIMIT_Y}$ | | 2 | 3 | 4 | A |
| Short-Circuit Protection | Short-Circuit Threshold | $V_{SCP}$ | $V_{FB}$ as percent of $V_{REF}$ | 20 | 30 | 40 | $\%V_{REF}$ |
| | Short-Circuit Response Time | $t_{SCP}$ | VIN = 5V | 5 | 10 | 20 | μs |

**Note 1:** Stresses beyond the “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

**Note 2:** $\theta_{JA}$ is measured in the natural convection at $T_A$ = 25°C on Silergy 4-layer 6.5cm x 6.5cm FR-4 substrate PCB, 2oz copper.

**Note 3:** The device is not guaranteed for electrical parameters outside the test conditions listed in the Electrical Characteristics Table.

**Note 4:** Guaranteed by design. Not tested in production.


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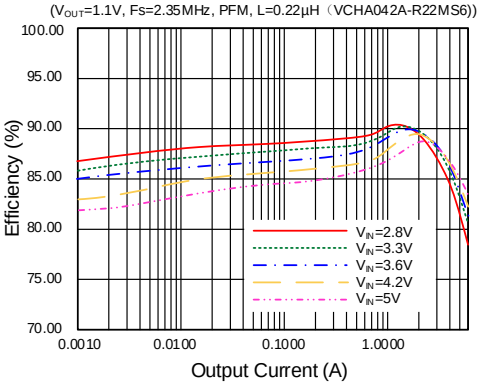
## Typical Performance Characteristics

($T_A$ = 25°C, VIN = 5V, $V_{OUT}$ =1.1V, L = 0.22µH, $C_{OUT}$ = 22µF×3, unless otherwise noted)

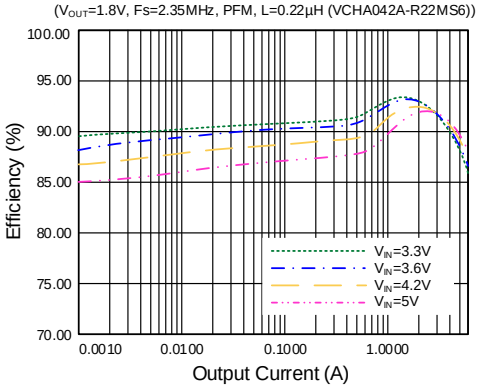
Efficiency vs Output Current

($V_{OUT}$=1.1V, Fs=2.35MHz, PFM, L=0.22µH（VCHA042A-R22MS6))



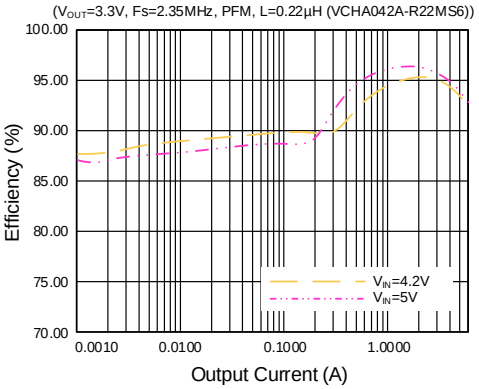

Efficiency vs Output Current

($V_{OUT}$=1.8V, Fs=2.35MHz, PFM, L=0.22µH (VCHA042A-R22MS6))



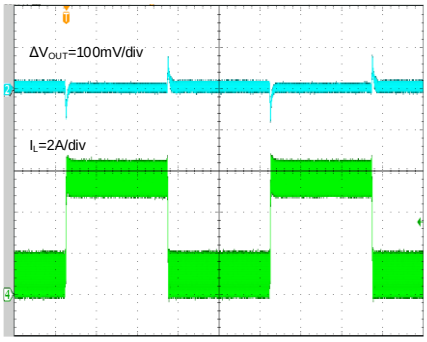

Efficiency vs Output Current

($V_{OUT}$=3.3V, Fs=2.35MHz, PFM, L=0.22µH (VCHA042A-R22MS6))



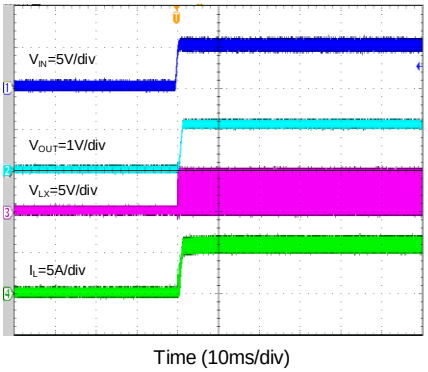

Load Transient Response

($V_{IN}$=5V, $V_{OUT}$=1.1V, $I_{OUT}$=0.6~5.4A)



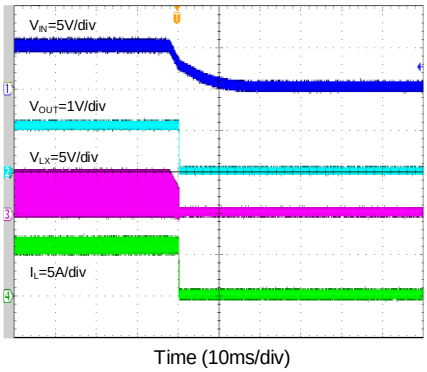

Startup from VIN

($V_{IN}$=5V, $V_{OUT}$=1.1V, $I_{OUT}$=6A)




Shutdown from VIN

($V_{IN}$=5V, $V_{OUT}$=1.1V, $I_{OUT}$=6A)





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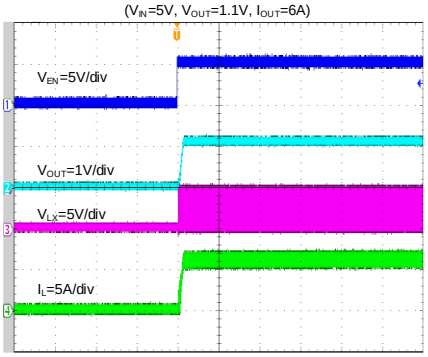
Startup from VEN

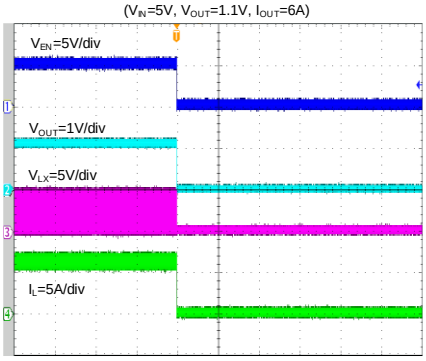
($V_{IN}$=5V, $V_{OUT}$=1.1V, $I_{OUT}$=6A)




Time (10ms/div)

Shutdown from VEN

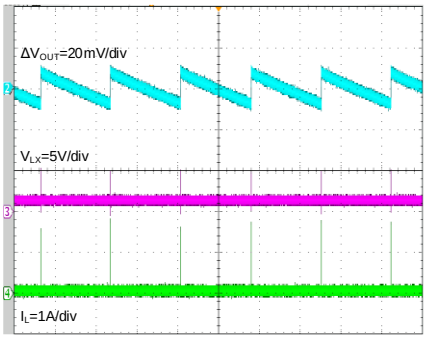
($V_{IN}$=5V, $V_{OUT}$=1.1V, $I_{OUT}$=6A)




Time (10ms/div)

Output Ripple

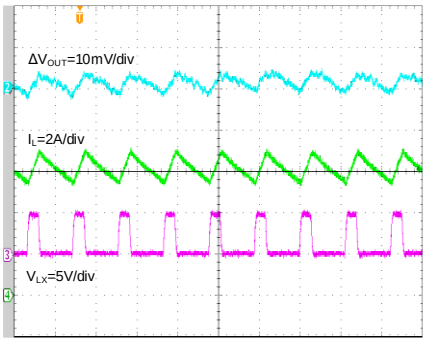
($V_{IN}$=5V, $V_{OUT}$=1.1V, $I_{OUT}$=0A)




Time (40ms/div)

Output Ripple

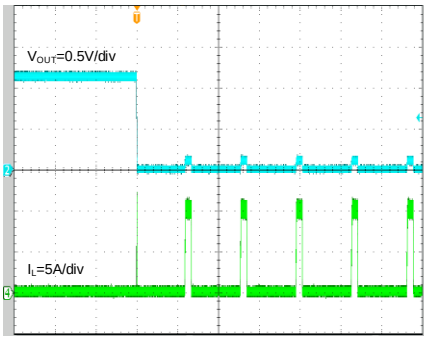
($V_{IN}$=5V, $V_{OUT}$=1.1V, $I_{OUT}$=6A)




Time (400ns/div)

Output Short Circuit

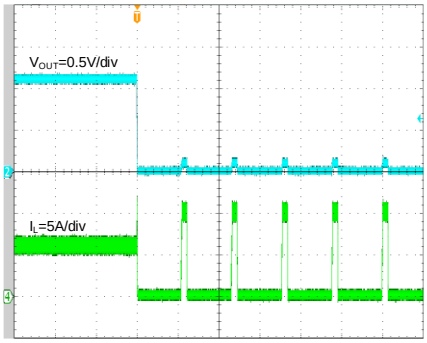
($V_{IN}$=5V, $V_{OUT}$=1.1V, $I_{OUT}$=0A)




Time (10ms/div)

Output Short Circuit

($V_{IN}$=5V, $V_{OUT}$=1.1V, $I_{OUT}$=6A)




Time (10ms/div)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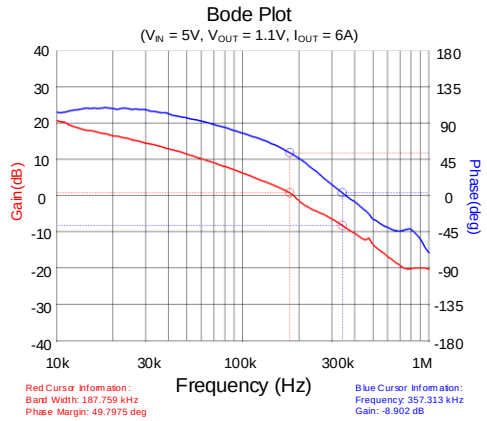


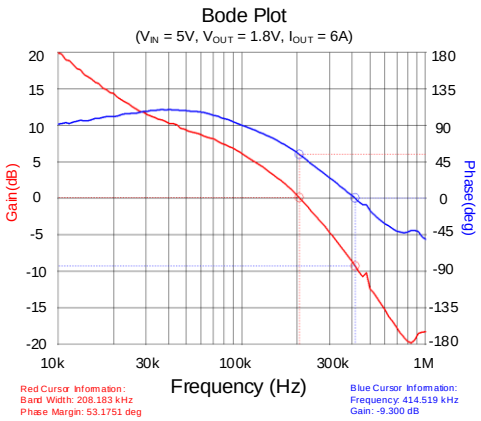


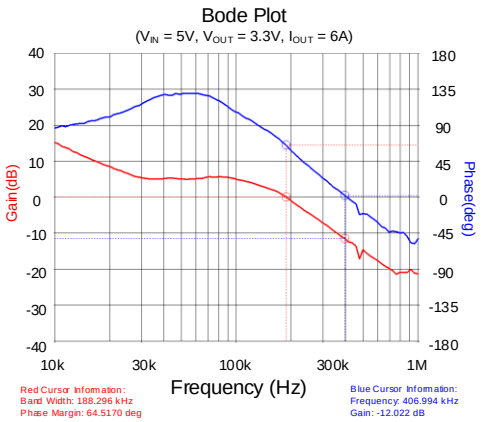



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## Detailed Description

The SY2A23006 synchronous buck converter has built-in power MOSFETs, an input voltage range of 2.8V to 5.5V, a configurable output voltage from 0.6V to $V_{IN}$, and a maximum load current capability of 6A. Under light load conditions, it can operate in either pulse width modulation (PWM) mode or pulse frequency modulation (PFM) mode. The soft-start time and 1.8MHz-3MHz switching frequency can be adjusted using external components. The SY2A23006 also provides power good indication, undervoltage lockout (UVLO), short-circuit protection, cycle-by-cycle current limit protection, and thermal shutdown.

### FSET

The FSET pin can independently configure the following parameters:

- Switching frequency (1.8MHz to 3MHz, adjustable in PWM mode)
- Internal compensation of control loop (two settings available)
- Frequency Spread Spectrum (7.5k modulation frequency and ±5% modulation amplitude)

Connect the FSET pin to GND with a resistor to configure the switching frequency and the control loop compensation. The switching frequency, which the user can adjust during operation, must be selected to meet the minimum on-time (typical 85ns/maximum 125ns) and minimum off-time (typical 100ns/maximum 150ns), based on the input and output voltages. The compensation selection, which is sampled and latched at converter startup, must balance the values of output capacitance with dynamic performance requirements.

To reduce external components, the FSET pin can also be directly tied to VIN or GND to set a predefined switching frequency or compensation. The minimum parasitic capacitance on FSET is beneficial for switching-frequency stability, which requires the resistor to be placed close to this pin. There is no internal pulldown resistor. Do not leave FSET floating.

**Table 1. Compensation Settings**

| Compensation | $R_{FS}$ | Switching Frequency | Spread Spectrum | $g_M$ |
|---|---|---|---|---|
| Setting 1 | 6k-10k | $f_{osc}=\frac{18\text{MHz}\cdot\text{k}\Omega}{R_{FS}(\text{k}\Omega)}$ | No | Low |
| Setting 2 | 20k-33k | $f_{osc}=\frac{60\text{MHz}\cdot\text{k}\Omega}{R_{FS}(\text{k}\Omega)}$ | Yes | Low |
| Setting 3 | 60k-100k | $f_{osc}=\frac{180\text{MHz}\cdot\text{k}\Omega}{R_{FS}(\text{k}\Omega)}$ | No | High |
| Setting 4 | Tied to GND | Fixed 2.35MHz | No | Low |
| Setting 5 | Tied to VIN | Fixed 2.35MHz | Yes | High |

### MODE_SYNC

The MODE_SYNC pin combines mode control and frequency synchronization. Under light load conditions, the SY2A23006 operates in PFM mode when the MODE_SYNC pin is set low, and operates in forced PWM mode when the MODE_SYNC pin is set high. If an external clock frequency is applied on the MODE_SYNC pin, the switching frequency will be synchronized to the external clock frequency and the device will operate in forced PWM mode. The external frequency must be selected in the frequency range 1.8 MHz to 3MHz, and it must meet the specifications for the minimum on-time (85ns typical) and minimum off-time (100ns typical).

To ensure device performance and successful synchronization, the external clock frequency must be at least 1.1 times larger than the internal oscillator clock set by $R_{FS}$, as shown in the following formula:

$$f_{external_clock} \geq 1.1\times f_{osc}$$

Otherwise, the SY2A23006 will fail to synchronize with the external clock. Also, the external clock minimum on-time and minimum off-time must be greater than 100ns. When there is no resistor from FSET to GND, but the pin is pulled high or low, external synchronization is not possible.

### Enable and Power Sequencing

The EN pin acts as the enable control input. The EN comparator has an accurate 1.1V rising threshold with 0.1V hysteresis. Pull EN high to enable the internal reference and the analog circuits. Soft-start is then activated, and the output voltage is ramped up. Pull EN low to turn off the device. To prevent power from cycling improperly due to disturbances on the EN pin, the device starts switching after a delay of approximately 250µs when EN is set high, and stops switching after a delay of about 3µs when EN is set low. Furthermore, the chip will stop switching when VIN voltage is above 7.1V (min 6.8V, max 7.4V) with 0.3V hysteresis voltage, even if the EN pin is high. See Figure 4.

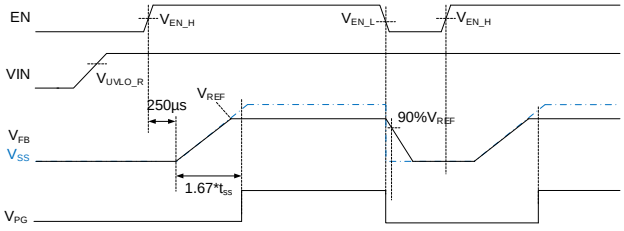


*Figure 4. Enable ON/OFF Sequence*

### SS

The SS/TR pin can be used as an external interface for the internal soft-start circuitry. SS is used to control the output voltage slope during startup to avoid excessive inrush current, prevent unwanted voltage drop from high impedance power sources, and ensure a controlled


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output voltage rise time. The internal reference rises with a slope controlled by an external capacitor, which is connected from the SS pin to GND and charged with 10.5μA by an internal current source. Leave the SS pin open for the fastest startup ramp (150μs typical). The capacitance required to set a given ramp time ($t_{RAMP}$) can be determined using the following equation:

$$C_{ss} = 10.5uA \cdot t_{ramp}(ms) / 1V$$

**TR**

The SS/TR pin can also be used as an input for tracking and sequencing, which allows the output voltage to follow the voltage applied at TR in both directions (up and down) in forced PWM mode. This requires the voltage applied at TR to be below the feedback voltage (0.6V). If the voltage on TR is above the feedback voltage, the internal reference is clamped to 0.6V and the output voltage no longer varies with TR pin voltage.

**Power Good**

The SY2A23006 provides an external PG pin for power good indication. PG is an open-drain output, which should be connected to VIN or another voltage source through a resistor (e.g. 100kΩ).

When VIN voltage rises until the internal initial power is ready, the PG internal MOSFET is turned on so that PG is actively driven low. After soft-start is complete and the feedback voltage $V_{FB}$ rises above 95% of $V_{REF}$ (rising edge) and stays below 107% of $V_{REF}$ (falling edge), PG is set to high-impedance state after a delay time of 15μs (typical). When $V_{FB}$ drops to 90% of $V_{REF}$ (falling edge), or rises above 110% of $V_{REF}$ (rising edge), PG is driven low after a delay time of 35μs (typical). When EN is set low, PG is driven low after a delay time of 3μs (typical), whether $V_{FB}$ drops to 90% of $V_{REF}$ or not. See Figure 5.

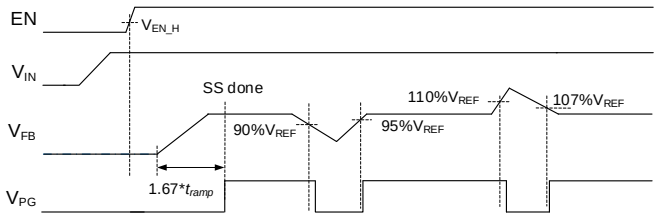


*Figure 5. Power Good Logic*

## Fault Protection Modes

**Current Limit Protection**

The SY2A23006 features cycle-by-cycle current limit protection. When the peak current exceeds the limit threshold, the device will turn off the power switch for the remainder of the cycle. If the peak current limit is detected for three consecutive cycles, the valley current limit threshold will fold back to 80% of the original value. See Figure 6.

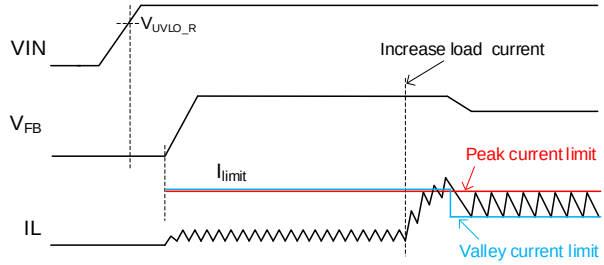


*Figure 6. Cycle-by-Cycle Current Limit*

**Short-Circuit Protection**

The SY2A23006 provides output short-circuit protection to prevent power MOSFET damage. When the output voltage drops below the short-circuit threshold, after the initial short-circuit blanking time $t_{SCP}$, the device will remain off for the hiccup time (7 × SS time) and then proceed through the soft-start $t_{SS}$. See Figure 7.

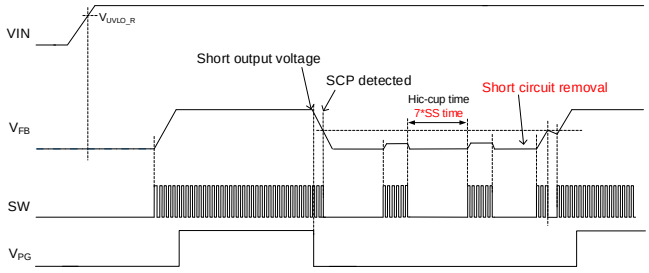


*Figure 7. Short Circuit Protection*

**Overtemperature Protection**

The SY2A23006 enters thermal shutdown when the junction temperature exceeds 165°C (typical). In this mode, the high side switch and low side switch are turned off. When the junction temperature falls below 150°C (typical), the buck will be re-enabled automatically. See Figure 8.

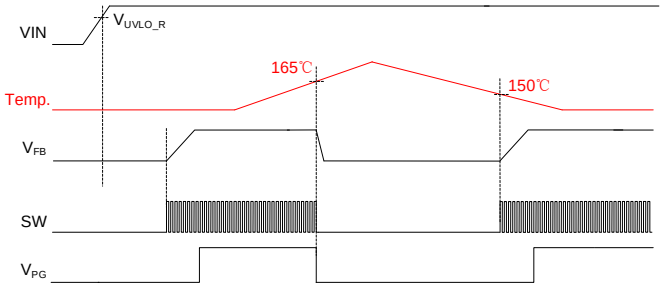


*Figure 8. Overtemperature Protection*

## Application Information

**Feedback Resistor Divider $R_{TOP}$ and $R_{BOT}$**

Choose $R_{TOP}$ and $R_{BOT}$ to program the proper output voltage. Choose larger resistor values for both $R_{TOP}$ and $R_{BOT}$ to minimize the power consumption under light loads. Choose lower resistor values for a more robust design


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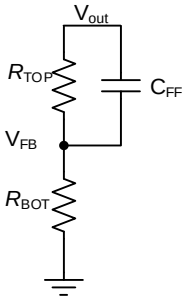
and to suppress high frequency noise. A value between 10kΩ and 100kΩ is highly recommended for both resistors.

The output voltage can be configured using the following equation:

$$V_{OUT} = (1 + \frac{R_{TOP}}{R_{BOT}}) \times V_{FB}$$




where $V_{FB}$ has a value of 0.6V (typical).

**Output Inductor L**

Consider the following when choosing this inductor.

1) Choose the inductance to provide the desired ripple current that is approximately 40% of the maximum output current. The recommended inductance is calculated as follows:

$$L = \frac{V_{OUT} \times (1 - V_{OUT} / V_{IN_MAX})}{F_S \times I_{OUT_MAX} \times 40\%}$$

where Fs is the switching frequency and $I_{OUT_MAX}$ is the maximum load current.

2) The SY2A23006 has high tolerance for ripple current amplitude variation. As a result, the final choice of inductance can vary slightly from the calculated value with no significant performance impact.

3) The inductor's saturation current rating must be greater than the peak inductor current under full load:

$$I_{SAT_MIN} > I_{OUT_MAX} + \frac{V_{OUT} \times (1 - V_{OUT} / V_{IN_MAX})}{2F_S \times L}$$

4) The DCR of the inductor and the core loss at the switching frequency must be low enough to achieve the desired efficiency requirement. Choose an inductor with smaller DCR to achieve good overall efficiency.

**Input Capacitor $C_{IN}$**

The ripple current through the input capacitor is calculated as follows:

$$I_{CIN_RMS} = I_{OUT_MAX} \times \sqrt{D \times (1 - D)}$$

The capacitance of input capacitor is calculated as follows:

$$C_{IN} = \frac{I_{OUT} \times V_{OUT} \times (V_{IN} - V_{OUT})}{\Delta V_{IN} \times F_s \times \eta \times V_{IN}^2}$$

where $\Delta V_{IN}$ is maximum allowed input voltage ripple.

For reliable operation, place typical X7R or better grade ceramic capacitors close to the VIN and GND pins. Minimize the loop area formed by $C_{IN}$ and the VIN/GND pins. For most applications, three 10µF ceramic capacitors are recommended, and a 1µF 0402 low ESR capacitor placed closest to the chip is highly recommended.

**Output Capacitor $C_{OUT}$**

Select the output capacitor $C_{OUT}$ to handle the output ripple requirements.
For applications where the design must meet stringent ripple requirements, the following considerations must be followed:

The output voltage ripple at the switching frequency is caused by the inductor current ripple ($\Delta I_L$) on the output capacitor's ESR (ESR ripple), as well as the stored charge (capacitive ripple). When calculating total ripple, consider both.

$$V_{RIPPLE,ESR} = \Delta I_L \times ESR$$

$$V_{RIPPLE,CAP} = \frac{\Delta I_L}{8 \times C_{OUT} \times f_{SW}}$$

The measured capacitive ripple may be higher than the calculated value because the effective capacitance for ceramic capacitors decreases with the voltage across their terminals. The voltage derating is usually included as a chart in the capacitor datasheet, and the ripple can be recalculated after taking the target output voltage into account. The recommended minimum output capacitance values for typical applications are provided below, based on the Vout selected.

It is recommended to use X7R or better grade ceramic capacitors. The recommended output capacitance values and configuration depends on the FSET pin configuration resistance and output voltage. Recommended values can be found in the Recommended Values for Typical Applications paragraph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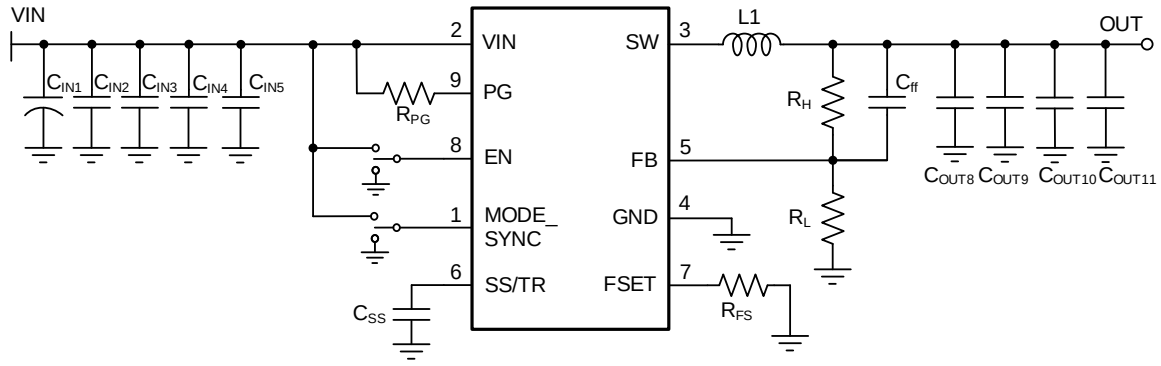
## Application Schematic ($V_{OUT}$ = 1.1V, $F_S$ = 2.35MHz)




## BOM List

| Reference Designator | Description | Part Number | Manufacturer |
|---|---|---|---|
| $C_{IN1}$ | E-cap 47µF, 10V | | Panasonic |
| $C_{IN2}$, $C_{IN3}$, $C_{IN4}$ | Cap 10µF, 6.3V, 0603 | GCM188D70J106ME36D | Murata |
| $C_{IN5}$ | Cap 1µF, 10V, 0402 | GCM155C71A105KE38D | Murata |
| $C_{SS}$ | Cap 15nF, 50V, 0603 | GCM188L81H153KA37D | Murata |
| $C_{FF}$ | Cap 47pF, 50V, 0603 | GCM1885G1H470FA16D | Murata |
| $C_{OUT8}$, $C_{OUT9}$, $C_{OUT10}$ | Cap 22µF, 6.3V, 1206 | GCM31CR70J226ME23L | Murata |
| $R_{PG}$ | Res 100kΩ, 0603 | | YAGEO |
| $R_{FS}$ | Res 7.5kΩ, 0603 | | YAGEO |
| $R_H$ | Res 39.2kΩ, 0603 | | YAGEO |
| $R_L$ | Res 47kΩ, 0603 | | YAGEO |
| L | Inductor 0.22µH | VCHA042A-R22MS6 | Cyntec |
| U1 | Silergy 6A Regulator | | Silergy |
| $C_{OUT11}$ | NC | | |

## Recommended Component Values for Typical Applications

| $V_{OUT}$ (V) | $R_H$ (kΩ) | $R_L$ (kΩ) | $C_{FF}$ (pF) | L (µH) | $C_{OUT}$ ($g_M$ is low) | $C_{OUT}$ ($g_M$ is high) |
|---|---|---|---|---|---|---|
| 0.6 | 0 | NC | NC | 0.22 | 22µF × 4, 6.3V, 1206, X7R | 22µF × 5, 6.3V, 1206, X7R |
| 0.8 | 10 | 30 | 47 | 0.22 | 22µF × 4, 6.3V, 1206, X7R | 22µF × 5, 6.3V, 1206, X7R |
| 0.9 | 15 | 30 | 47 | 0.22 | 22µF × 4, 6.3V, 1206, X7R | 22µF × 5, 6.3V, 1206, X7R |
| 1 | 20 | 30 | 47 | 0.22 | 22µF × 4, 6.3V, 1206, X7R | 22µF × 5, 6.3V, 1206, X7R |
| 1.1 | 39.2 | 47 | 47 | 0.22 | 22µF × 3, 6.3V, 1206, X7R | 22µF × 4, 6.3V, 1206, X7R |
| 1.2 | 47 | 47 | 47 | 0.22 | 22µF × 3, 6.3V, 1206, X7R | 22µF × 4, 6.3V, 1206, X7R |
| 1.5 | 30 | 20 | 47 | 0.22 | 22µF × 3, 6.3V, 1206, X7R | 22µF × 4, 6.3V, 1206, X7R |
| 1.8 | 30 | 15 | 47 | 0.22 | 22µF × 3, 6.3V, 1206, X7R | 22µF × 4, 6.3V, 1206, X7R |
| 2.5 | 47.5 | 15 | 47 | 0.22 | 22µF × 3, 6.3V, 1206, X7R | 22µF × 4, 6.3V, 1206, X7R |
| 3.3 | 88.7 | 19.6 | 47 | 0.22 | 22µF × 3, 6.3V, 1206, X7R | 22µF × 4, 6.3V, 1206, X7R |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## Layout Design

Follow these PCB layout guidelines for optimal performance:

- To achieve the best thermal and noise performance, maximize the PCB copper area connected to the GND pin. Using a separate layer as a ground plane is highly recommended.
- Place the input capacitors on the left side of the IC, as close as possible, between the VIN and GND pins. A 1µF 0402 low ESR capacitor $C_{IN2}$ placed near the IC is highly recommended. See Figure 9.
- Minimize the PCB copper area associated with the SW pin to reduce EMI.
- To reduce noise, place the feedback components $R_{TOP}$ and $R_{BOT}$ close to the IC and not adjacent to the SW net. The trace connecting to the FB pin must be as short as possible, and the GND of $R_{BOT}$ must not be adjacent to the GND of the VIN capacitor.

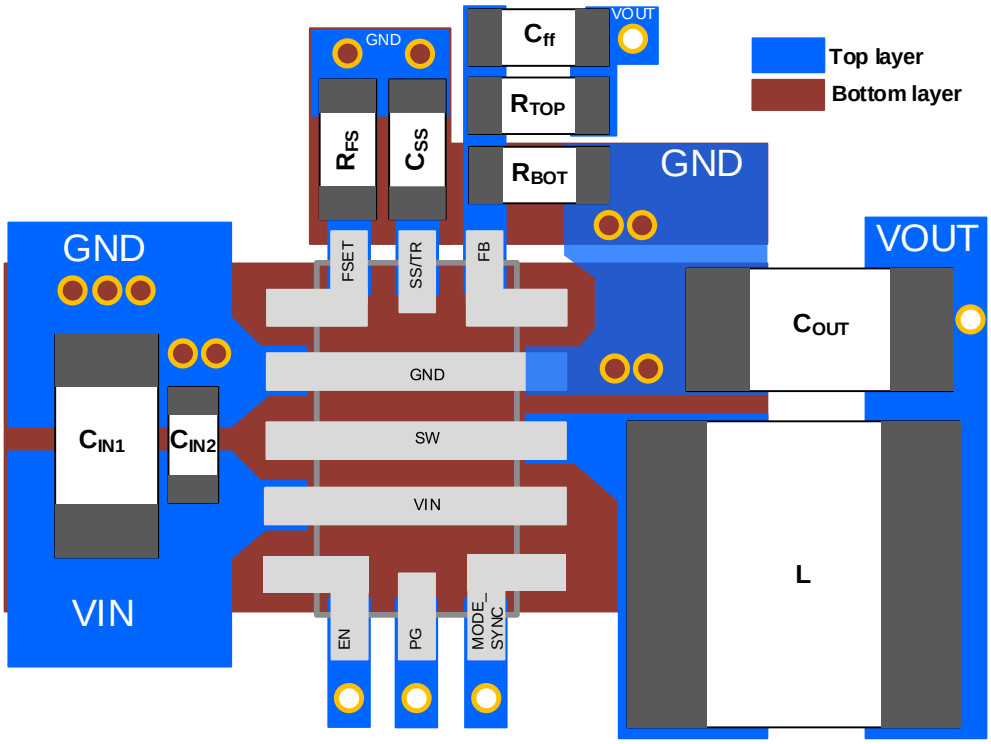


*Figure 9. Layout Design Suggestion*


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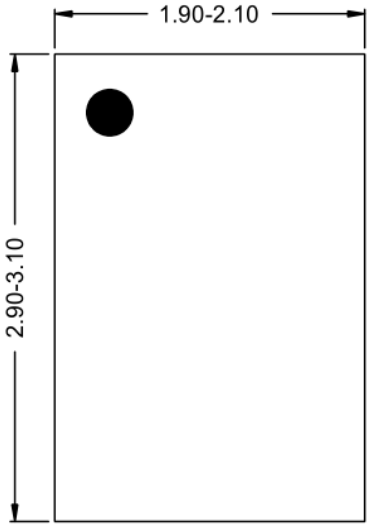
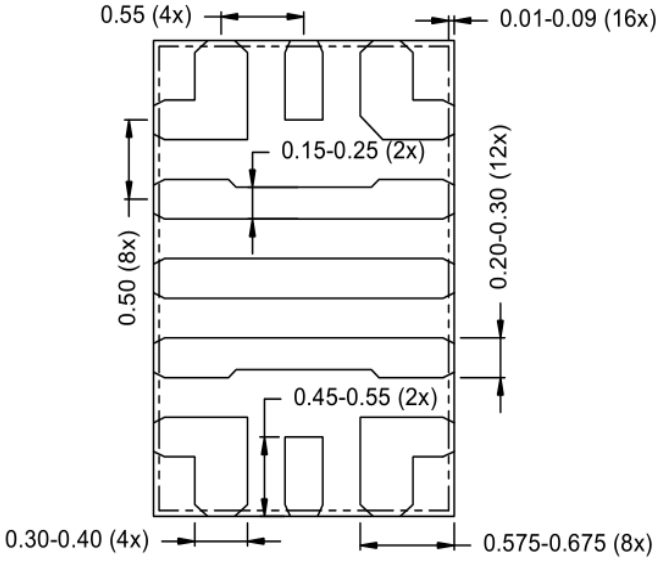
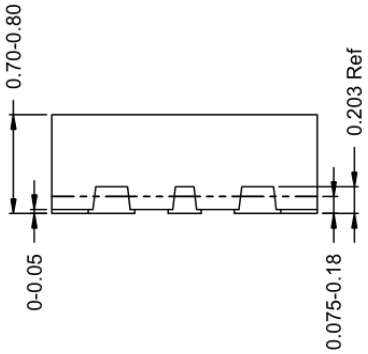
## QFN2×3-9 Package Outline Drawing



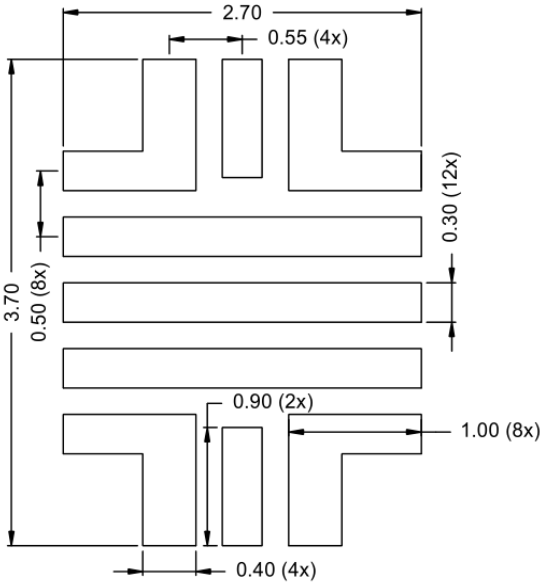

**Top View**




**Bottom View**




**Front View**




**Recommended PCB Layout (Reference Only)**

***Note:*** *All dimensions are in millimeters and exclude mold flash and metal burr.*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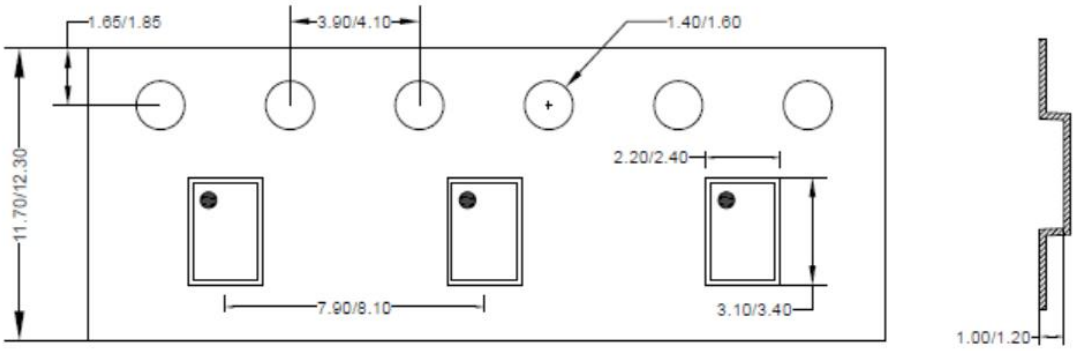
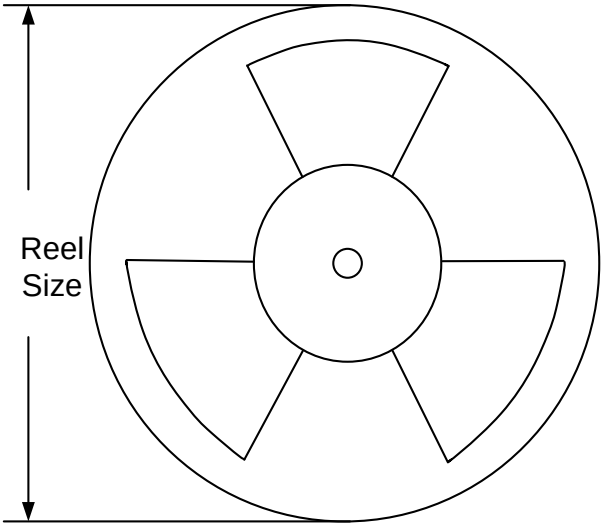
# Tape and Reel Specification

## QFN2×3-9 Taping Orientation




**Feeding direction** ⟶

## Carrier Tape and Reel Specification for Packages




| Package Types | Tape Width (mm) | Pocket Pitch (mm) | Reel Size (inch) | Trailer Length (mm) | Leader Length (mm) | Qty per Reel |
|---|---|---|---|---|---|---|
| QFN2×3-9 | 12 | 8 | 13" | 400 | 400 | 5000 |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# Revision History

The revision history provided is for informational purposes only and is believed to be accurate, however, not warrantied. Please make sure that you have the latest revision.

| Date | Revision | Change | Pages changed |
|---|---|---|---|
| Mar.11, 2024 | Revision 1.0 | Initial Release | - |
| Apr.12, 2024 | Revision 1.0A | Language Improving (No change in specification). | - |


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