SY21249F

High Efficiency,Fast Response, 11A, 28V Input Synchronous Buck Converter with 100mA 5V LDO

General Description

The SY21249F is a high efficiency synchronous buck converter capable of delivering up to 11A current. It integrates low $R_{DS(ON)}$ top and bottom MOSFETs to minimize the conduction loss. It operates at pseudo-constant frequency of 600kHz, to enable the use of small size inductor and capacitors. The SY21249F integrates a fixed 5V LDO with 100mA current capability, which can be used to power the external peripheries, such as the keyboard controller in the notebook. The 5V LDO can switch to bypass input to reduce power loss.

Silergy's constant on-time and ripple-based control strategy supports high input/output voltage ratios (low duty cycles), and fast transient response while maintaining a near constant operating frequency over line, load and output voltage ranges. This control method provides stable operation without complex compensation, including when using low ESR output ceramic capacitors.

The SY21249F provides cycle-by-cycle current limit, input under voltage lockout, internal soft-start, output under voltage protection, over voltage protection and over temperature protection, to guarantee safe operation in all operating conditions.

Features

- Low $R_{DS(ON)}$ for Internal MOFETs: 17mΩ Top, 7.5mΩ Bottom
- Wide Input Voltage Range: 5.5V ~ 24V
- Adjustable Output Voltage: 1V ~ 12V
- High Duty Cycle Capable using On-Time Stretch
- 11A Continuous Output Current Capability
- 100mA LDO Current Capability
- 600kHz Pseudo-Constant Frequency
- ±1% Internal Reference Voltage (V_{REF})
- Internal 0.8ms Soft-Start Limits the Inrush Current
- Constant On-Time and Ripple-Based Control to Achieve Fast Transient Responses
- Integrated 1.5Ω Bypass Switch
- PFM/USM Selectable Light Load Operation Mode
- Power Good Indicator
- Output Auto-Discharge Function
- Cycle-by-Cycle Valley and Peak Current Protection for buck
- Latch-off Mode Output Under Voltage Protection for buck
- Latch-off Mode Output Over Voltage Protection for buck
- Latch-off Mode Over Temperature Protection for buck
- Auto-recovery Mode Output Under Voltage Protection for LDO
- Auto-recovery Mode Over Temperature Protection for LDO
- Input Under Voltage Lockout(UVLO)
- RoHS Compliant and Halogen Free
- Compact Package: QFN3×4-13

Applications

- LCD-TV/Net-TV/3DTV
- Set Top Box
- Notebook
- High Power AP

Typical Application

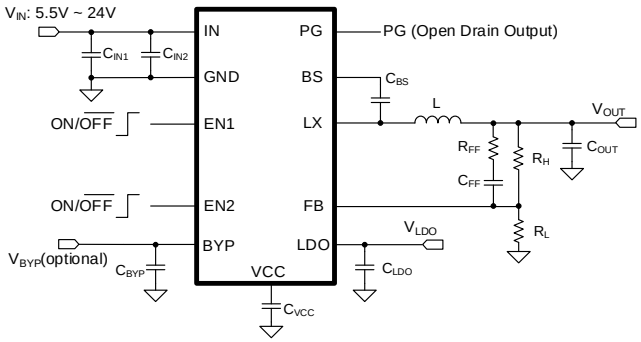

Figure1. Schematic Diagram

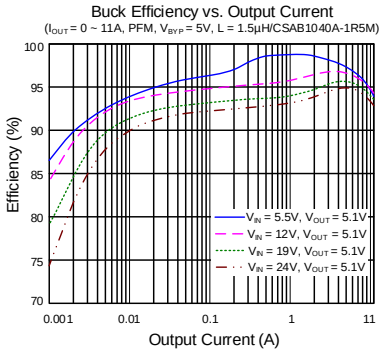

Figure2. Buck Efficiency vs. Output Current

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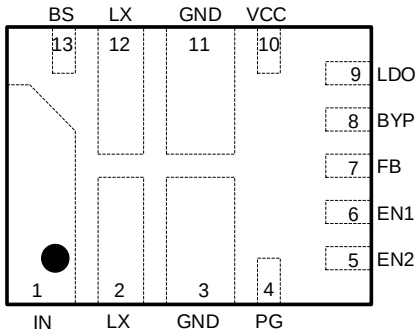
Ordering Information

Ordering Part Number	Package type	Top Mark
SY21249FTMC	QFN3×4-13 RoHS Compliant and Halogen Free	**EHE*xyz***

x = year code, y = week code, z = lot number code

Pinout (top view)



Pin Description

Pin No.	Pin Name	Pin Description
1	IN	Input pin. Decouple this pin to GND pin with at least a 20μF ceramic capacitor. A 0.1μF input ceramic capacitor is recommended to reduce the input noise.
2, 12	LX	Inductor pin. Connect this pin to the switching node of the inductor.
3, 11	GND	Ground pin.
4	PG	Power good indicator pin. PG pin should be connected to V_{IN} or another voltage source through a resistor (e.g., 10kΩ ~ 100kΩ). This pin becomes high when the output voltage is within 90% to 120% of regulated value under normal operation.
5	EN2	Enable control pin for the buck converter and internal LDO. Pull high to turn on. Pull low to turn off. Do not leave this pin floating.
6	EN1	Enable control pin of the buck converter. Pull high to turn on. Pull low to turn off. Do not leave this pin floating. The pin is also used for controlling the operation mode of the buck converter under light load condition after its output is within the regulated range. When its voltage is lower than 1.6V and higher than 1V, the buck converter operates in ultra-sonic mode. When its voltage is higher than 2.2V, the buck converter operates in pulse-frequency modulation mode.
7	FB	Output feedforward pin. Connect to the center point of the resistor divider.
8	BYP	External 5V bypass power supply input pin. Decouple this pin to the GND with a 1μF ceramic capacitor. Make one good RC filter for BYP input if the external power rail has significant ripple.. Leave this pin floating or connect this pin to the GND if it is not used.
9	LDO	5V LDO output pin. Decouple this pin to ground with at least a 4.7μF capacitor.
10	VCC	Internal 3.6V LDO output pin. Power supply for internal analog circuits and driving circuit. Decouple this pin to GND with at least a 2.2μF ceramic capacitor.
13	BS	Bootstrap pin. Supply top MOSFET gate driver. Connect a 0.1μF ceramic capacitor between the BS pin and the LX pin.

EN2	EN1	BYP Voltage	LDO	Buck	TSD Temperature
0	Any	Any	0V	0V	
1	0	0V	5V (Powered by Input)	0V	LDO 160℃
1	0	5V	5V (Powered by BYP)	0V	LDO 160℃
1	1	0V	5V (Powered by Input)	V_{SET}	buck 150℃/LDO 160℃
1	1	5V	5V (Powered by BYP)	V_{SET}	buck 150℃/LDO 160℃

Table1. Truth Table

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Block Diagram

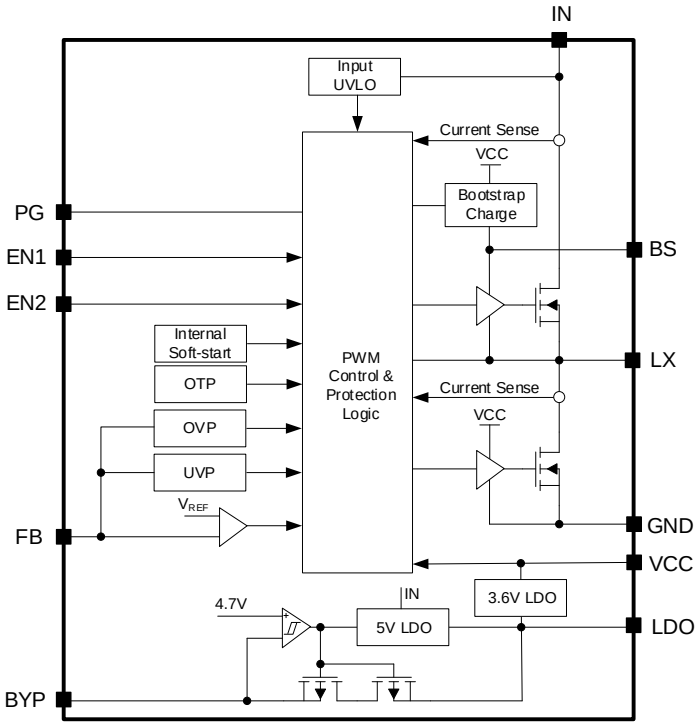

Figure3. Block Diagram

Absolute Maximum Ratings

Parameter (Note1)	Min	Max	Unit
IN	-0.3	28	V
LX, PG, EN1, EN2	-0.3	26	
BS-LX, VCC, FB	-0.3	4	
BYP, LDO	-0.3	6.5	
LX, 10ns Duration	-5	29	
LX, 20ns Duration	-1	28	
Junction Temperature, Operating	-40	150	°C
Lead Temperature (Soldering, 10s.)		260	
Storage Temperature	-65	150	

Thermal Information

Parameter (Note2)	Typ	Unit
θ_{JA} Junction-to-Ambient Thermal Resistance	27	°C/W
θ_{JC} Junction-to-Case Thermal Resistance	4.3	
P_D Power Dissipation T_A = 25°C	3.7	W

Recommended Operating Conditions

Parameter (Note3)	Min	Max	Unit
IN	5.5	24	V
Buck Output Voltage	1	12	
Buck Output Current		11	A
LDO Output Current		100	mA
Ambient Temperature	-40	85	°C
Junction Temperature	-40	125	

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Electrical Characteristics

(V_{IN} = 12V, L = 1.5μH, C_{OUT} = 100μF, C_{FF} = 470pF, T_A = 25°C, I_{OUT} = 1A unless otherwise specified)

Parameter		Symbol	Test Conditions	Min	Typ	Max	Unit
Input	Voltage Range	V_{IN}		5.5		24	V
	UVLO Rising Threshold	$V_{IN,UVLO}$	V_{IN} rising			5	
	UVLO Hysteresis	$V_{IN,HYS}$			0.5		
	Quiescent Current	I_Q	I_{OUT} = 0A, EN1 = EN2 = 1, V_{FB} = V_{REF} × 105%		180	225	μA
	Shutdown Current 1	I_{SHDN1}	EN1 = Low, EN2 = High		75	98	
	Shutdown Current 2	I_{SHDN2}	EN1 = Low, EN2 = Low		7	12	
Output	Voltage Range	V_{SET}		1		12	V
	Feedback Reference Voltage	V_{REF}		0.594	0.600	0.606	
	Maximum Duty Cycle	D_{MAX}		95			%
	FB Input Current	I_{FB}	V_{FB} = 3.3V	-50		50	nA
	Discharge Current	I_{DIS}	V_{OUT} = 5.1V		100		mA
	Soft-Start Time	t_{SS}	V_{OUT} from 0% to100%V_{REF} (Note4)		0.8		ms
	OVP Threshold	V_{OVP}	V_{FB} rising	115	120	125	%V_{REF}
	OVP Hysteresis	$V_{OVP,HYS}$			5		
	OVP Delay Time	$t_{OVP,DLY}$	(Note4)	30	40		μs
	UVP Threshold	V_{UVP}	V_{FB} falling	28	33	38	%V_{REF}
	UVP Delay Time	$t_{UVP,DLY}$	(Note4)		200		μs
MOSFET	Top MOSFET $R_{DS(ON)}$	$R_{DS(ON),TOP}$			17		mΩ
	Bottom MOSFET $R_{DS(ON)}$	$R_{DS(ON),BOT}$			7.5		
	Top MOSFET Current Limit Threshold	$I_{LMT,TOP}$			22		A
	Bottom MOSFET Current Limit Threshold	$I_{LMT,BOT}$		13.5			
	Bottom MOSFET Reverse Current Limit Threshold	$I_{LMT,RVS}$	USM	4	6.5		
Enable(EN)	Input Voltage High	$V_{EN,H}$		1			V
	Input Voltage Low	$V_{EN,L}$				0.4	
	EN1 Voltage for Ultra-sonic Mode	$V_{EN1,USM}$		1		1.6	
	EN1 Voltage for PFM Mode	$V_{EN1,PFM}$		2.2		V_{IN}	
Frequency	Switching Frequency	f_{SW}	V_{OUT} = 5.1V, CCM	510	600	690	kHz
	Ultra-sonic Mode Frequency	f_{USM}	I_{OUT} = 0A, USM	20			
	Minimum On-Time	$t_{ON,MIN}$	V_{IN} = $V_{IN,MAX}$ (Note4)		50		ns
	Minimum Off-Time	$t_{OFF,MIN}$			150		

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Parameter		Symbol	Test Conditions	Min	Typ	Max	Unit
Power Good	Rising Threshold	$V_{PG,R}$	V_{FB} rising (good)	87	90.5	94	$\%V_{REF}$
	Falling Threshold	$V_{PG,F}$	V_{FB} falling (not good)	80	83.5	87	
	Delay Time	$t_{PG,R}$	Low to high (Note4)		200		μs
		$t_{PG,F}$	High to low (Note4)		40		
	Low Voltage	$V_{PG,LOW}$	V_{FB} = 0V, I_{PG} = 5mA			0.45	V
VCC	Output Voltage	V_{CC}	VCC adds 1mA load	3.45	3.6	3.75	
LDO	Output Voltage	V_{LDO}	BYP off, I_{LDO} = 0mA	4.9	5	5.15	
	Dropout Voltage	$V_{DROPOUT}$	I_{LDO} = 100mA		300		mV
	Output Current Limit Threshold	$I_{LMT,LDO}$		150		310	mA
BYP	$R_{DS(ON)}$	$R_{DS(ON),BYP}$			1.5		Ω
	Turn on Voltage	V_{BYP}		4.5	4.7	4.9	V
	Turn on Hysteresis	$V_{BYP,HYS}$			0.2		
	OVP Voltage	$V_{BYP,OVP}$			120		$\%V_{LDO}$
OTP	buck Temperature	$T_{OTP,BUCK}$	T_J rising (Note4)		150		°C
	buck Temperature Hysteresis	$T_{BUCK,HYS}$	T_J falling (Note4)		15		
	LDO Temperature	$T_{OTP,LDO}$	T_J rising (Note4)		160		
	LDO Temperature Hysteresis	$T_{LDO,HYS}$	T_J falling (Note4)		25		

Note 1: Stresses beyond the “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: Package thermal resistance is measured in the natural convection at T_A = 25°C on a 8.5cm×8.5cm size, four-layer Silergy Evaluation Board with 2-oz copper.

Note 3: The device is not guaranteed to function outside its operating conditions.

Note 4: Guaranteed by design.

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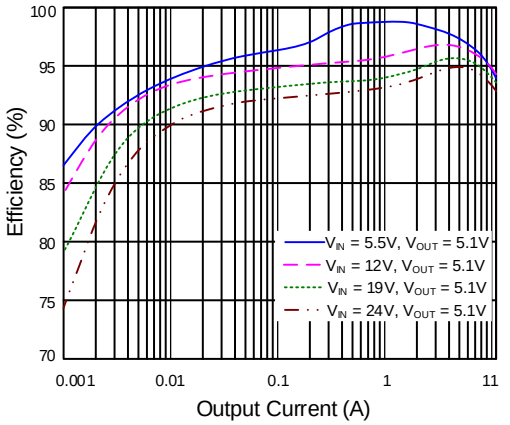
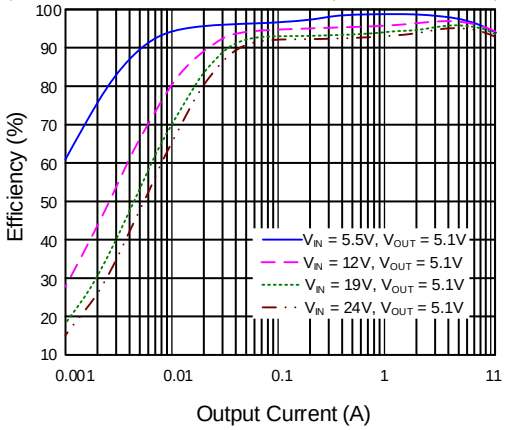
Typical Performance Characteristics

(T_A = 25°C, V_{IN} = 12V, V_{OUT} = 5.1V, L = 1.5µH, C_{OUT} = 88µF, C_{FF} = 220pF, unless otherwise noted)

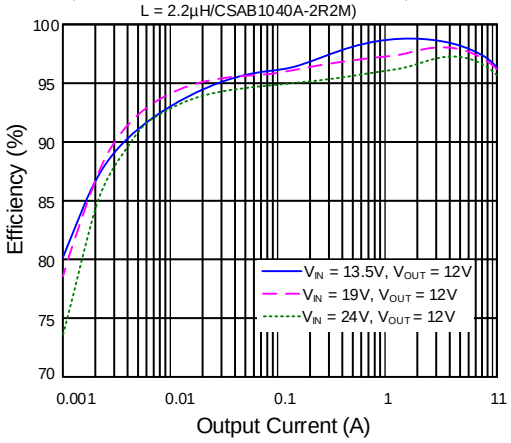
Buck Efficiency vs. Output Current
(I_{OUT} = 0.001A ~ 11A, PFM, V_{BYP} = 5V, L = 1.5µH/CSAB1040A-1R5M)



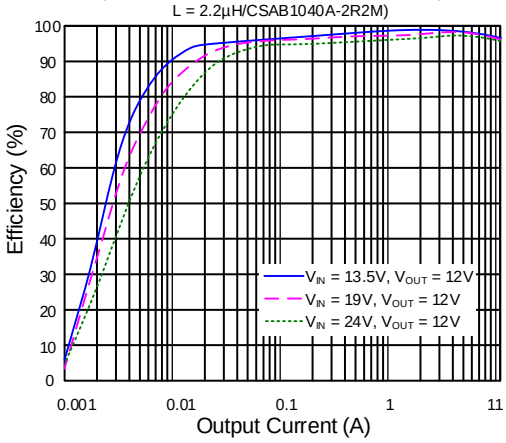
Buck Efficiency vs. Output Current
(I_{OUT} = 0.001A ~ 11A, USM, V_{BYP} = 5V, L = 1.5µH/CSAB1040A-1R5M)



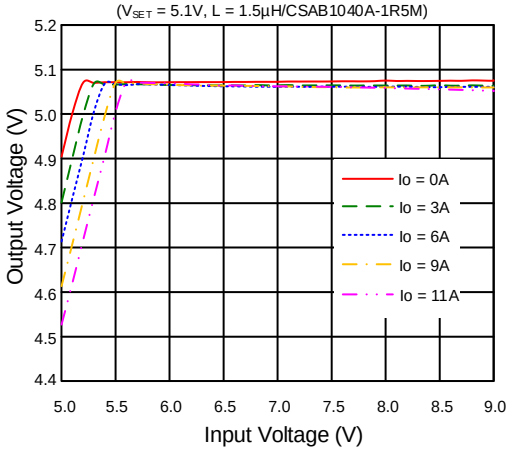
Buck Efficiency vs. Output Current
(I_{OUT} = 0.001A ~ 11A, PFM, V_{BYP} = 5V, C_{FF} = 47pF, L = 2.2µH/CSAB1040A-2R2M)



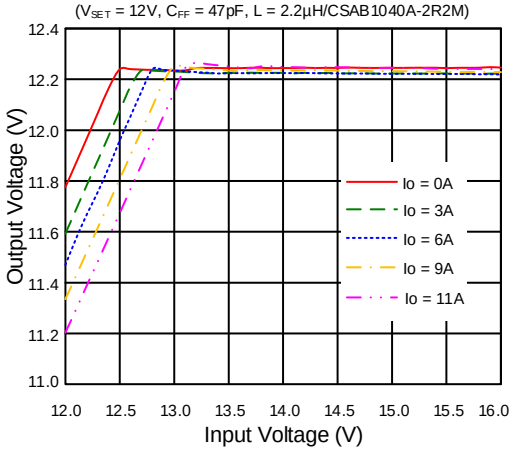
Buck Efficiency vs. Output Current
(I_{OUT} = 0.001A ~ 11A, USM, V_{BYP} = 5V, C_{FF} = 47pF, L = 2.2µH/CSAB1040A-2R2M)



Line Regulation
(V_{SET} = 5.1V, L = 1.5µH/CSAB1040A-1R5M)



Line Regulation
(V_{SET} = 12V, C_{FF} = 47pF, L = 2.2µH/CSAB1040A-2R2M)



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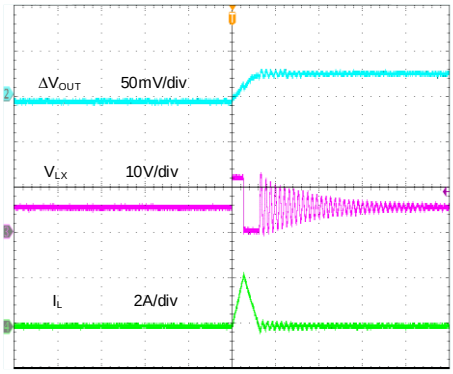
Output Ripple

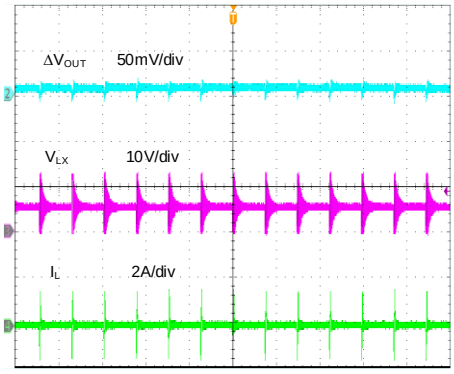
(V_{IN} = 12V, V_{OUT} = 5.1V, I_{OUT} = 0A, PFM)



Time (2μs/div)

Output Ripple

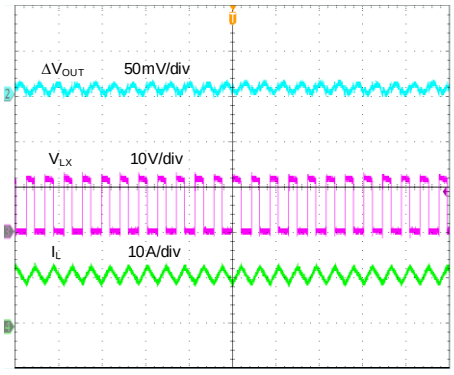
(V_{IN} = 12V, V_{OUT} = 5.1V, I_{OUT} = 0A, USM)



Time (40μs/div)

Output Ripple

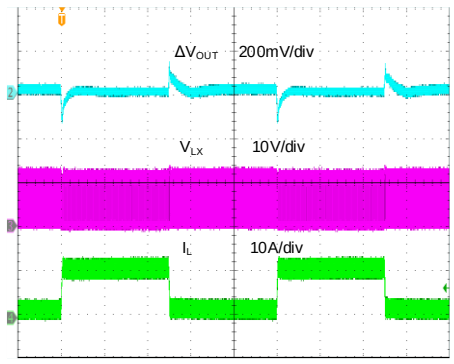
(V_{IN} = 12V, V_{OUT} = 5.1V, I_{OUT} = 11A)



Time (4μs/div)

Load Transient

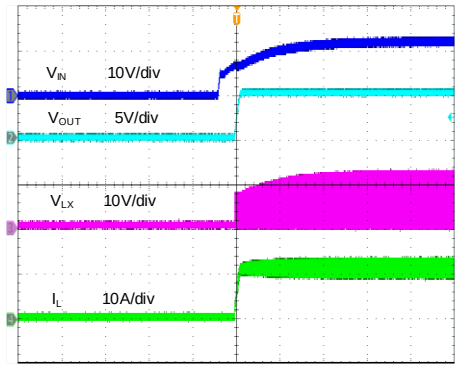
(V_{IN} = 12V, V_{OUT} = 5.1V, I_{OUT} = 1.1 ~ 11A, PFM)



Time (200μs/div)

Startup from V_{IN}

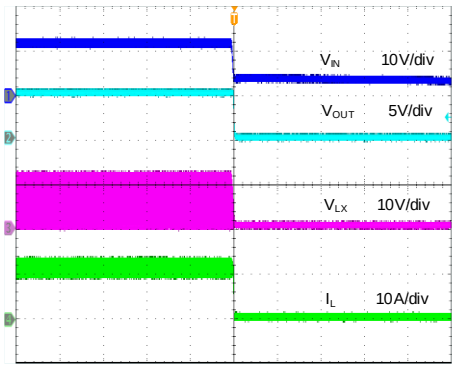
(V_{IN} = 12V, V_{OUT} = 5.1V, I_{OUT} = 11A)



Time (4ms/div)

Shutdown from V_{IN}

(V_{IN} = 12V, V_{OUT} = 5.1V, I_{OUT} = 11A)



Time (4ms/div)

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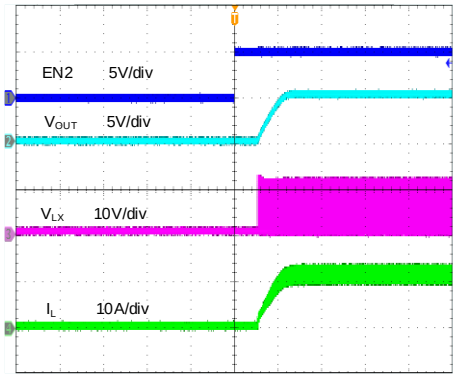
Startup from EN2

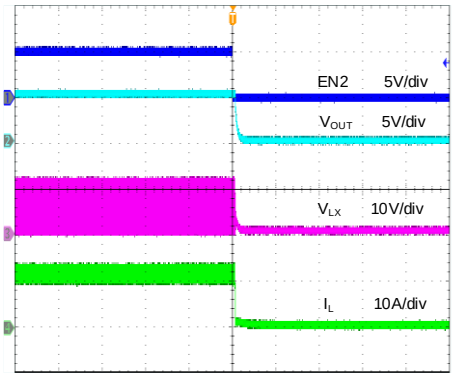
(V_{IN} = 12V, V_{OUT} = 5.1V, I_{OUT} = 11A)



Time (800µs/div)

Shutdown from EN2

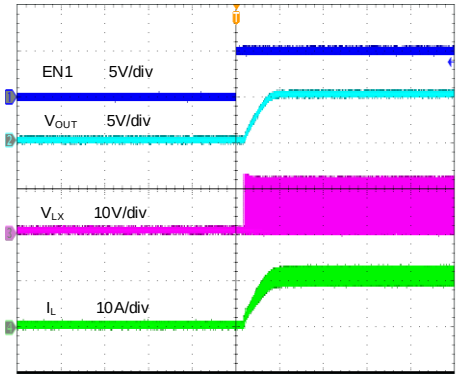
(V_{IN} = 12V, V_{OUT} = 5.1V, I_{OUT} = 11A)



Time (800µs/div)

Startup from EN1

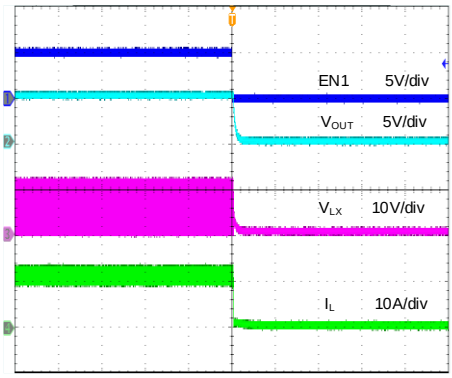
(V_{IN} = 12V, V_{OUT} = 5.1V, I_{OUT} = 11A)



Time (800µs/div)

Shutdown from EN1

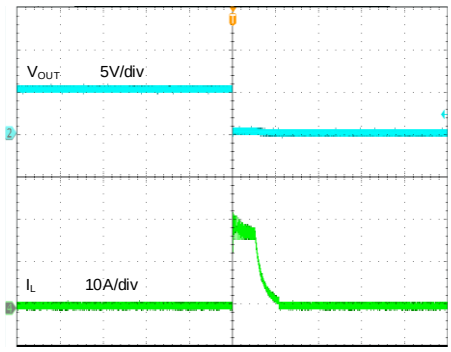
(V_{IN} = 12V, V_{OUT} = 5.1V, I_{OUT} = 11A)



Time (800µs/div)

Output Short Circuit Protection

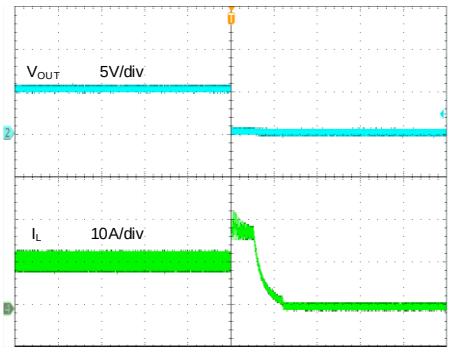
(V_{IN} = 12V, V_{OUT} = 5.1V, I_{OUT} = 0A ~ Short)



Time (400µs/div)

Output Short Circuit Protection

(V_{IN} = 12V, V_{OUT} = 5.1V, I_{OUT} = 11A ~ Short)



Time (400µs/div)

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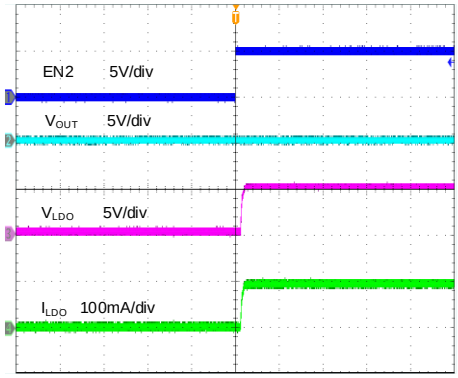
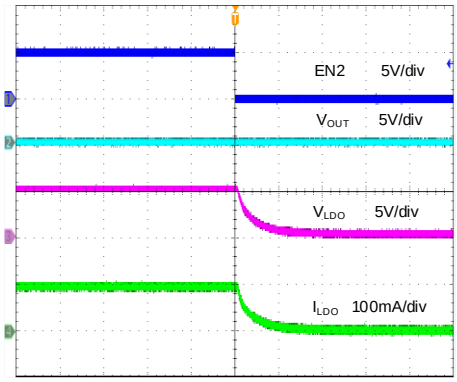
LDO Startup from EN2

(V_{IN} = 12V, I_{LDO} = 100mA, EN1 = Low)



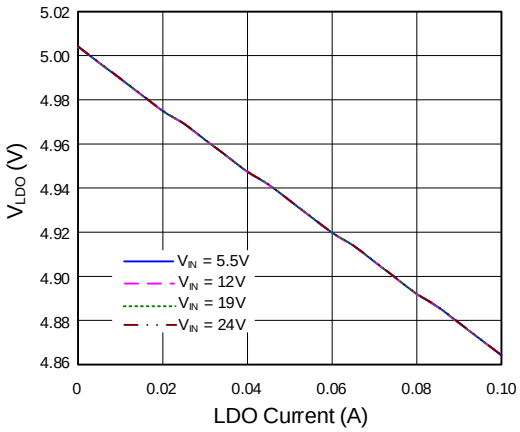
LDO Shutdown from EN2

(V_{IN} = 12V, I_{LDO} = 100mA, EN1 = Low)



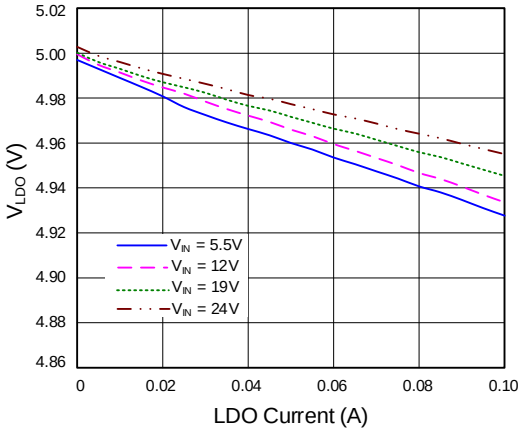
LDO Load Regulation(BYP ON)

(EN2 = High, EN1 = Low, V_{BYP} = 5V)



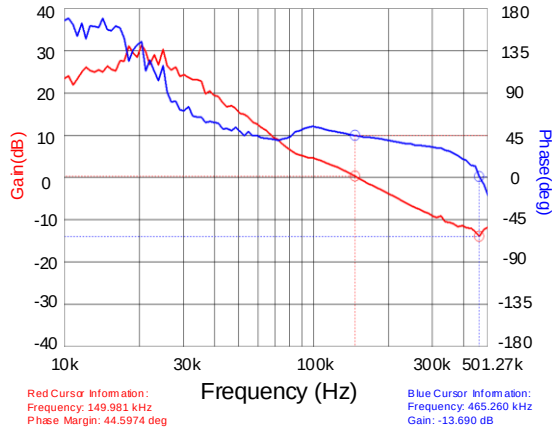
LDO Load Regulation(BYP OFF)

(EN2 = High, EN1 = Low, V_{BYP} = 0V)



Bode Plot

(V_{IN} = 12V, V_{OUT} = 5.1V, I_{OUT} = 5.5A)



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Detailed Description

General Features

Constant On-Time Architecture

Fundamental to any constant-on-time (COT) architecture is the one-shot circuit or on-time generator, which determines how long to turn on the top MOSFET. Each on-time (t_{ON}) is a "fixed" voltage ratio,

$$t_{ON} = \frac{V_{OUT}}{V_{IN}} \times \frac{1}{f_{SW}}$$

For example, considering that a hypothetical converter targets 5.1V output from a 12V input at 600kHz, the target on-time is

$$\frac{5.1\text{V}}{12\text{V}} \times \frac{1}{600\text{kHz}} = 708.33\text{ns}$$

Each t_{ON} pulse is triggered by the feedback comparator when the output voltage as measured at FB node drops below the regulated value. After one t_{ON} period, a minimum off-time ($t_{OFF,MIN}$) is imposed before any further switching is initiated, even if the output voltage is lower than the regulated value. This approach avoids making any switching decisions during the noisy periods just after switching events and while the switching node (LX) is rapidly rising or falling.

In a COT architecture, there is no fixed clock, so the top MOSFET can turn on almost immediately after a load transient and subsequent switching pulses can be quickly initiated, ramping the inductor current up to meet load requirements with minimal delays.

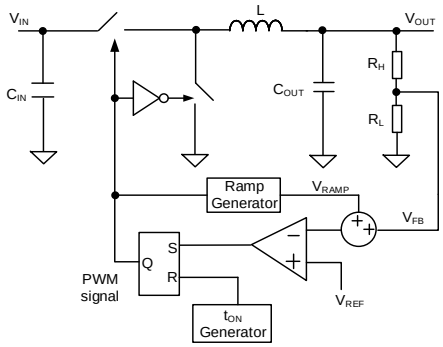
Minimum Duty Cycle and Maximum Duty Cycle

In the COT architecture, there is no limitation for operating the part at low duty cycle, since in this case, when the on-time is close to the minimum on time, the switching frequency can be reduced as needed to always ensure a proper operation.

The device allows on-time stretching for increasing the duty cycle under high duty cycle operation. When the device detects the feedback voltage lower than the target, it will increase the on-time as long as needed. The maximum on-time can be up to 6μs. This function is disabled when the feedback voltage is less than the UVP threshold.

With the on-time stretch function, the device can support up to 98% duty cycle operation, across the entire junction temperature range of -40°C ~ 125°C.

Instant-PWM Operation



Silergy's COT ripple-based control strategy adds several proprietary improvements to the traditional COT architecture. Whereas most legacy based on COT implementations require a dedicated connection to the output voltage terminal to calculate the t_{ON} duration, instant-PWM control method derives this signal internally. Another improvement optimizes operation with low ESR ceramic output capacitors. In many applications it is desirable to utilize very low ESR ceramic output capacitors, but legacy COT regulators may become unstable in these cases because the beneficial ramp signal that results from the inductor current flowing into the output capacitor maybe become too small to maintain smooth operation. For this reason, instant-PWM synthesizes a virtual replica of this signal internally. This internal virtual ramp and the feedback voltage are combined and compared to the reference voltage. When the sum is lower than the reference voltage, the t_{ON} pulse is triggered as long as the minimum off-time has been satisfied and the inductor current as measured in the bottom MOSFET is lower than the bottom MOSFET current limit threshold. As the t_{ON} pulse is triggered, the bottom MOSFET turns off and the top MOSFET turns on. Then the inductor current ramps up linearly during the t_{ON} period. At the conclusion of the t_{ON} period, the top MOSFET turns off, the bottom MOSFET turns on and the inductor current ramps down linearly. This action also initiates the minimum off-time timer to ensure sufficient time for stabilizing any transient conditions and settling the feedback comparator before the next cycle is initiated. This minimum off-time is relatively short so that during high speed load transient t_{ON} can be retriggered with minimal delay, allowing the inductor current to ramp quickly to provide sufficient energy to the load side.

In order to avoid shoot-through, a dead time (t_{DEAD}) is generated internally between the top MOSFET off and the bottom MOSFET on period or the bottom MOSFET off and the bottom MOSFET on period.

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Light Load Operation Mode Selection

PFM or USM light load operation is selected using the EN1 pin. EN1 is a dual purpose input serving as the buck converter enable pin but also as mode selection pin to control operation mode of the buck converter under light load conditions, after its output is within the regulated range. If the voltage on this pin is lower than 1.6V and higher than 1V, the buck converter operates in ultra-sonic mode (USM). If the voltage on this pin is higher than 2.2V, the buck converter operates using pulse-frequency modulation (PFM) mode.

If PFM light load operation is selected, under light load conditions, typically when the load satisfies the following equation,

$$I_{OUT_CTL} = \frac{\Delta I_L}{2} = \frac{V_{OUT} \times (1 - D)}{2 \times f_{SW} \times L} \qquad (1)$$

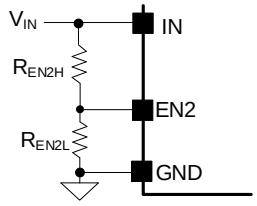
the current through the bottom MOSFET will ramp to near zero before the next t_{ON} time. When this occurs, the bottom MOSFET turns off, preventing recirculation current that can seriously reduce efficiency under these light load conditions. As load current is further reduced, the combined feedback and ramp signals remain much higher than the reference voltage, the instant-PWM control loop will not trigger another t_{ON} until needed, and the apparent operating switching frequency will correspondingly drop, improving efficiency. The switching frequency can be lower than audible frequency area under deep light load or null load conditions. Continuous conduction mode (CCM) resumes smoothly as soon as the load current increases sufficiently for the inductor current to remain above zero at the time of the next t_{ON} cycle. The buck converter enters CCM once the load current exceeds the threshold shown in (1). Above the threshold, the switching frequency stays fairly constant over the output current range.

If USM light load operation is selected, the control loop keeps the switching frequency above the audible frequency range, even under deep light load or null load conditions.

Input Under Voltage Lockout (UVLO)

To prevent operation before the internal circuitry is ready and to ensure that the top and bottom MOSFETs can be properly driven, the device incorporates an input undervoltage lockout protection.

The device remains in a low current state and LX node switching actions and LDO are inhibited until V_{IN} exceeds the UVLO (rising) threshold. At that time, if EN2 is high, the LDO starts operating, and if EN1 is also high, the buck converter is enabled and soft-start ramp is initiated. If V_{IN} falls below $V_{IN,UVLO}$ less than the input UVLO hysteresis, LX node switching actions and LDO will again be suppressed.



Increasing the default input UVLO threshold can be implemented using an external resistor divider connected to EN2.

EN1/EN2 Control

The devicehas two enable pins to control the buck converter and LDO.

The buck converter and LDO are all turned off under S4/S5 state (EN2 = Low, EN1 = High or Low). Under S3 state (EN2 = High, EN1 = Low), only LDO output is turned on while the buck converter is turned off. Under S0 state (EN2 = High, EN1 = High), the buck regulator and LDO are all turned on. Only if EN2 is high could LDO be turned on, and only if EN1 and EN2 are both high could the buck converter be turned on. See EN1/EN2 logic details in below table:

EN2	EN1	STATE	LDO	BUCK
High	High	S0	On	On
High	Low	S3	On	Off
Low	Low/High	S4/S5	Off	Off

The EN2/EN1 inputs are high-voltage capable inputs with logic-compatible threshold. EN2/EN1 logic high is defined as a voltage higher than 1V, and a logic low as a voltage lower than 0.4V. When the device is turned off, the shutdown current I_{SHDN} is below 12μA.

It is not recommended to connect EN2 or EN1 pin to V_{IN} or another voltage source directly. A resistor in a range of 1kΩ to 1MΩ should be used for EN2/EN1 pin in this case.

Startup and Shutdown

The device incorporates an internal soft-start circuit to smoothly ramp the buck converter output to the desired voltage whenever the device is enabled. Internally, the soft-start circuit clamps the output at zero and then allows the output to rise to the desired voltage over approximately 0.8ms, which avoids high current flow and transients during startup. The startup and shutdown sequence are shown below:

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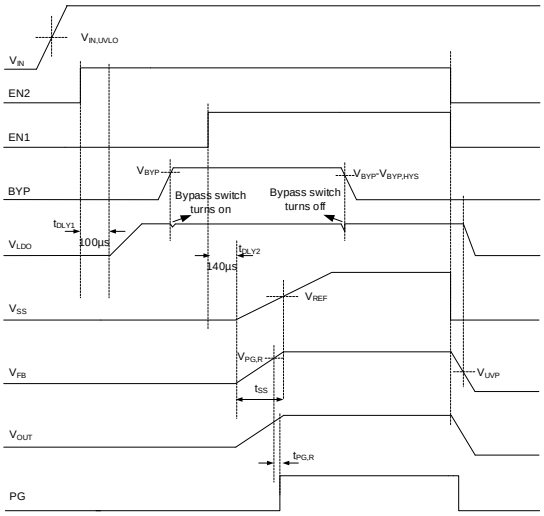


After V_{IN} exceeds the UVLO rising threshold, the internal LDO is turned on after the delay time t_{DLY1} if EN2 is high, the buck converter is turned on after the delay time t_{DLY2} if EN1 is also high. When the output voltage is 90% of the regulated value, PG is set to the high-impedance state after the delay time $t_{PG,R}$. LDO output switches to the BYP if BYP voltage is higher than bypass switch turn on voltage. LDO output will switch to internal LDO when BYP voltage is lower than V_{BYP} - $V_{BYP,HYS}$.

The device supports startup with pre-biased output. If the output is pre-biased to a certain voltage before startup, the buck converter disables the switching of both the top MOSFET and the bottom MOSFET until the internal soft-start voltage V_{SS} exceeds the sensed output voltage at the FB node. The first pulse on-time is internally calculated based the input voltage and pre-biased output voltage.

PG Power Good Indicator

PG is an open drain output controlled by a window comparator connected to OUT. If the voltage is higher than $V_{PG,R}$ and less than V_{OVP} for at least the power good delay time (low to high), PG will be set to high-impedance state.

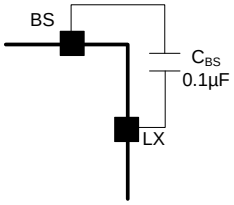
PG should be connected to V_{IN} or another voltage source through a resistor (e.g., 100kΩ). After V_{IN} rises until the internal initial power is ready, the PG internal MOSFET is turned on so that PG is actively driven low before output voltage is ready. After the feedback voltage V_{FB} reaches $V_{PG,R}$, PG is set to high-impedance state after a delay time of 200µs (typ.). When V_{FB} drops to $V_{PG,F}$, or rises above V_{OVP} for the OVP delay time, PG is driven low after a delay time of 40µs (typ.).

Buck Output Auto-Discharge Function

The device discharges the output voltage when the buck converter shuts down due to low V_{IN} or EN2/EN1, or caused by a protection function being triggered, so that the output voltage can be discharged in a minimal time, even if the buck output load current is zero. The discharge MOFET in parallel with the bottom MOSFET turns on after the bottom MOSFET turns off when the shutdown logic is enabled. The output discharge current is typically 100mA for V_{OUT} = 5.1V. The discharge MOSFET is not active outside of these shutdown conditions.

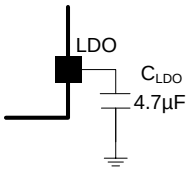
External Bootstrap Capacitor

This device integrates a floating power supply for the gate driver of the top MOSFET. Proper operation requires a 0.1µF low ESR ceramic capacitor to be connected between BS and LX. This bootstrap capacitor provides the gate driver supply voltage for the N-channel top MOSFET.



LDO Output

The device integrates a high performance, low drop-out linear regulator (LDO) and its output voltage set-point is fixed to 5V, which can power the internal 3.6V VCC, and also power the external peripherals with up to 100mA of current. This LDO is intended mainly as an auxiliary 5V supply for notebook systems, when in standby mode. When the input voltage exceeds the UVLO rising threshold, and EN2 is high, LDO is turned on and supplied power by V_{IN}. When the BYP input voltage exceeds bypass switch turn on voltage, the internal LDO regulator will be turned off and the bypass switch will be turned on so that LDO output switches over to BYP to reduce power consumption. Connect a 4.7µF low ESR ceramic capacitor from LDO to GND.



VCC Output

The device integrates a high performance, low drop-out linear regulator 3.6V VCC, which can power the internal gate drivers, PWM logic, analog circuitry and other blocks. VCC is supplied by the LDO. Connect a 2.2µF low ESR ceramic capacitor from VCC to GND. Make sure the loop formed by the VCC capacitor is shorter than the loop for the LDO capacitor, if there is placement conflict between them.

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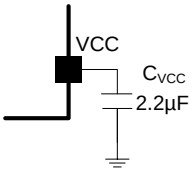
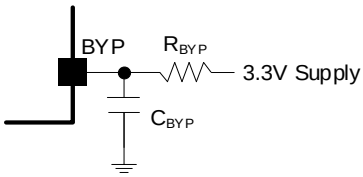


BYP Input

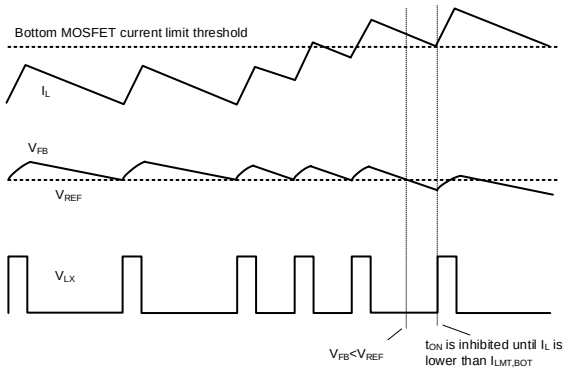
When a 5V external power supply is connected to the BYP, the internal LDO is automatically turned off. The overall efficiency may be improved by using an external power supply. Connect a 1μF low ESR ceramic capacitor from BYP pin to GND. Using an external low pass filter consisting of a small value resistor R_{BYP} and a ceramic capacitor C_{BYP} is recommended for applications where the external power rail has significant ripple. Connect the pin to GND or leave floating if not used.



Fault Protection Modes

Buck Output Current Limit

The buck converter features cycle-by-cycle “valley” current limit (bottom MOSFET current limit). The Inductor current is monitored in the bottom MOSFET when it turns on and as the inductor current ramps down. If the monitored current is higher than current limit threshold, t_{ON} is inhibited until the current returns back to below the threshold.



The buck converter features cycle-by-cycle “valley” current limit (bottom MOSFET current limit). The Inductor current is monitored in the bottom MOSFET when it turns on and as the inductor current ramps down. If the monitored current is higher than current limit threshold, t_{ON} is inhibited until the current returns back to below the threshold.

When the valley current limit occurs, the output current limit value is

$$I_{LMT,OUT} = I_{LMT,BOT} + \frac{\Delta I_L}{2}$$

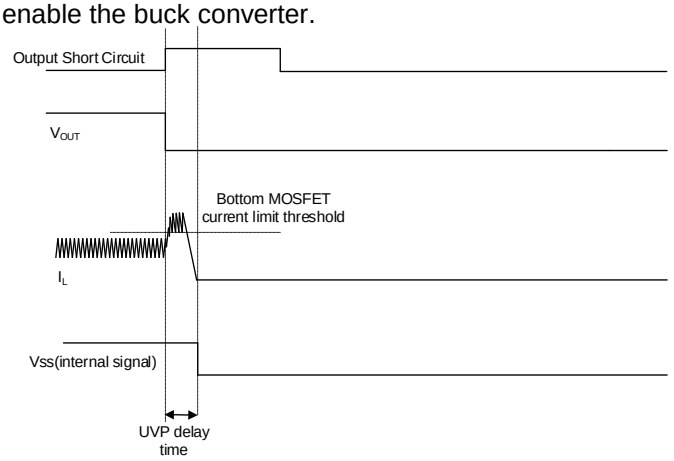
$$\Delta I_L = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times f_{SW} \times L}$$

The valley current limit protection limits the inductor current, but the OCP itself is a non-latched protection. When the load current is higher than the bottom MOSFET current limit threshold by one half of the peak-to-peak inductor ripple current, the output voltage starts to drop. When the feedback voltage falls below the under voltage protection (UVP) threshold, and continues for the UVP delay time, the buck converter will be disabled and enter latch-off state. Independent from this mechanism, the over temperature protection may also be triggered under the over current condition and the buck converter will be disabled and enter latch-off state.

The buck converter also features cycle-by-cycle peak current limit (top MOSFET current limit). During the t_{ON} time, the top MOSFET current is monitored. If it exceeds the current limit threshold, the MOSFET will be turned off, and the bottom MOSFET will be turned on. t_{ON} can be not inhibited when the bottom MOSFET current is lower than the bottom MOSFET current limit threshold.

Buck Output Under Voltage Protection (UVP)

If V_{OUT} < ~33% of the regulated value for approximately 200μs occurring when the output short circuit or the load current is much higher than the maximum current capacity, the output under voltage protection (UVP) will be triggered, and the buck converter will be disabled and set to a latch-off state. Cycle EN2 or EN1 input to re-enable the buck converter.



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Buck Output Over Voltage Protection (OVP)

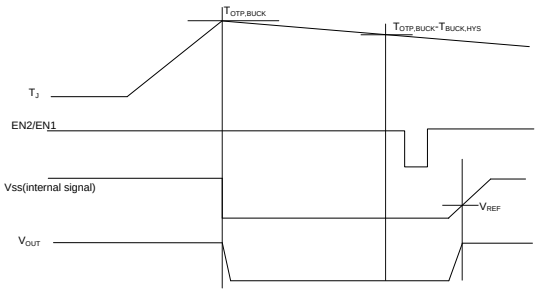
The buck converter includes output over voltage protection (OVP). If the feedback voltage rises above the reference voltage level, the top MOSFET naturally remains off and different actions are taken depending on the operation mode.

When operating in PFM light load mode, if the feedback voltage remains high, the bottom MOSFET remains on until the inductor current reaches zero and the LX node switching actions are suppressed. If the feedback voltage doesn't exceed the over voltage protection threshold, the LX node switching actions will be resumed when the combined feedback and ramp signals become lower than the reference voltage. If the feedback voltage exceeds the over voltage protection threshold for the OVP delay time, the output over voltage protection (OVP) will be triggered, and the buck converter will be disabled and enter latch off state. Cycle EN2 or EN1 input to re-enable the buck converter.

When operating in USM light load mode, if the feedback voltage remains high, the bottom MOSFET turn on time will be longer and inductor current average value becomes more and more negative until the reverse current limit is triggered, trying to make output voltage lower. If the feedback voltage exceeds the OVP threshold for the OVP delay time, the protection will be triggered, and the buck converter will be disabled and enter latch off state. Cycle EN2 or EN1 input to re-enable the buck converter. False OVP triggers may happen under USM light load conditions, if the inductance value is chosen too low.

Buck Over Temperature Protection (OTP)

The buck converter includes over temperature protection (OTP) circuitry to prevent overheating due to excessive power dissipation. When the thermal sensor detects a junction temperature exceeding 150°C, the over temperature protection (OTP) will be triggered, and the buck converter will be disabled and enter a latch off state. In this case the LDO is not disabled. Cycle EN2 or EN1 to re-enable the buck converter after the junction temperature cools down about 15°C. For continuous operation, provide adequate thermal dissipation so that the junction temperature does not exceed the OTP threshold.



LDO Output Current Limit

The device features LDO current limit to guarantee LDO safe operation in all operating conditions. When the LDO output voltage is less than the target value after LDO is turned on, the internal LDO regulator or bypass switch will operate in current limit mode until the LDO output voltage is reaches the target. For example, when a LDO output short circuit occurs, the LDO will operate in a current limit mode. The LDO will switch to normal operation after the short circuit condition is removed.

LDO Over Temperature Protection

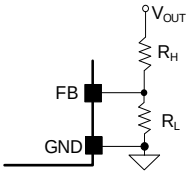
The device also features auto-recovery mode LDO over temperature protection to guarantee LDO safe operation when under increased power dissipation. When the LDO thermal sensor detects that the junction temperature exceeds 160°C, the LDO will be turned off. When the junction temperature cools down by approximately 25°C, the LDO will be turned on and the buck converter will also recover from a latch off state.

Design Procedure

Feedback Resistor Divider Selection

Choose R_H and R_L to program the proper output voltage. To minimize the power consumption under light loads, it is desirable to choose large resistance values for both R_H and R_L. A value of between 10kΩ and 1MΩ is strongly recommended for both resistors. If V_{SET} is 5.1V, R_H = 100kΩ is chosen, then using following equation, R_L can be calculated to be 13.3kΩ.

$$R_L = \frac{0.6V}{V_{SET} - 0.6V} \times R_L$$



Buck Input Capacitor Selection

Input filter capacitors are needed to reduce the ripple voltage on the input, to filter the switched current drawn from the input supply and to reduce potential EMI. When selecting an input capacitor, be sure to select a voltage rating at least 20% greater than the maximum voltage of the input supply and a temperature rating above the system requirements. X5R series ceramic capacitors are most often selected due to their small size, low cost, surge current capability and high RMS current ratings over a wide temperature and voltage range. However, systems that are powered by a wall adapter or other long and therefore inductive cabling may be susceptible to significant inductive ringing at the input to the device. In these cases, consider adding some bulk capacitance like electrolytic, tantalum or polymer type capacitors. Using a combination of bulk capacitors (to reduce overshoot or

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ringing) in parallel with ceramic capacitors (to meet the RMS current requirements) is helpful in these cases.

Consider the RMS current rating of the input capacitor, paralleling additional capacitors if required to meet the calculated RMS ripple current,

$$I_{CIN_RMS} = I_{OUT} \times \sqrt{D \times (1-D)}$$

The worst-case condition occurs at D = 0.5, then

$$I_{CIN_RMS,MAX} = \frac{I_{OUT}}{2}$$

For simplification, choose an input capacitor with an RMS current rating greater than half of the maximum load current.

The input capacitance value determines the input voltage ripple of the converter. If there is an input voltage ripple requirement in the system, choose an appropriate input capacitor that meets the specification. Given the very low ESR and ESL of ceramic capacitors, the input voltage ripple can be estimated by

$$V_{CIN_RIPPLE,CAP} = \frac{I_{OUT}}{f_{SW} \times C_{IN}} \times D \times (1-D)$$

The worst-case condition occurs at D = 0.5, then

$$V_{CIN_RIPPLE,CAP,MAX} = \frac{I_{OUT}}{4 \times f_{SW} \times C_{IN}}$$

The capacitance value is less important than the RMS current rating. In most applications two 10μF X5R capacitors are sufficient. Take care to locate the ceramic input capacitor as close to the device IN and GND pin as possible.

Buck Inductor Selection

The inductor is necessary to supply constant current to the output load while being driven by the LX node.

The buck converter operates well over a wide range of inductance values. This flexibility allows for optimization to find the best trade-off between efficiency, cost and size for a particular application. Selecting a low inductance value will help reduce size and cost and enhance transient response, but will increase peak inductor ripple current, reducing efficiency and increasing output voltage ripple. The low DC resistance (DCR) of these low inductance value inductors may help reduce DC losses and increase efficiency. Choosing higher inductance value inductors tend to have higher DCR and will slow down transient response.

A reasonable compromise between size, efficiency, and transient response can be determined by selecting a ripple current (ΔI_L) about 20% ~ 50% of the desired full output load current. Start calculating the approximate inductor value by selecting the input and output voltages, the operating frequency (f_{SW}), the maximum output current ($I_{OUT,MAX}$) and estimating a ΔI_L as some percentage of that current.

$$L = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times f_{SW} \times \Delta I_L}$$

Use this inductance value to determine the actual inductor ripple current (ΔI_L) and required peak current inductor current $I_{L,PEAK}$.

$$\Delta I_L = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times f_{SW} \times L}$$

$$I_{L,PEAK} = I_{OUT,MAX} + \frac{\Delta I_L}{2}$$

Select an inductor with a saturation current and thermal rating in excess of $I_{L,PEAK}$.

If USM light load operation is selected, make sure the inductor value is high enough to avoid reverse current limit threshold is been triggered just under steady state if the load current is zero.

For highest efficiency, select an inductor with a low DCR that meets the inductance, size and cost targets. Low loss ferrite materials should be considered.

Buck Inductor Design Example

Consider a typical design for a device providing 5.1V_{OUT} at 11A from 12V_{IN}, operating at 600kHz and using target inductor ripple current (ΔI_L) of 40% or 4.4A. Determine the approximate inductance value at first:

$$L = \frac{5.1V \times (12V - 5.1V)}{12V \times 600kHz \times 4.4A} = 1.11\mu H$$

Next, select the nearest standard inductance value, in this case 1.5μH, and calculate the resulting inductor ripple current (ΔI_L):

$$\Delta I_L = \frac{5.1V \times (12V - 5.1V)}{12V \times 600kHz \times 1.5\mu H} = 3.26A$$

$$I_{L,PEAK} = 11A + \frac{3.26A}{2} = 12.63A$$

The resulting 3.26A ripple current is 3.26A/11A is 29.64%, well within the 20% ~ 50% target.

$$I_{L,PEAK,RVS} = \frac{3.26A}{2} = 1.63A < I_{LMT,RVS}$$

Finally, select an available inductor with a saturation current higher than the resulting $I_{L,PEAK}$ of 12.63A.

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Buck Output Capacitor Selection

The buck converter provides excellent performance with a wide variety of output capacitor types. Ceramic and POS types are most often selected due to their small size and low cost. Total capacitance is determined by the transient response and output voltage ripple requirements of the system.

Buck Steady State Output Ripple

Steady state output voltage ripple at the switching frequency is caused by the inductor current ripple (ΔI_L) on the output capacitors ESR (ESR ripple) as well as the stored charge (capacitive ripple). When considering total ripple, both should be considered.

$$V_{RIPPLE,\ ESR} = \Delta I_L \times ESR$$

$$V_{RIPPLE,\ CAP} = \frac{\Delta I_L}{8 \times C_{OUT} \times f_{SW}}$$

Consider a typical application with ΔI_L = 3.26A using four 22μF ceramic capacitors, each with an ESR of ~6mΩ for parallel total of 88μF and 1.5mΩ ESR.

$$V_{RIPPLE,\ ESR} = 3.26A \times 1.5m\Omega = 4.89mV$$

$$V_{RIPPLE,\ CAP} = \frac{3.26A}{8 \times 88\mu F \times 600kHz} = 7.72mV$$

Total ripple = 12.61mV. The actual capacitive ripple may be higher than calculated value because the capacitance decreases with the voltage on the capacitor.

Using a 150μF 40mΩ POS cap, the above result is

$$V_{RIPPLE,\ ESR} = 3.26A \times 40m\Omega = 130.40mV$$

$$V_{RIPPLE,\ CAP} = \frac{3.26A}{8 \times 150\mu F \times 600kHz} = 4.53mV$$

Total ripple = 134.93mV

Buck Output Transient Undershoot/Overshoot

If very fast load transient must be supported, consider the effect of the output capacitor on the output transient undershoot and overshoot. Instant-PWM responds quickly to changing load conditions, however, some considerations must be needed, especially when using small ceramic capacitors which have low capacitance at low output voltages which results in insufficient stored energy for load transient. Output transient undershoot and overshoot have two causes: voltage changes caused by the ESR of the output capacitor and voltage changes caused by the output capacitance and inductor current slew rate.

ESR undershoot or overshoot may be calculated as

$$V_{ESR} = \Delta I_{OUT} \times ESR$$

Using the ceramic capacitor example above and a fast load transient of ± 5.5A, V_{ESR} = ± 5.5A × 1.5mΩ = ± 8.25mV. The POS capacitor result with the same load transient, V_{ESR} = ± 5.5A × 40mΩ = ± 220mV.

Capacitive undershoot (load increasing) is a function of the output capacitance, the load step, the inductor value and the input-output voltage difference and the maximum duty factor. During a fast load transient, the maximum duty factor of instant-PWM is a function of t_{ON} and the minimum t_{OFF} as the control scheme is designed to rapidly ramp the inductor current by grouping together many t_{ON} pulses in this case. The maximum duty factor D_{MAX} may be calculated by

$$D_{MAX} = \frac{t_{ON}}{t_{ON} + t_{OFF,MIN}}$$

Given this, the capacitive undershoot may be calculated by

$$V_{UNDERSHOOT,CAP} = -\frac{L \times \Delta I^2{}_{OUT}}{2 \times C_{OUT} \times \left(V_{IN,MIN} \times D_{MAX} - V_{OUT}\right)}$$

Consider a 5.5A load increase using the ceramic capacitor case when V_{IN} = 12V. At V_{OUT} = 5.1V, the result is t_{ON} = 708.33ns, $t_{OFF,MIN}$ = 150ns, D_{MAX} = 708.33 / (708.33 + 150) = 0.825 and

$$V_{UNDERSHOOT,CAP} = -\frac{1.5\mu H \times (5.5A)^2}{2 \times 88\mu F \times (12V \times 0.825 - 5.1V)} = -53.71mV$$

Using the POS capacitor case, the above result is

$$V_{UNDERSHOOT,CAP} = -\frac{1.5\mu H \times (5.5A)^2}{2 \times 150\mu F \times (12V \times 0.825 - 5.1V)} = -31.51mV$$

Capacitive overshoot (load decreasing) is a function of the output capacitance, the inductor value and the output voltage.

$$V_{OVERSHOOT,CAP} = \frac{L \times \Delta I^2{}_{OUT}}{2 \times C_{OUT} \times V_{OUT}}$$

Consider a 5.5A load decrease using the ceramic capacitor case above. At V_{OUT} = 5.1V the result is

$$V_{OVERSHOOT,CAP} = \frac{1.5\mu H \times (5.5A)^2}{2 \times 88\mu F \times 5.1V} = 50.55mV$$

Using the POS capacitor case, the above result is

$$V_{OVERSHOOT,CAP} = \frac{1.5\mu H \times (5.5A)^2}{2 \times 150\mu F \times 5.1V} = 29.66mV$$

Combine the ESR and capacitive undershoot and overshoot to calculate the total overshoot and undershoot for a given application. If the system requirements are not met, recalculate with a different configuration.

Load Transient Considerations

The device uses the COT ripple-based control strategy to achieve good stability and fast transient response. In applications with high step load current, adding an RC

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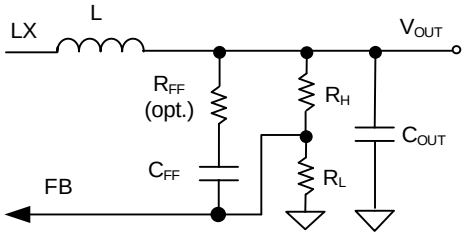
network R_{FF} and C_{FF} between the OUT pin and the FF pin may further speed up the load transient response. R_{FF} = 1kΩ and C_{FF} = 47 ~ 220pF have been shown to perform well in most applications. Increasing C_{FF} will speed up the load transient response if there is no stability issue.



Note: For C_{OUT} > 500μF and when the minimum load current is low, use feedforward values of R_{FF} = 1kΩ and C_{FF} = 2.2nF to provide sufficient ripple to FB node for low output ripple and good transient behavior.

Thermal Design Considerations

Maximum power dissipation depends on the thermal resistance of the IC package, the PCB layout, the surrounding airflow, and the difference between the junction and ambient temperatures. The maximum power dissipation may be calculated by:

$$P_{D,MAX} = \frac{T_{J,MAX} - T_A}{\theta_{JA}}$$

Where, $T_{J,MAX}$ is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction to ambient thermal resistance.

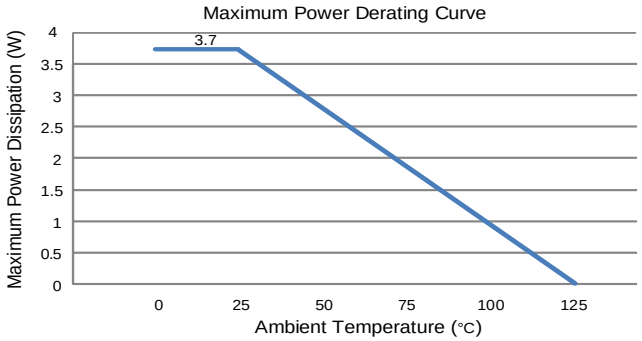
To comply with the recommended operating conditions, the maximum junction temperature is 125°C. The junction to ambient thermal resistance θ_{JA} is layout dependent. For the QFN3×4-13 package the thermal resistance θ_{JA} is 27°C /W when measured on a standard Silergy 8.5cm×8.5cm size four-layer thermal test board. These standard thermal test layouts have a very large area with long 2-oz. copper traces connected to each IC pin and very large, unbroken 1-oz. internal power and ground planes.

Meeting the performance of the standard thermal test board in a typical tiny evaluation board area requires wide copper traces well-connected to the IC's backside pads leading to exposed copper areas on the component side of the board as well as good thermal via from the exposed pad connecting to a wide middle-layer ground plane and, perhaps, to an exposed copper area on the board's solder side.

The maximum power dissipation at T_A = 25°C may be calculated by the following formula:

$$P_{D,MAX} = \frac{125°C - 25°C}{27°C/W} = 3.7W$$

The maximum power dissipation depends on operating ambient temperature for fixed $T_{J,MAX}$ and thermal resistance θ_{JA}. Use the derating curve in figure below to calculate the effect of rising ambient temperature on the maximum power dissipation.



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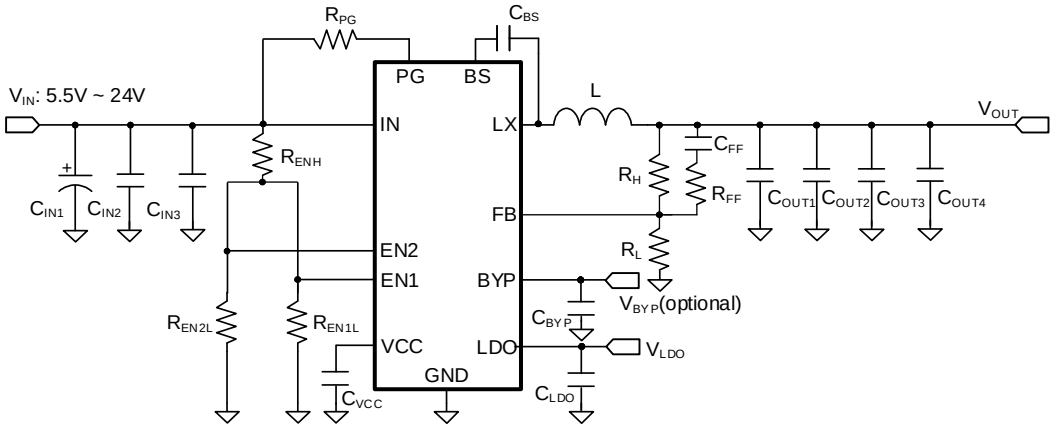
Application Schematic (V_{OUT} = 5.1V)



BOM List

Designator	Description	Part Number	Manufacturer
C_{IN1}	47μF/50V, Electrolytic Capacitor		
C_{IN2}	10μF/50V/X5R, 1206	GRM31CR61H106KA12L	mμRata
C_{IN3}, C_{BS}	0.1μF/50V/X5R, 0603	GRM188R61H104KA93D	mμRata
C_{OUT1}, C_{OUT2}, C_{OUT3}, C_{OUT4}	22μF/16V/X5R, 1206	GRM31CR61C226ME15L	mμRata
C_{VCC}	2.2μF/16V/X5R, 0603	GRM188R61C225KE15D	mμRata
C_{FF}	220pF/50V/C0G, 0603	GRM1885C1H221JA01D	mμRata
C_{BYP}	1.0μF/25V/X5R, 0603	GRM155R61E105KE11D	mμRata
C_{LDO}	4.7μF/25V/X5R, 1206	GRM319R61E475KA12D	mμRata
L	1.5μH/16A, inductor	PCMB104T-1R5MS	CYNTEC
R_H, R_{PG}	100kΩ, 1%, 0603		
R_L	13.3kΩ, 1%, 0603		
R_{ENH}	10kΩ, 1%, 0603		
R_{EN1L}, R_{EN2L}	1MΩ, 1%, 0603		
R_{FF}	1kΩ, 1%, 0603		

Recommend Table for Typical Applications

V_{OUT}(V)	R_H(kΩ)	R_L(kΩ)	C_{FF}(pF)	L/Part Number
5.1	100	13.3	220	1.5μH/PCMB104T-1R5MS
12	100	5.23	47	2.2μH/PCMB104T-2R2MS

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Layout Design

Follow these PCB layout guidelines for optimal performance and thermal dissipation.

Input Capacitors: Place the input capacitor very near IN and GND, minimizing the loop formed by these connections. And the input capacitor should be connected to the IN and GND by wide copper plane. A 0.1μF input ceramic capacitor is recommended to reduce the input noise.

Output Capacitors: Guarantee the C_{OUT} negative sides are connected with GND pin by wide copper traces instead of vias, in order to achieve better accuracy and stability of output voltage.

VCC and LDO Capacitor: Place the VCC/LDO capacitor close to VCC/LDO pin using short, direct copper trace to one nearest device GND pin (pin 11). Make sure the loop formed by VCC capacitor is shorter than LDO capacitor if there is position conflict between them.

BYP Capacitor: Place the BYP capacitor close to BYP using short, direct copper trace to one nearest device GND pin (pin 11) if bypass function is used. Keep bypass line width at least 20mil as it is also the 100mA LDO's bypass input.

Feedback Network and Output Line: Place the feedback components (R_{FF} and C_{FF}) as close to FB pin as possible. Avoid routing the feedback line near LX, BS or other high frequency signal as it is noise sensitive. Make the feedback sampling point Kelvin connect with C_{OUT} rather than the inductor output terminal.

LX Connection: Keep LX area small to prevent excessive EMI, while providing wide copper traces to minimize parasitic resistance and inductance. Wide LX copper trace between pin 2 and pin 12 should be adopted to improve efficiency.

BS Capacitor: Place the BS capacitor on the same layer as the device, keep the BS voltage path (BS, LX and C_{BS}) as short as possible.

Control Signals: It is not recommended to connect control signals to V_{IN} or another voltage source directly. A resistor in a range of 1kΩ to 1MΩ should be used if they are pulled high.

GND Vias: Place adequate number of vias on the GND layer around the device for better thermal performance. Especially, make one good thermal heating GND copper trace and add several GND vias around pin 3 and pin 11.

PCB Board: A four-layer layout with 2-oz copper is strongly recommended to achieve better thermal performance. The top layer and bottom layer should place power IN and GND copper plane as wide as possible. Middle1 layer should place all GND layer for conducting heat and shielding middle2 layer signal line from top layer crosstalk. Place signal lines on middle2 layer instead of the other layers, so that the other layers' GND plane not be cut apart by these signal lines.

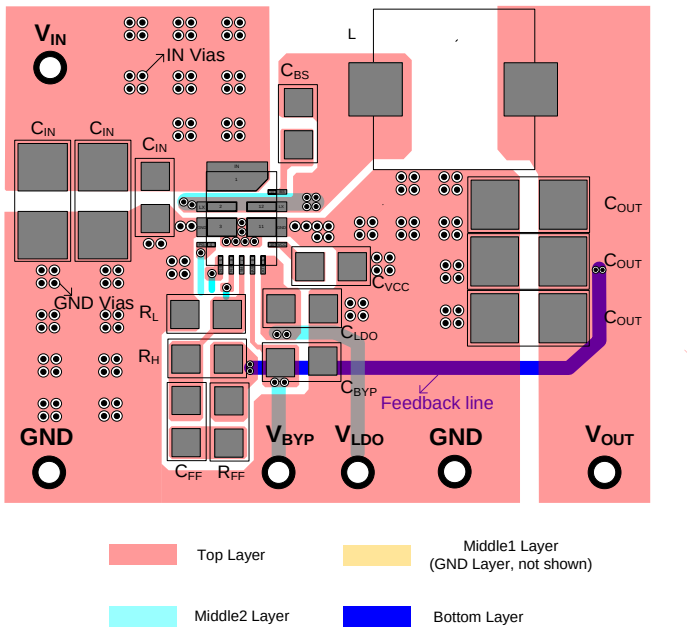

Figure4. PCB Layout Suggestion

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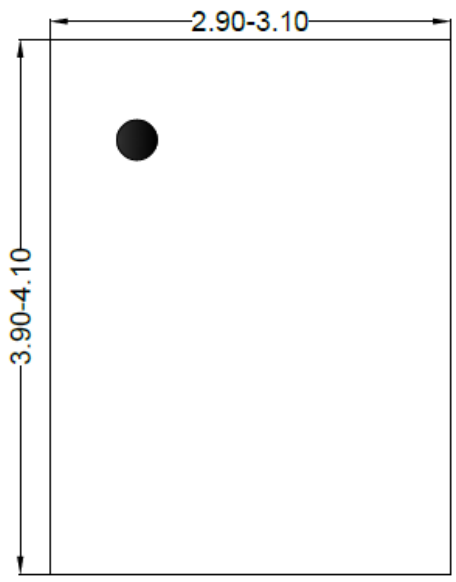
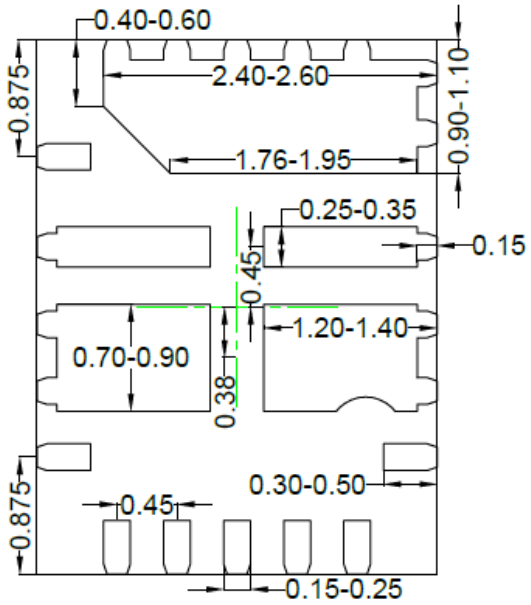
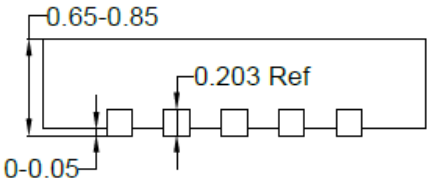
QFN3×4-13 Package Outline Drawing



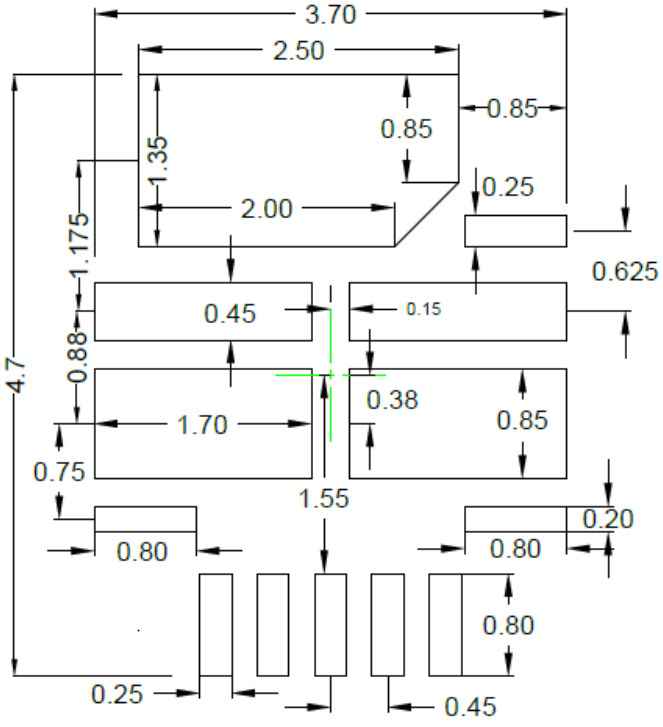
Top View



Bottom View



Front View



Recommended PCB layout
(Reference only)

Notes: 1, All dimension in millimeter and exclude mold flash & metal burr;
2, center line on drawing refers to the chip body center

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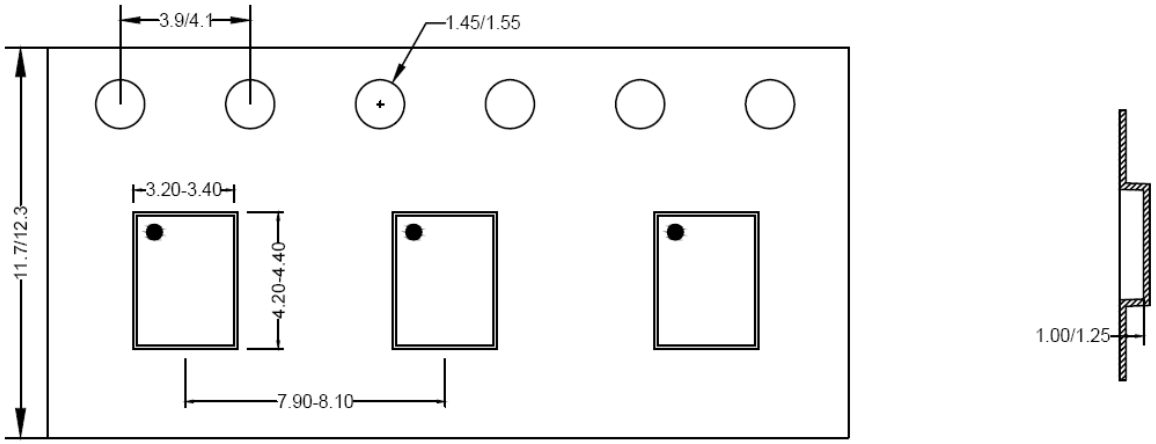
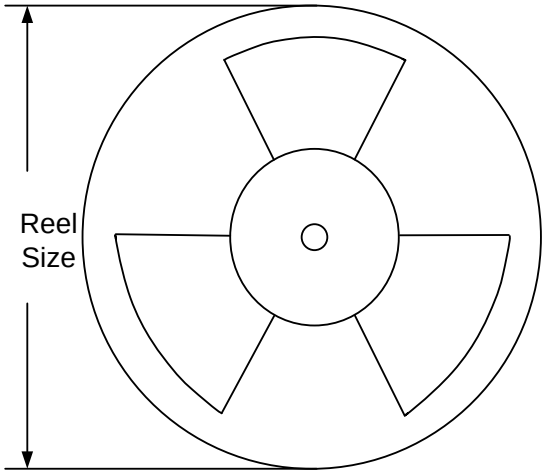
Taping & Reel Specification

1. QFN3×4-13 taping orientation



Feeding direction →

2. Carrier Tape & Reel specification for packages



Package types	Tape width (mm)	Pocket pitch(mm)	Reel size (Inch)	Trailer length(mm)	Leader length (mm)	Qty per reel
QFN3×4	12	8	13"	400	400	5000

3. Others: NA

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Revision History

The revision history provided is for informational purposes only and is believed to be accurate; however, it is not warrantied. Please make sure that you have the latest revision.

Date	Revision	Change
Feb. 19, 2024	Rev. 1.0	Initial Release

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