

### General Description

The SY205269SLD is a single-line, unidirectional TVS (transient voltage suppressor) designed to provide ESD (electrostatic discharge) protection for various applications. The device safeguards sensitive electronic components from ESD and other transient events. It complies with IEC 61000-4-2 (ESD) ( $\pm 30\text{kV}$  air,  $\pm 30\text{kV}$  contact discharge) and IEC 61000-4-5 (surge) 100A (8/20 $\mu\text{s}$ ) standards.

The SY205269SLD is available in a compact DFN 1.6mm $\times$ 1.0mm-2pin package.

### Features

- Operating Voltage: 5V and below
- Capacitance: 600pF(Typical)
- Transient Protection for a Single line
  - IEC 61000-4-2 (ESD)  $\pm 30\text{kV}$  (Air) $\pm 30\text{kV}$  (Contact)
  - IEC 61000-4-5 (Surge) 100A (8/20 $\mu\text{s}$ )
- Protects One Control or Power Line
- Low Clamping Voltage

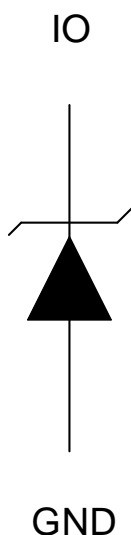
### Applications

- VBUS and VBAT Lines
- Desktops, Servers and Laptops
- Smartphones
- Microprocessor-Based equipment
- Portable Instrumentation

### Mechanical Characteristics

- DFN1.6 $\times$ 1.0-2 package
  - Marking: Device Code, Date Code.
  - Packaging: Tape and Reel
- 

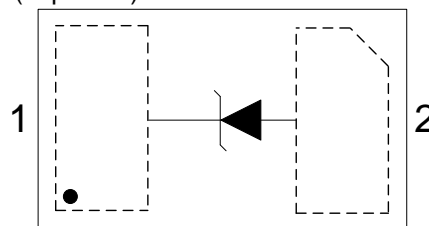
### Circuit Diagram



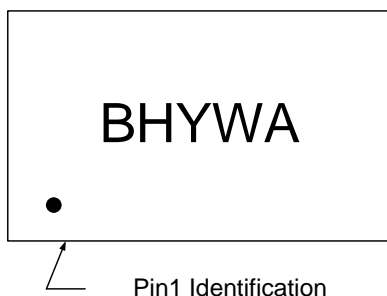
## Ordering Information

Part Number	Package Type	Top Mark
SY205269SLD	DFN1.6x1.0-2	BHYWA

## Pinout (Top View)



## Marking Codes



**Note 1:** “BH” is the device code, fixed.

**Note 2:** “YWA” is the date code.

## Pin Descriptions

Device Pins	Pin Name	Description
1	Input/Output	IO
2	GND	GND

## Absolute Maximum Rating

Parameter	Symbol	Min	Max	Unit
ESD per IEC 61000-4-2 (Air)	$V_{ESD}$	-30	30	kV
ESD per IEC 61000-4-2 (Contact)		-30	30	
Peak Pulse Power ( $t_p=8/20\mu s$ )	$P_{PK}$		800	W
Operating Temperature	$T_{OPT}$	-40	+125	°C
Storage Temperature	$T_{STG}$	-55	+150	°C

## Electrical Characteristics $T_A = 25^\circ C$

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Nominal Reverse Working Voltage	$V_{RWM}$				5.0	V
Reverse Leakage Current at $V_{RWM}$	$I_R$	$V_{RWM} = 5V, T_A = 25^\circ C$			3	$\mu A$
Reverse Breakdown Voltage at $I_R$	$V_{BR}$	$I_T = 1mA, \text{Pin1 to Pin2}$	5.5		8	V
Forward voltage	$V_F$	$I_F = 1mA, \text{Pin2 to Pin1}$	0.4		1.2	V
Clamping Voltage at $I_{PP}$	$V_C^1$	$I_{PP} = 16A, t_p = 10/100ns$		5.5		V
Clamping Voltage at $I_{PP}$	$V_C^1$	$I_{PP} = 100A, t_p = 8/20us$		8		V
Dynamic Resistance	$R_{DYN}^{1,2}$	$t_p = 10/100ns$		0.01		$\Omega$
Parasitic Capacitance	$C_{ESD}^1$	$V_R = 0V, f = 1MHz$		600		pF

**Note 1:** Guaranteed by design and not subject to production test.

**Note 2:**  $R_{DYN}$  calculated based on  $I_{PP}=8A$  to  $I_{PP}=16A, t_p = 10/100ns$ .

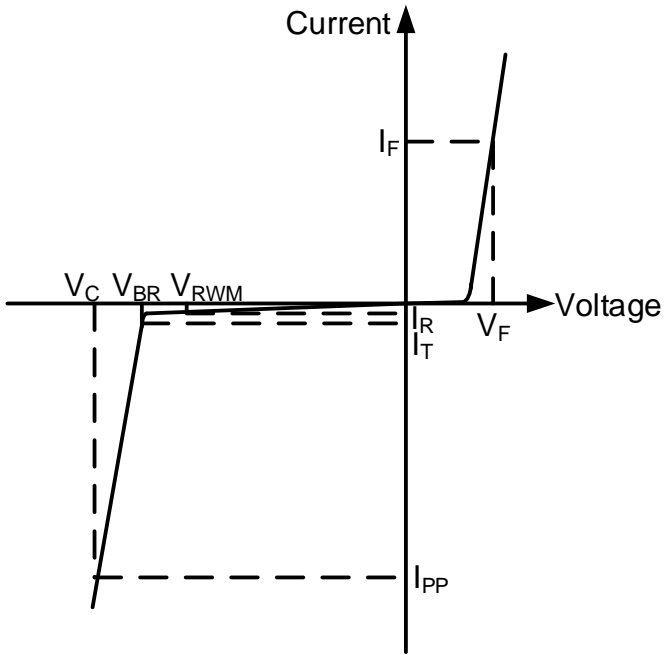
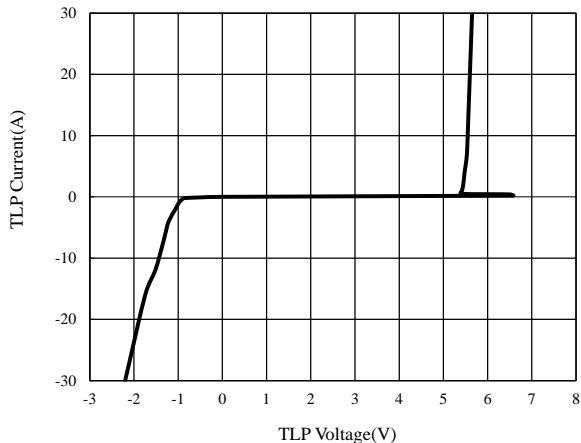


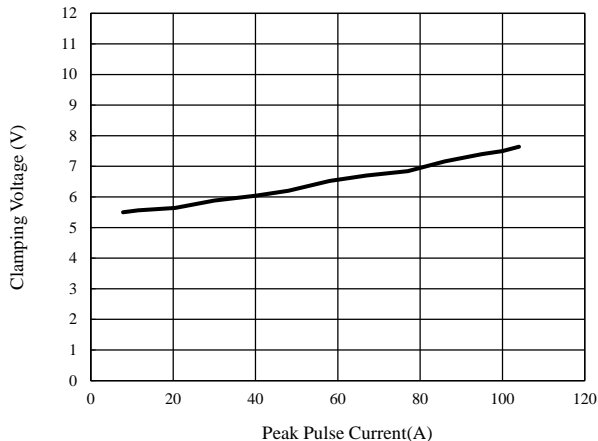
Figure 1. Uni-directional TVS

## Typical Characteristics

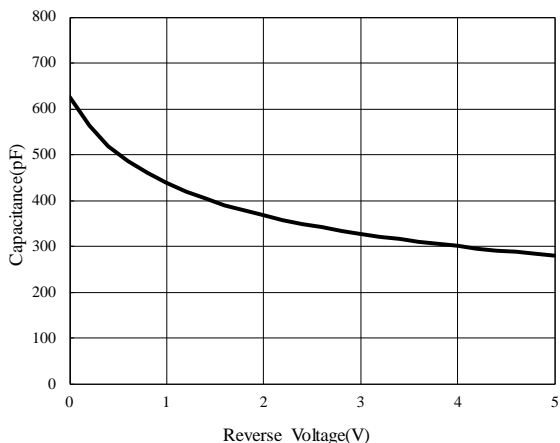
### TLP Testing of IO to GND



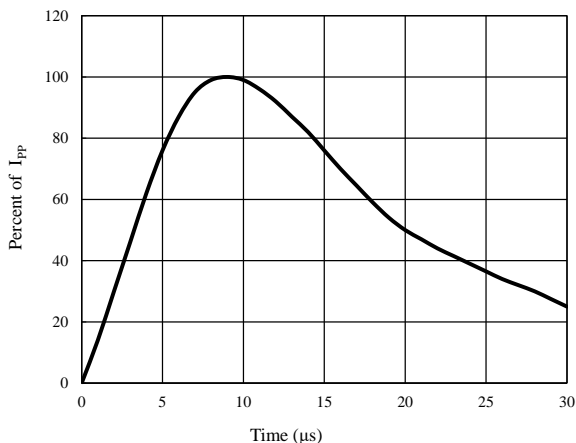
### Clamping Voltage vs. Peak Pulse Current (8/20μs)



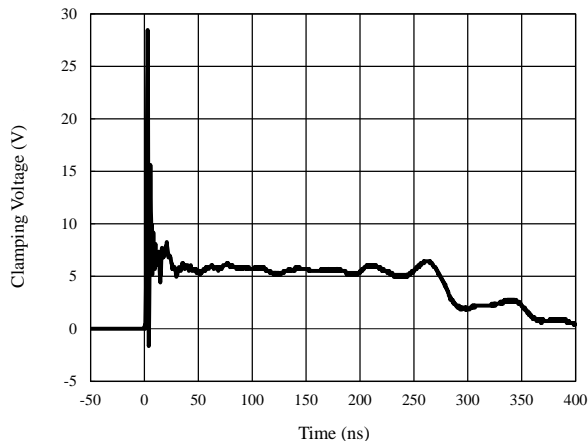
### Capacitance vs. Reverse Voltage



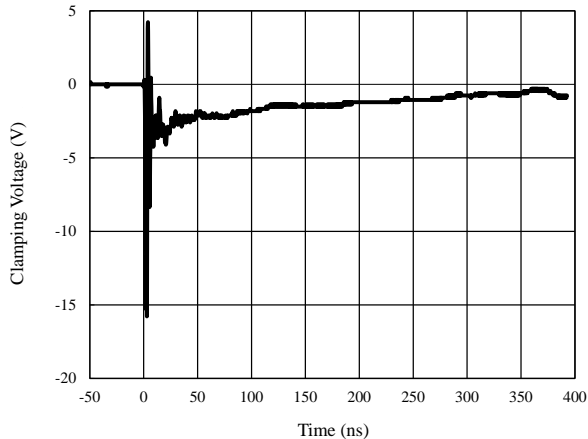
### 8/20μs Pulse Waveform



### ESD Clamping of IO to GND (+8kV Contact per IEC 61000-4-2)



### ESD Clamping of IO to GND (-8kV Contact per IEC 61000-4-2)



## Application Information

### Pin Connection in PCB

The SY205269SLD can protect one uni-directional line. It can be used to protect a single power or VBAT line. The pin connections are shown in Figure 2.

The single power or VBAT line can be connected directly to Pin1. Pin2 of the SY205269SLD is the negative reference pin, which should connect to the GND. The connection traces should be as short as possible to minimize parasitic inductance.

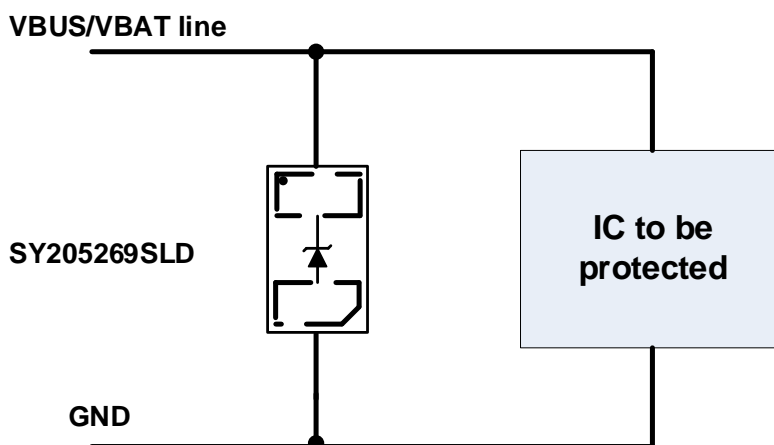


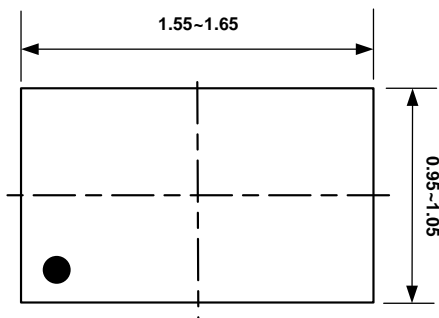
Figure 2. SY205269SLD Pin Connection in PCB

### PCB Layout Guidelines

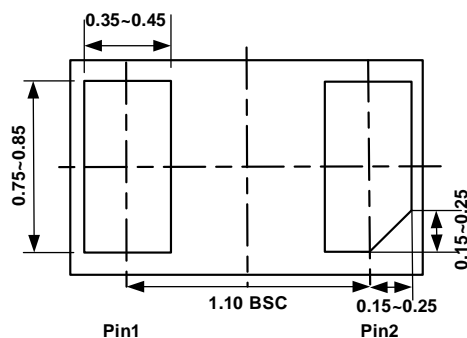
For optimum ESD protection and circuit performance, the following PCB layout guidelines are recommended:

- The distance between Pin2 and the PCB GND should be as short as possible to reduce the ESD transient return path to GND.
- Use large vias to connect Pin1 and Pin2 to the PCB VCC and GND.
- Place the SY205269SLD as close to the connector or battery port as possible to reduce parasitic inductance and reduce ESD coupling into adjacent traces

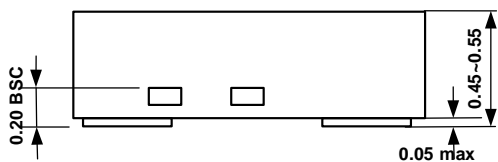
## DFN1.6x1.0-2 Package Outline



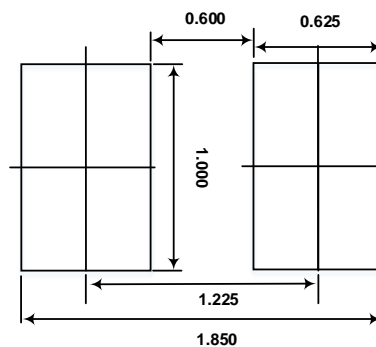
Top View



Bottom View



Side View

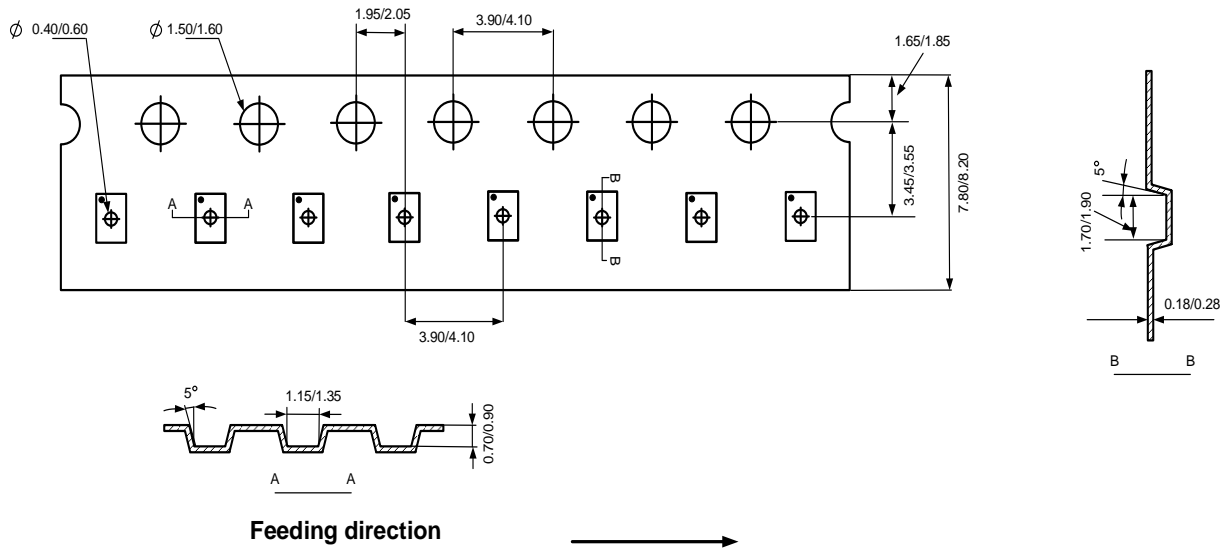


Recommended PCB Layout

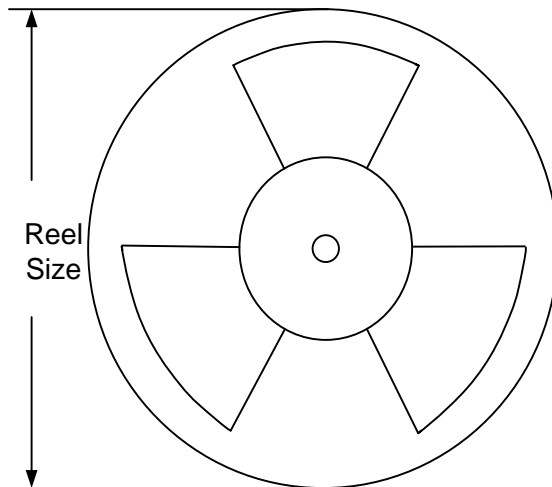
Note: All dimensions are in millimeters and exclude mold flash and metal burr..

## Taping & Reel Specification

### DFN1.6x1.0-2 Taping Orientation



### Carrier Tape & Reel Specification for Packages



Package Types	Tape Width (mm)	Pocket Pitch(mm)	Reel Size (Inch)	Qty per Reel(pcs)
DFN1.6x1.0-2	8	4	7"	3000



**Revision History**

The revision history provided is for informational purpose only and is believed to be accurate, however, not warranted. Please make sure that you have the latest revision.

Revision Number	Revision Date	Description	Pages changed
1.0	Mar 27, 2024	Initial Release	



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