SA24406/SA24406E

High Efficiency, 36V Input, 6A Synchronous Step-Down Regulator

General Description

The SA24406x is a high efficiency synchronous step-down DC-DC regulator with internal power and synchronous rectifier MOSFETs. It operates using fixed frequency and peak current control over a wide input voltage range of 4V to 36V, and can deliver up to 6A of continuous output current.

The SA24406x is specially designed with a symmetric QFN package and adjustable LX rise time to achieve good EMI performance. The switching frequency can be adjusted from 300kHz to 2.2MHz, or synchronized to an external clock. The frequency can be selected to meet application EMI limits and to avoid noise in important frequency bands.

The SA24406x offers excellent efficiency over a wide range of applications by providing internal 41mΩ power and 21mΩ synchronous rectifier MOSFETs and an external bias input. The 1μA shutdown supply current allows the device to be used in battery powered applications. The SA24406x ensures safe operation in all operating conditions, providing cycle-by-cycle current limit, input undervoltage lockout, internal soft-start, output undervoltage and overvoltage protection, and thermal shutdown.

The SA24406x is available in a QFN3.5×4-14 package and pin-to-pin compatible with SA24404 (automotive, 36V/4A, PFM).

Features

- 4V to 36V Input Voltage Range
- 6A Output Current Capability
- Low $R_{DS(ON)}$ for Internal MOSFETs: 41mΩ Top, 21mΩ Bottom
- 30μA Quiescent Current (SA24406 Typical)
- 1μA Shutdown Current (Typical)
- 300kHz to 2.2MHz Switching Frequency
- Synchronization to External Clock
- Spread Spectrum Function
- Hiccup Mode Output Short-Circuit Protection
- EN On/Off Control with Accurate Threshold
- Cycle-by-Cycle Peak Current Limit
- Power Good Indicator
- Operating Mode at Light Load
  - SA24406: PFM
  - SA24406E: FCCM
- 1V ±1% Reference Voltage Over -40˚C to 150˚C Temperature Range
- Package: QFN3.5×4-14 with Wettable Flanks
- Automotive AEC- Q100 Grade 1 Certified

Applications

- Automotive
- Industrial
- High Voltage DC/DC Converters

Typical Application

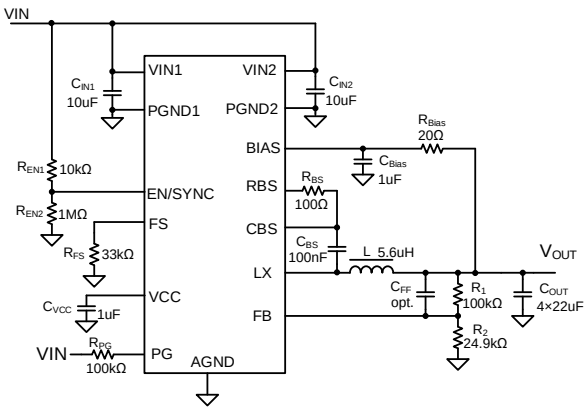

Figure 1. Schematic Diagram

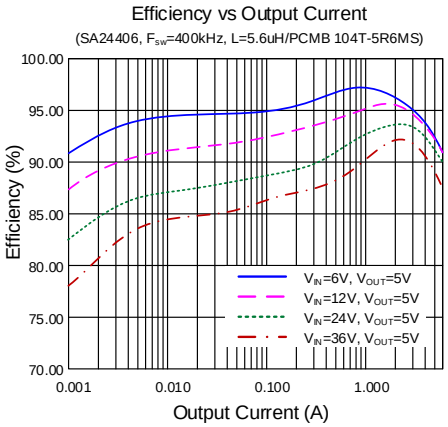

Figure 2. Efficiency vs. Output Current

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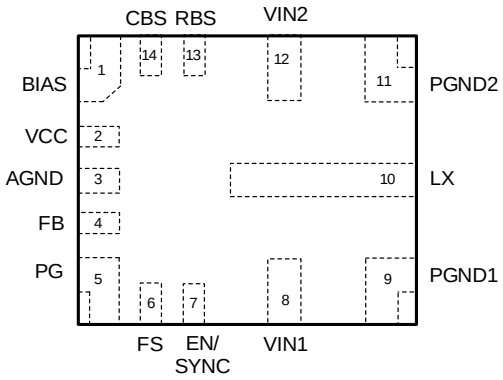
Ordering Information

Ordering Part Number	Package Type	Top Mark
SA24406XNQ	QFN3.5×4-14 RoHS-Compliant and Halogen-Free	**GLD*xyz***
SA24406EXNQ	QFN3.5×4-14 RoHS-Compliant and Halogen-Free	**AAFC*xyz***

x = year code, y = week code, z = lot number code

Pinout (top view)



(QFN3.5×4-14)

Pin Description

Pin Number	Pin Name	Pin Description
1	BIAS	Input to internal LDO. Connect this pin to the output for improved efficiency. Place a ceramic capacitor with a value of 1μF or higher between BIAS and GND for improved noise immunity.
2	VCC	Decouple this pin to GND with at least a 1μF ceramic capacitor.
3	AGND	Analog ground. Connect this pin to both PGND1 and PGND2 on the PCB.
4	FB	Output Feedback Pin. Connect this pin to the center point of the output resistor divider to program the output voltage: $V_{OUT} = 1\times(1 + R_1/R_2)$.
5	PG	Power good indicator, open-drain output. PG is externally pulled high when the FB pin voltage is between 95.5% and 115% of the reference voltage. The PG pin is internally driven low when the FB pin voltage is lower than 94% or greater than 120% of the reference voltage.
6	FS	Oscillator frequency programming pin. Connect an external resistor to GND to set the switching frequency f_{SW}. $f_{SW}(kHz) = 1.346 \times 10^4/(R_{FS}(k\Omega) + 0.444)$.
7	EN/SYNC	Enable control. Pull high to enable the device, pull low to disable the device. This pin can be used as an adjustable UVLO if it is connected to V_{IN} and GND through a resistor divider. Do not leave floating. EN/SYNC also functions as a synchronization input. When it is connected to an external clock, the internal oscillator synchronizes to the external clock, and the device functions in forced PWM mode.
8	VIN1	Input pin 1. Decouple this pin to GND with at least a 10μF ceramic capacitor.
9	PGND1	Power ground pin 1. Connect this pin to both PGND2 and AGND on the PCB.
10	LX	Inductor pin. Connect this pin to the switching node of the inductor.
11	PGND2	Power ground pin 2. Connect this pin to both PGND1 and AGND on the PCB.
12	VIN2	Input pin 2. Decouple this pin to GND with at least a 10μF ceramic capacitor.
13	RBS	Connect to CBS through a resistor. This resistance can be used to determine LX node rise time.
14	CBS	Bootstrap pin. Supply high side gate driver. Connect a 0.1μF capacitor between this and the LX pin.

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Block Diagram

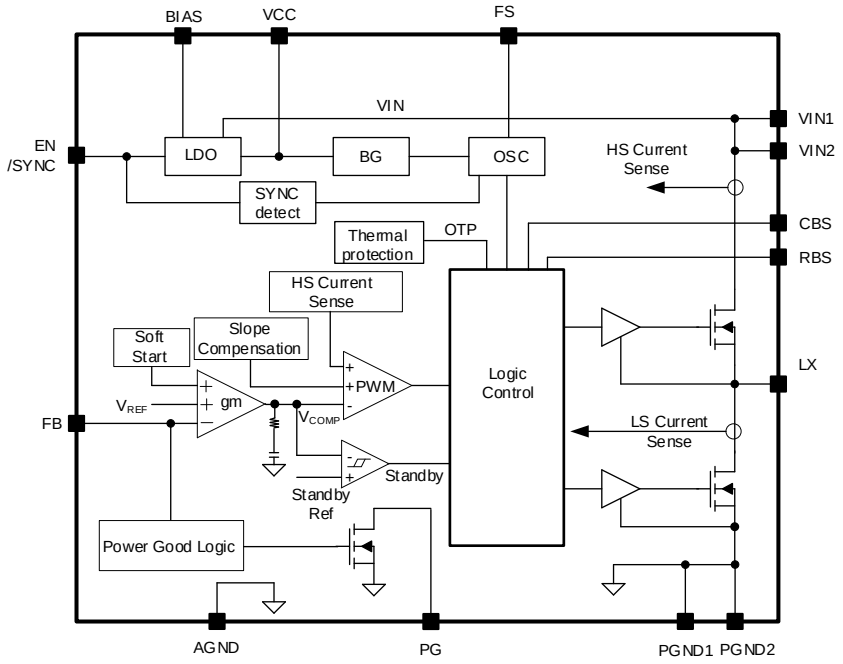

Figure 3. Block Diagram

Absolute Maximum Ratings

Parameter (Note 1)	Min	Max	Unit
VIN1, VIN2, EN/SYNC, LX, FB, FS, PG	-0.3	40	V
BIAS	-0.3	16	
CBS-LX, RBS-LX	-0.3	4	
VCC	-0.3	4	
Dynamic LX Voltage in 20ns Duration	GND - 5	IN + 5	
Junction Temperature Range	-40	170	°C
Ambient Temperature Range	-40	125	
Lead Temperature (Soldering, 10s)		260	
Storage Temperature Range	-65	150	
ESD Susceptibility			
HBM (Human Body Model)		±2000	V
CDM (Charged Device Model)		±750	

Thermal Information

Parameter (Note 2)	Typ	Unit
θ_{JA} Junction-to-Ambient Thermal Resistance	31.5	°C/W
$\theta_{JC(top)}$ Junction-to-Case (Top) Thermal Resistance	16	
θ_{JB} Junction-to-Board Thermal Resistance	14	
P_D Power Dissipation T_A = 25°C	4	W

Recommended Operating Conditions

Parameter (Note 3)	Min	Max	Unit
Input Voltage	4	36	V
Junction Temperature T_J	-40	150	°C

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Electrical Characteristics

(V_{IN} = 12V, T_J = -40°C to +150°C. Typical values are at T_J = 25°C, unless otherwise specified. The values are guaranteed by test, design or statistical correlation. (**Note 4**))

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Input Voltage Range	V_{IN}		4		36	V
Input UVLO Threshold	V_{UVLO}		3.4		3.9	V
Input UVLO hysteresis	V_{HYS}			0.2		V
Quiescent Current	I_Q	SA24406 EN high, non-switching, V_{FB}=105% V_{REF} T_J = -40°C to 150°C		30		μA
		SA24406E EN high, switching, V_{FB}=95% V_{REF} T_J = -40°C to 150°C		11		mA
Shutdown Current	I_{SHDN}	EN = 0V, T_J = 25°C		1		μA
		EN = 0V, T_J = -40°C to 150°C		3		
Feedback Reference Voltage	V_{REF}	T_J = -40°C to 150°C	0.99	1	1.01	V
EN Rising Threshold	$V_{EN,R}$		1.1	1.2	1.3	V
EN Falling Threshold	$V_{EN,F}$		0.9	1.0	1.1	V
FB Input Current	I_{FB}	V_{FB} = 3V	-100		100	nA
Top FET R_{ON}	$R_{DS(ON)1}$			41		mΩ
Bottom FET R_{ON}	$R_{DS(ON)2}$			21		mΩ
Top FET Current Limit	I_{PK_LIM}		9	10	12.5	A
Bottom FET Current Limit	I_{VA_LIM}			7		A
Bottom FET Reverse Current Limit	$I_{NEG,RVS}$		1.7	3	4.2	A
Switching Frequency Program Range	$f_{SW,RNG}$	R_{FS} = 5.6k~44.5k	300		2200	kHz
Switching Frequency Setting Accuracy	f_{SW}	R_{FS} = 5.6k	1.98	2.2	2.42	MHz
		R_{FS} = 44.5k	270	300	330	kHz
Clock Sync Frequency Range	$f_{SYNC,RNG}$	(Note 5)	300		2200	kHz
Power Good Threshold	V_{PG}	V_{FB} falling, PG from high to low	91%	94%	97%	V_{REF}
		V_{FB} rising, PG from low to high	92.5%	95.5%	98.5%	V_{REF}
		V_{FB} rising, PG from high to low	117%	120%	123%	V_{REF}
		V_{FB} falling, PG from low to high	112%	115%	118%	V_{REF}
Power Good Delay	t_{PG_F}	High to low (Note 5)		20		μs
	t_{PG_R}	Low to high (Note 5)		120		μs
Power Good Output Low	$V_{PG,L}$	I_{PG} = 2mA			0.3	V
Power Good High Leakage Current	$I_{PG,LK}$				1	μA
Internal Soft-Start Time	t_{SS}			1		ms
Edge Height for SYNC	$V_{EN/SYNC}$	Rise/fall time < 30ns (Note 5)			2.4	V
Blanking Time of EN after Rising or Falling Edges	t_B	(Note 5)	4		28	μs
Enable Sync Signal Hold Time after Edge for Edge Recognition	t_{SYNC_EDGE}	(Note 5)	100			ns

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Frequency Span of Spread Spectrum Operation	f_{SS}			±5		%
LX Rise Time	t_{RISE}	R_{BS} = 0, I_{OUT} = 2A, 10%–80% (Note 5)		3		ns
		R_{BS} = 100Ω, I_{OUT} = 2A, 10%–80% (Note 5)		18		ns
Maximum On-Time	$t_{ON,MAX}$	f_{SW} = 300kHz		5.5		µs
Minimum On-Time	$t_{ON,MIN}$	(Note 5)		90		ns
Minimum Off-Time	$t_{OFF,MIN}$	f_{SW} = 2.2MHz (Note 5)		90		ns
VCC Output Voltage	V_{CC}		3.2	3.3	3.4	V
Output Overvoltage Threshold	V_{OVP}	V_{FB} Rising	115	120	125	%V_{REF}
Output Overvoltage Delay	$t_{OVP,DLY}$	(Note 5)		20		µs
Output Undervoltage Protection Threshold	V_{UVP}			50		%V_{REF}
Output Undervoltage Delay	t_{UVP_DLY}	(Note 5)		100		µs
Thermal Shutdown Temperature	T_{SD}		160	170	180	°C
Thermal Shutdown Hysteresis	T_{HYS}			15		°C

Note 1: Stresses beyond the “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: θ_{JA} is measured in the natural convection at T_A = 25°C on a 2oz four-layer Silergy evaluation board. Case temperature θ_{JC} is measured at pin10.

Note 3: The device is not guaranteed to function outside its operating conditions.

Note 4: Unless otherwise stated, limits are 100% production tested under pulsed load conditions such that $T_A \cong T_J$ = 25C. Limits over the operating temperature range (See recommended operating conditions) and relevant voltage range(s) are guaranteed by design, test, or statistical correlation.

Note 5: Guaranteed by design or statistical correlation and not production tested.

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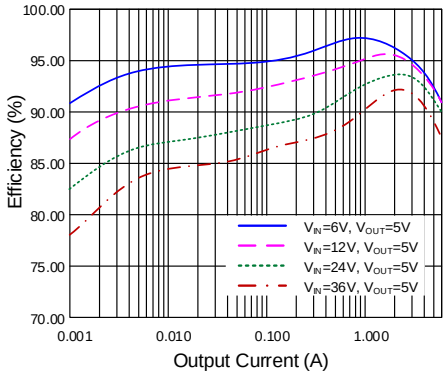
Typical Performance Characteristics

(T_A = 25°C, V_{IN} = 12V, V_{OUT} = 5V, L = 5.6μH, C_{OUT} = 4 × 22μF/25V, f_{SW} = 400kHz, unless otherwise noted. The circuit is shown in the Application Schematic section.)

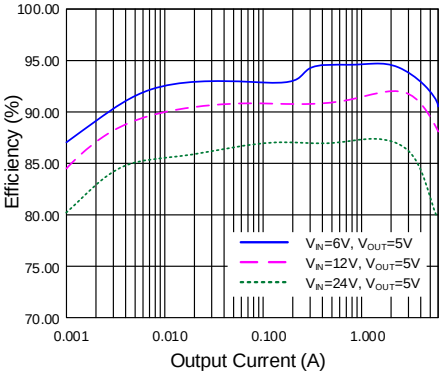
Efficiency vs Output Current

(SA24406, F_{sw}=400kHz, L=5.6uH/PCMB 104T-5R6MS)



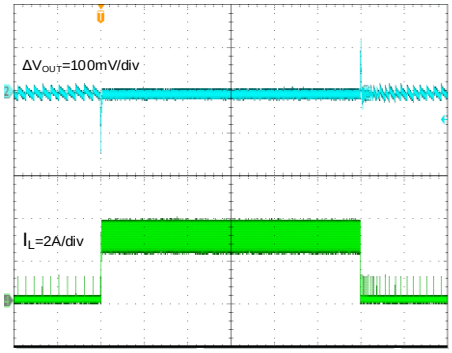
Efficiency vs Output Current

(SA24406, F_{sw}=2.1MHz, L=1.0uH/PCMB 104T-1R0MS)



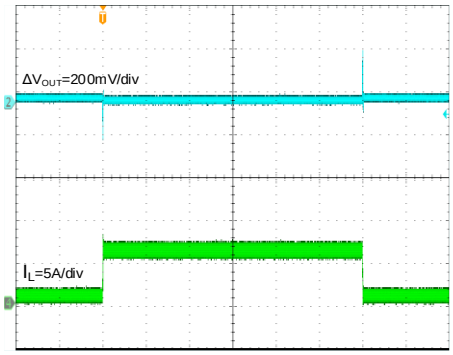
Load Transient

(SA24406, V_{IN}=12V, V_{OUT}=5V, I_{OUT}=0~3A)



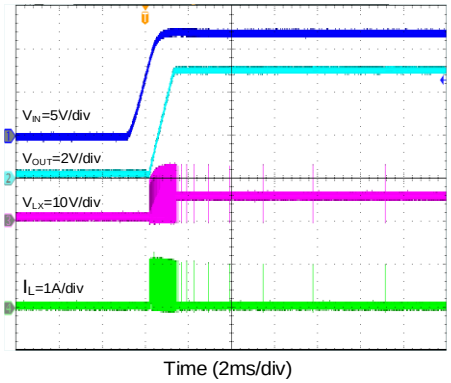
Load Transient

(SA24406, V_{IN}=12V, V_{OUT}=5V, I_{OUT}=0.6~6A)



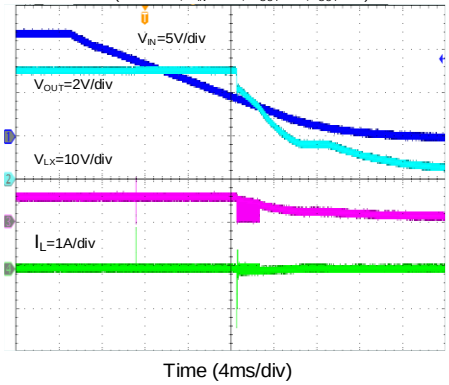
Startup From V_{IN}

(SA24406, V_{IN}=12V, V_{OUT}=5V, I_{OUT}=0A)



Shutdown From V_{IN}

(SA24406, V_{IN}=12V, V_{OUT}=5V, I_{OUT}=0A)



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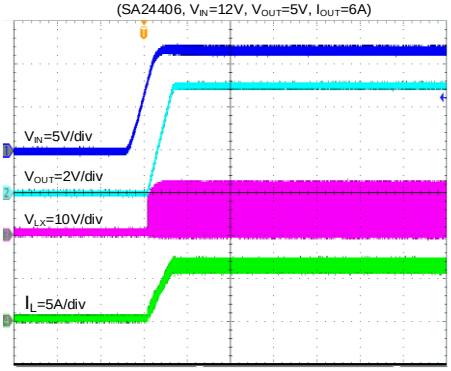
Startup From V_{IN}

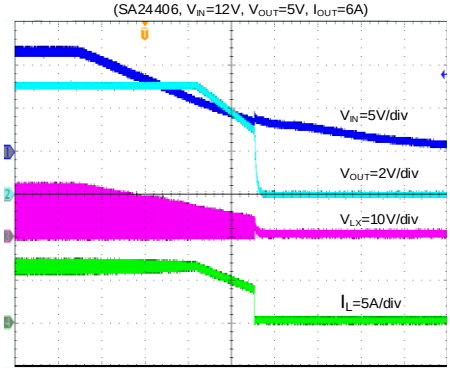
(V_{IN}=12V, V_{OUT}=5V, I_{OUT}=6A)



Time (2ms/div)

Shutdown From V_{IN}

(V_{IN}=12V, V_{OUT}=5V, I_{OUT}=6A)



Time (2ms/div)

Startup From Enable

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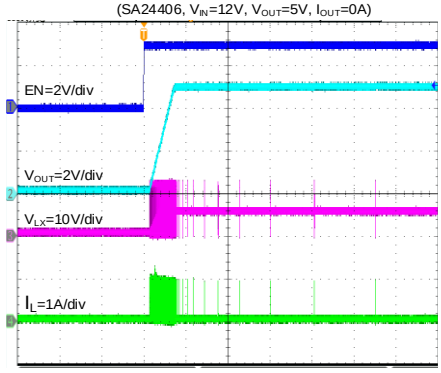
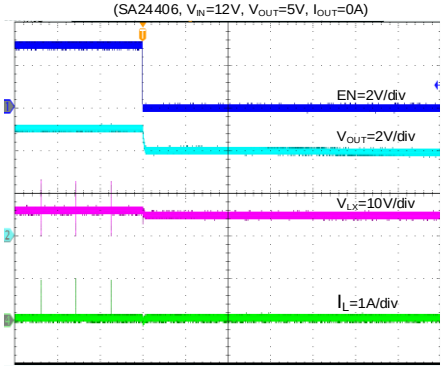


Time (2ms/div)

Shutdown From Enable

(V_{IN}=12V, V_{OUT}=5V, I_{OUT}=0A)



Time (20ms/div)

Startup From Enable

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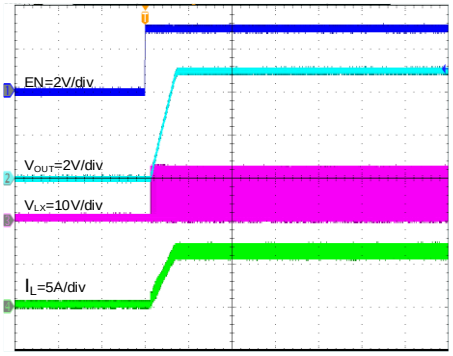
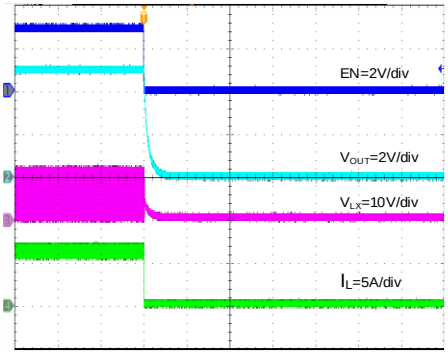


Time (2ms/div)

Shutdown From Enable

(V_{IN}=12V, V_{OUT}=5V, I_{OUT}=6A)



Time (800µs/div)

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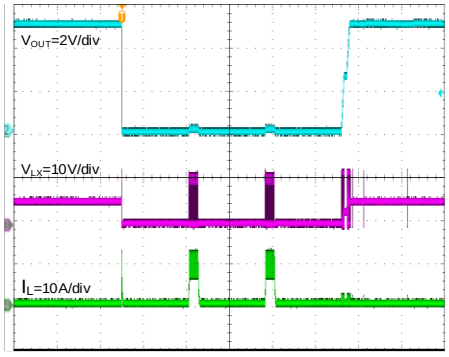
Short Circuit Protection

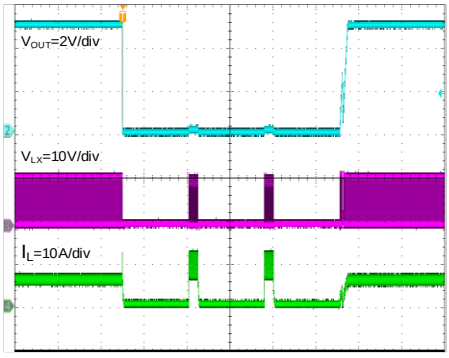
(SA24406, V_{IN}=12V, V_{OUT}=5V, I_{OUT}=0A)



Time (10ms/div)

Short Circuit Protection

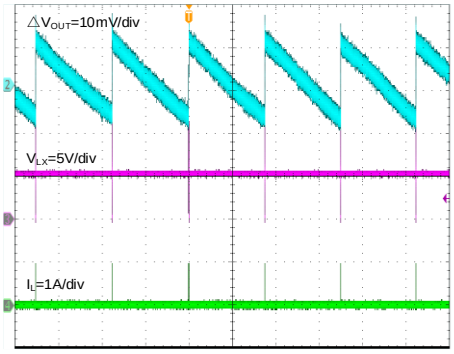
(SA24406, V_{IN}=12V, V_{OUT}=5V, I_{OUT}=6A)



Time (10ms/div)

Output Ripple

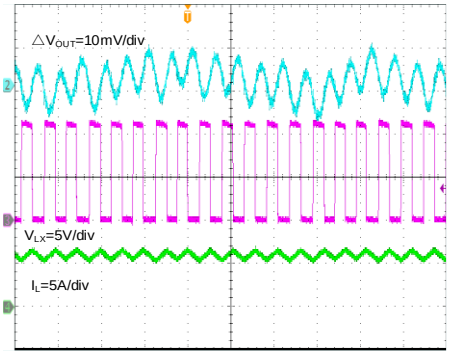
(SA24406, V_{IN}=12V, V_{OUT}=5V, I_{OUT}=0A)



Time (10ms/div)

Output Ripple

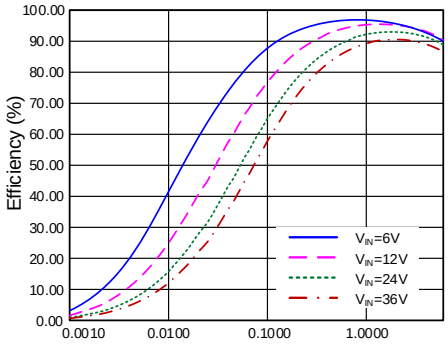
(SA24406, V_{IN}=12V, V_{OUT}=5V, I_{OUT}=6A)



Time (4μs/div)

Efficiency vs Output Current

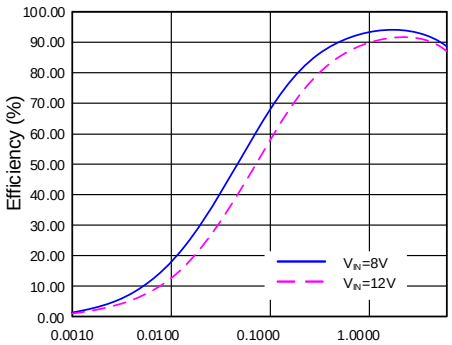
(SA24406E, F_{SW}=400kHz, L=5.6uH/PCMB 104T-5R6MS)



Output Current (A)

Efficiency vs Output Current

(SA24406E, F_{SW}=2.1MHz, L=1.0uH/PCMB 104T-1R0MS)



Output Current (A)

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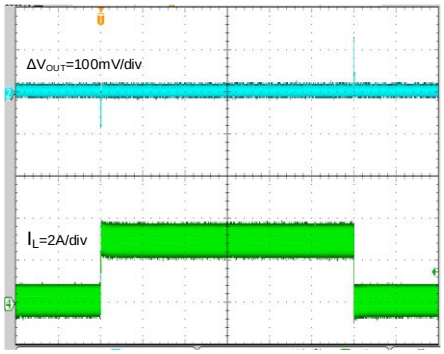
Load Transient

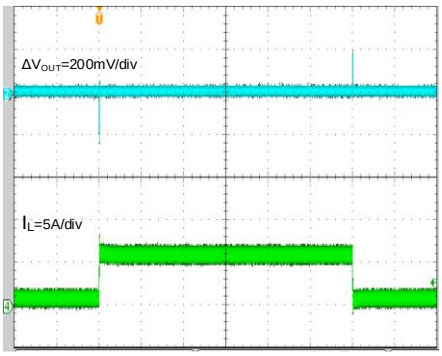
(SA24406E, V_{IN}=12V, V_{OUT}=5V, I_{OUT}=0~3A)



Time (2ms/div)

Load Transient

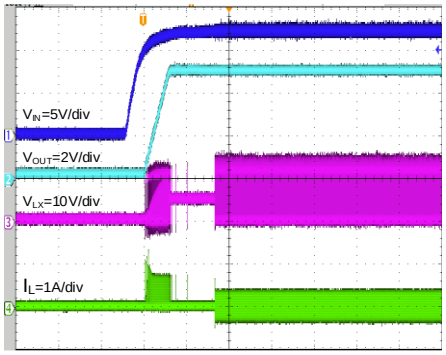
(SA24406E, V_{IN}=12V, V_{OUT}=5V, I_{OUT}=0.6~6A)



Time (2ms/div)

Startup From V_{IN}

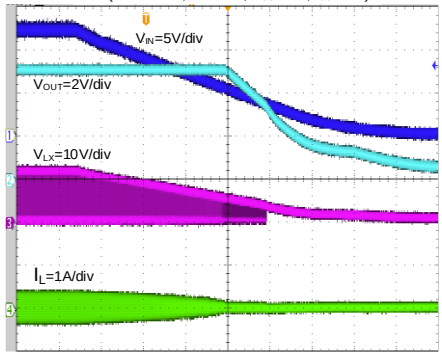
(SA24406E, V_{IN}=12V, V_{OUT}=5V, I_{OUT}=0A)



Time (2ms/div)

Shutdown From V_{IN}

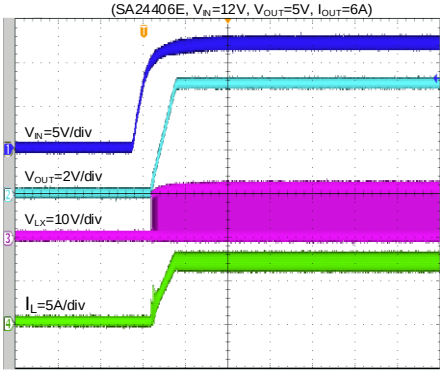
(SA24406E, V_{IN}=12V, V_{OUT}=5V, I_{OUT}=0A)



Time (4ms/div)

Startup From V_{IN}

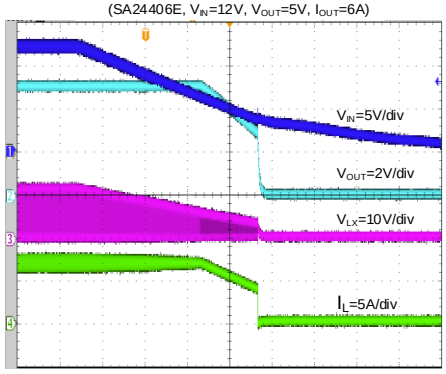
(SA24406E, V_{IN}=12V, V_{OUT}=5V, I_{OUT}=6A)



Time (2ms/div)

Shutdown From V_{IN}

(SA24406E, V_{IN}=12V, V_{OUT}=5V, I_{OUT}=6A)



Time (2ms/div)

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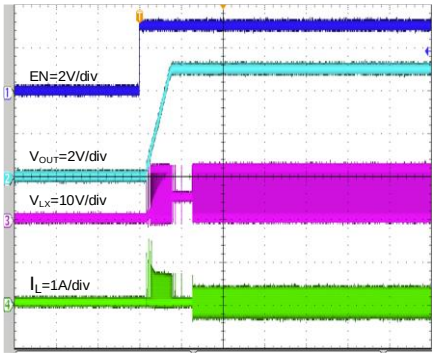
Startup From Enable

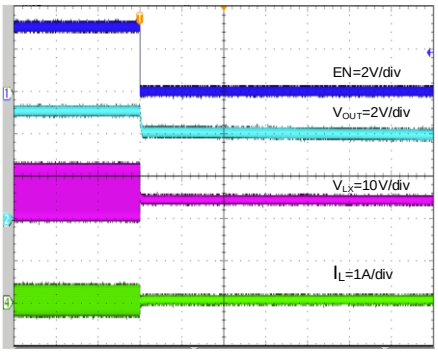
(SA24406E, V_{IN}=12V, V_{OUT}=5V, I_{OUT}=0A)



Time (2ms/div)

Shutdown From Enable

(SA24406E, V_{IN}=12V, V_{OUT}=5V, I_{OUT}=0A)



Time (20ms/div)

Startup From Enable

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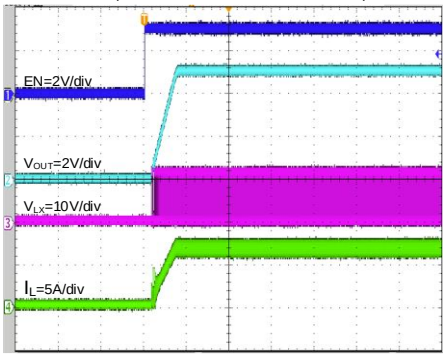
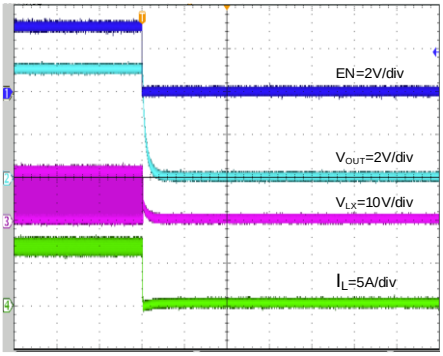


Time (2ms/div)

Shutdown From Enable

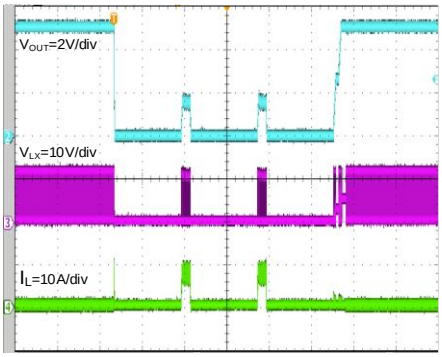
(SA24406E, V_{IN}=12V,V_{OUT}=5V,I_{OUT}=6A)



Time (800µs/div)

Short Circuit Protection

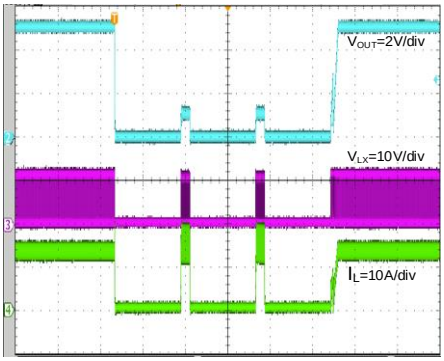
(SA24406E, V_{IN}=12V, V_{OUT}=5V, I_{OUT}=0A)



Time (10ms/div)

Short Circuit Protection

(SA24406E, V_{IN}=12V, V_{OUT}=5V, I_{OUT}=6A)



Time (10ms/div)

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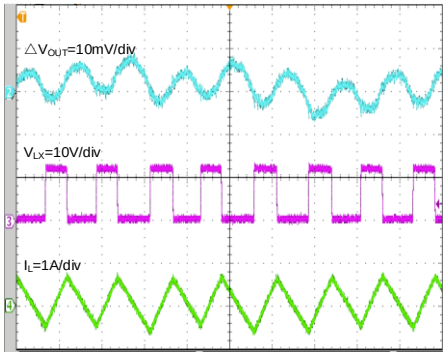
Output Ripple

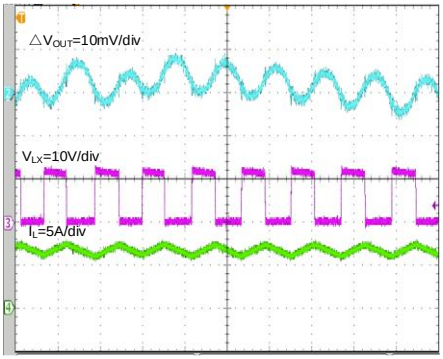
(SA24406E, V_{IN}=12V,V_{OUT}=5V,I_{OUT}=0A)



Time (10ms/div)

Output Ripple

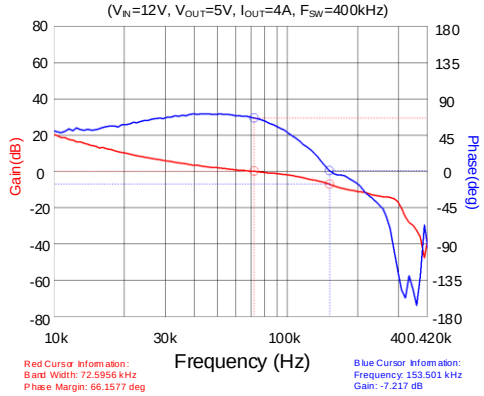
(SA24406E, V_{IN}=12V,V_{OUT}=5V,I_{OUT}=6A)



Time (4μs/div)

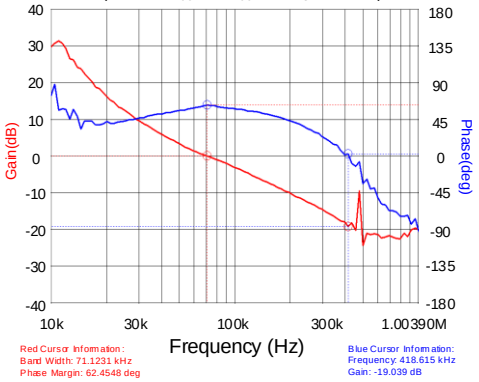
Bode Plot

(V_{IN}=12V, V_{OUT}=5V, I_{OUT}=4A, F_{SW}=400kHz)



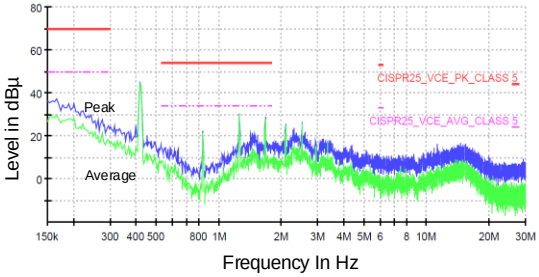
Bode Plot

(V_{IN}=12V, V_{OUT}=5V, I_{OUT}=4A, F_{SW}=2.2MHz)



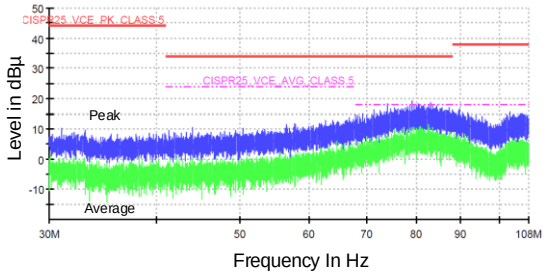
CISPR 25 Class 5 Conducted Emission

(f_{SW}=150kHz-30MHz)



CISPR 25 Class 5 Conducted Emission

(f_{SW}=30MHz-108MHz)



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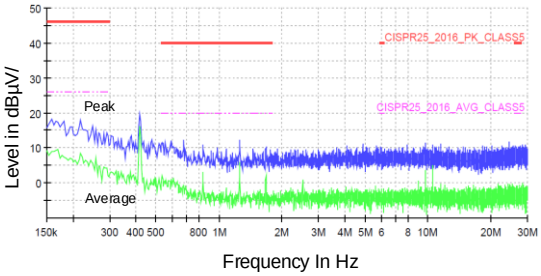
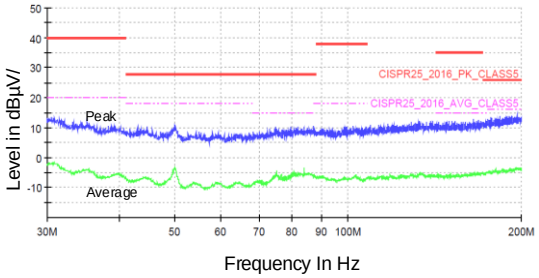
CISPR 25 Class 5 Radiated Emission

(f_{SW}=150kHz-30MHz)



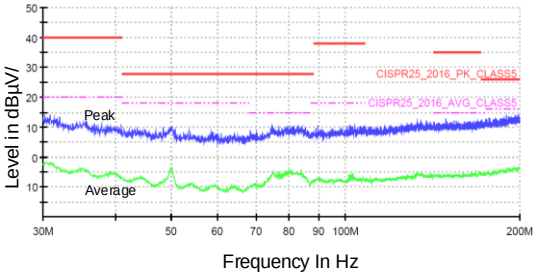
CISPR 25 Class 5 Radiated Emission

(Vertical f_{SW}=30MHz-200MHz)



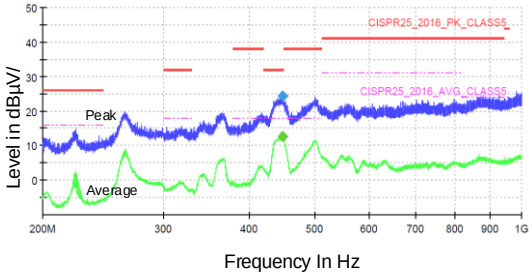
CISPR 25 Class 5 Radiated Emission

(Horizontal f_{SW}=30MHz-200MHz)



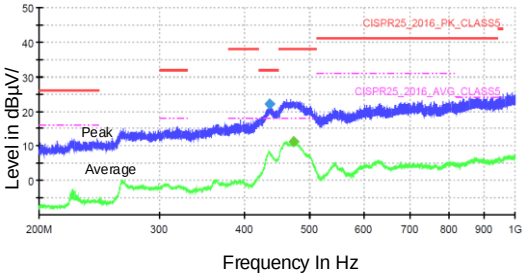
CISPR 25 Class 5 Radiated Emission

(Vertical f_{SW}=200MHz-1GHz)



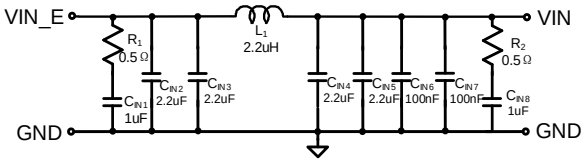
CISPR 25 Class 5 Radiated Emission

(Horizontal f_{SW}=200MHz-1GHz)



EMI Filter

(V_{IN}=12V, V_{OUT}=5V, F_{SW}=400kHz)



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Functional Description

The SA24406x is a high efficiency synchronous step-down DC-DC regulator with internal power and synchronous rectifier MOSFETs. It operates using fixed frequency and peak current control over a wide input voltage range of 4V to 36V, and can deliver up to 6A of continuous output current.

The SA24406x is specially designed with a symmetric QFN package and adjustable LX rise time to achieve good EMI performance. The switching frequency can be adjusted from 300kHz to 2.2MHz, or synchronized to an external clock. The frequency can be selected to meet application EMI limits and to avoid noise in important frequency bands.

The SA24406x offers excellent efficiency over a wide range of applications by providing internal 41mΩ power and 21mΩ synchronous rectifier MOSFETs, frequency reduction at light load conditions, and an external bias input. The 1μA shutdown supply current allows the device to be used in battery powered applications. The SA24406x ensures safe operation in all operating conditions, providing cycle-by-cycle current limit, input undervoltage lockout, internal soft-start, output undervoltage and overvoltage protection, and thermal shutdown.

General Features

Fixed Frequency PWM Control and Slope Compensation

The SA24406x uses fixed frequency and peak current mode control. The output voltage is fed back to the error amplifier through an external resistor divider connected to the FB pin, and compared with the internal reference voltage V_{REF}. The output of the error amplifier (V_{COMP}) controls the peak current level and the output voltage.

On the rising edge of the internally generated fixed frequency clock, the internal high side N-channel power MOSFET will turn on. The MOSFET current is converted into a ramp voltage signal using a 1/GPK coefficient. When the ramp voltage plus the compensation ramp reaches V_{COMP}, the high side power MOSFET will turn off and the synchronous rectifier MOSFET turns on. Peak current mode control also provides inherent cycle-by-cycle peak current limit.

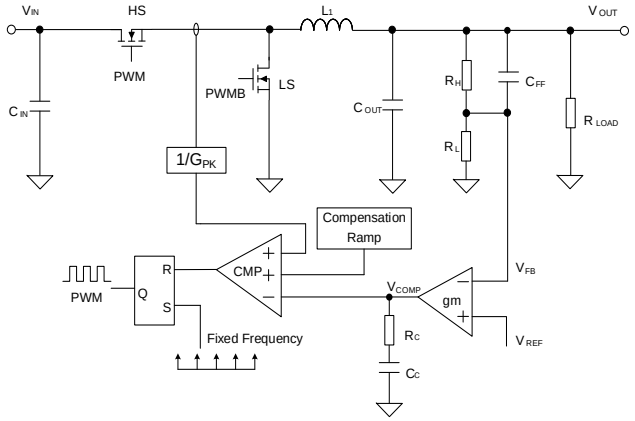

Figure 4. Fixed Frequency PWM Control and Slope Compensation

Light Load Operation

The SA24406 provides two light load operation modes: pulse frequency modulation (PFM) (default) and forced continuous current mode (FCCM). In PFM mode, the low-side synchronous rectifier is turned off when the current through the rectifier ramps to zero, preventing recirculation current that can reduce efficiency under light load conditions. In addition, the output of the error amplifier (V_{COMP}) naturally decreases and then reduces the peak current during light load conditions. When V_{COMP} decreases further with the decreasing load and reaches the preset low threshold, the device stops switching to reduce switching power loss and quiescent current, further improving light load efficiency. Switching resumes when V_{COMP} rises above the low threshold.

When EN/SYNC is used for synchronization and the internal oscillator is synchronized to an external clock, the SA24406 operates in FCCM mode over the entire output current range, including at low loads. The low side synchronous rectifier stays on, even when the inductor current crosses zero. Current flow continues until the high side MOSFET switches on. SA24406E always runs FCCM mode over the entire output current range, including low load, when the start-up is complete.

EN/SYNC and Adjustable Input Undervoltage Lockout

The EN/SYNC input supports high voltage and logic compatible thresholds. The input comparator design features a relatively accurate rising threshold. When EN voltage rises to approximately 0.8V, VCC provides the EN comparator with source supply. When EN is driven above 1.2V, normal device operation is enabled, and the converter starts switching. When EN voltage falls below $V_{EN,F}$, the device stops switching. When EN voltage is driven lower than 0.4V, the device is shut down, reducing the input current to less than 10μA (typical).

If the default input UVLO threshold is too low for some applications, adding a resistor divider between VIN and

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GND with the midpoint connected to EN can be used adjust the input UVLO to a higher threshold. This pin doesn't have an internal pulldown resistor and should not be left floating.

The EN/SYNC pin can also be used as a synchronization input for the switching frequency. When an external clock ranging from 300kHz to 2.2MHz is connected to EN/SYNC, the internal oscillator will be synchronized to the clock, spread spectrum will be turned off, and the IC will operate in FCCM mode at light load conditions. See Figure 5 for details.

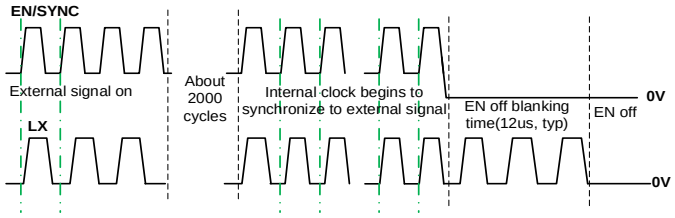

Figure 5. EN/SYNC Timing

VCC Linear Regulator and BIAS Input

The 3.3V internal linear regulator input (VCC) provides the power supply for the internal gate drivers, PWM logic, analog circuitry, and other blocks. Connect a low ESR ceramic capacitor with a capacitance of at least 1μF from VCC to GND.

The BIAS pin is one of the inputs to the internal LDO. Connecting this pin to the output can reduce power loss caused by internal LDO and improve efficiency. If the BIAS voltage is less than 3.1V, the internal LDO will be powered by V_{IN} directly.

When powering from V_{OUT}, add a 10Ω to 51Ω resistor between V_{OUT} and BIAS, and place a ceramic capacitor with a value of 1μF or higher between BIAS and GND to reduce noise.

Power Good Indication

The power good indicator (PG) is an open-drain output controlled by a window comparator connected to the feedback signal. This pin is pulled to ground if output voltage is lower than 94% of regulation voltage or higher than 120% of regulation voltage. This pin is set to high impedance state if output voltage is between 95.5% and 115% of regulation voltage

PG should be connected to V_{IN} or another voltage source through a resistor (e.g., 10kΩ–100kΩ).

External Bootstrap Capacitor

The SA24406x integrates a floating power supply for the gate driver that operates the internal high side N-channel power MOSFET. Connect a 0.1μF low ESR ceramic capacitor between BS and LX for proper operation.

Adjustable LX Rising Time

The LX node rising time (10%-80%V_{LX}) can be adjusted from 3ns to 21ns using a resistor between RBS and CBS. See Figure 6.

The LX rising time can be selected for improved efficiency when using fast rise time or reduce EMI by using slower rise time.

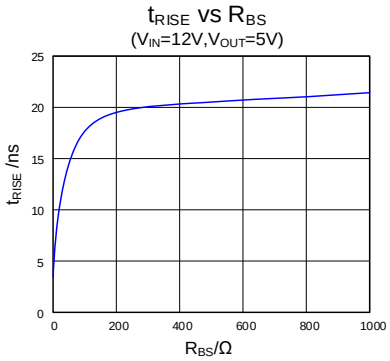

Figure 6. LX Rising Time

Adjustable Switching Frequency

The switching frequency can be adjusted from 300kHz to 2.2MHz by connecting a resistor between FS and GND. The switching frequency can be calculated as follows:

$$f_{SW}(kHz) = \frac{1.346 \times 10^4}{RFS(k\Omega) + 0.444}$$

Note that the IC's stability will be affected if the on-time is close to the minimum on time $t_{ON,MIN}$. Table 1 shows the switching frequency and RFS values for typical applications.

Table 1. Adjustable Switching Frequency

f_{SW}(kHz)	R_{FS}(kΩ)	V_{IN}(V), V_{OUT} = 5V	
		12	36
300	44.2	✓	✓
400	33	✓	✓
1000	13.3	✓	✓
2200	5.67	✓	×
450	OPEN	✓	✓

Minimum Duty Cycle and Maximum Duty Cycle

The switching frequency is not only affected by component tolerance, but also minimum on-time and off-time limits. Therefore, the minimum duty cycle is approximately 3.6% at 400kHz switching frequency, considering approximately 90ns minimum on-time. Due to the device's on-time stretch function, the maximum duty cycle is up to 95% over the -40°C-125°C temperature range.

For SA24406E (FCCM version), special attention should be paid whether minimum on time ($t_{ON,MIN}$) will be continuously trigged in the system application. This

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should be avoided for the sake of output voltage accuracy and ripple. Once the minimum on time is continuously triggered, the VOUT voltage will increase with the switching until the OVP (typ. 120%*V_{REF}) is triggered and the IC stops switching to prevent output voltage runaway. Then the output voltage drops and after the output voltage is less than the set point, the IC enters FCCM again. This switching behavior will be repeated unless the condition disappears.

Frequency Spread Spectrum

A ±5% spread of the internal oscillator frequency is used to create side bands of the switching frequency and its harmonics. This spreads out the emission power spectrum and reduces the peak EMI switching noise.

Fault Protections

Peak Current Limit Protection

Because the converter operates using peak current mode control, the SA24406x provides inherent cycle-by-cycle peak current limiting (top MOSFET current limit). During time t_{ON}, if the high side power MOSFET current exceeds the current limit threshold, it is turned off and the low side synchronous rectifier is turned on. A blanking on time period is used at the beginning of the on-time, during which current sampling is disabled to avoid false triggers caused by switching noise. Peak current limit protection priority is lower than minimum on-time.

Valley Current Limit Protection

The SA24406x provides valley current limiting (bottom MOSFET current limit). If the peak current limit is triggered, the high side MOSFET is turned off. The high side switch cannot be turned on again until the low side synchronous rectifier current is lower than the bottom MOSFET current limit, and the inductor current returns to safe levels.

Reverse Current Limit Protection

The SA24406x provides cycle-by-cycle reverse current limiting. When the current is lower than the reverse current limit (-3A, typical), the low side synchronous rectifier is turned off and the high side power switch is turned on. A blanking off-time period is used at the beginning of the on-time in the low side synchronous rectifier, during which current sampling is disabled to avoid false triggers caused by switching noise.

Short-Circuit Protection

The SA24406x integrates hiccup mode short-circuit protection. If V_{FB} < 50%*V_{REF} and the peak current limit is triggered, short-circuit protection mode will be initiated. The SA24406x will shut down for approximately 14ms, and then restart with a complete soft-start cycle that is approximately 2ms. If the fault condition is resolved, the device will resume normal operation. See Figure 7.

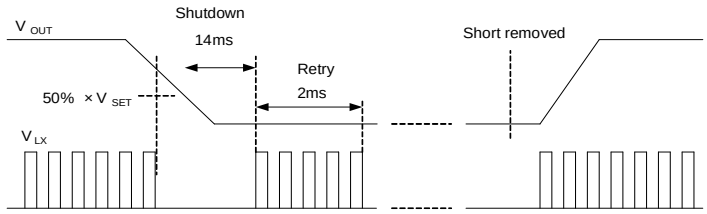

Figure 7. Short-Circuit Protection

Output Overvoltage Protection (OVP)

The SA24406x provides overvoltage protection. When the FB voltage is higher than V_{REF}, V_{COMP} will decrease. If the SA24406x is operating in PFM mode, the high side MOSFET will not be able to turn on when V_{COMP} is lower than the preset low threshold. If the frequency is synchronized to an external clock, switching will continue until the FB exceeds 120% of V_{REF} and overvoltage protection is triggered. When OVP is triggered, light load operation mode will change to PFM mode, and the high-side switch will not be turned on until V_{COMP} is higher than the low threshold.

Overtemperature Protection (OTP)

The overtemperature protection (OTP) circuitry prevents overheating due to excessive power dissipation. This will shut down the device when the junction temperature exceeds T_{SD}. Once the junction temperature cools down by approximately 15°C, the device will resume normal operation after a complete soft-start cycle. For continuous operation, provide adequate cooling so that the junction temperature does not exceed the T_{SD}.

Design Procedure

Feedback Resistor Selection

Choose R_H and R_L to program the proper output voltage. Choose large resistance values for both R_H and R_L to minimize power consumption under light loads. A value of between 10kΩ and 1MΩ is recommended for R_H. If V_{OUT} = 12V and R_H is chosen to be 100kΩ, R_L can be calculated as 24.9kΩ using following equation:

$$R_L = \frac{1V}{V_{OUT} - 1V} \times R_H$$

Input Capacitor Selection

Input filter capacitors are needed to reduce the ripple voltage on the input, to filter the switched current drawn from the input supply and to reduce EMI. When selecting an input capacitor, select a voltage rating at least 20% greater than the maximum voltage of the input supply and a temperature rating above the system requirements. X7R series ceramic capacitors are most often selected

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due to their small size, low cost, surge current capability and high RMS current ratings over a wide temperature and voltage range. Systems that are powered by a wall adapters or other long and therefore inductive wires may be susceptible to significant inductive ringing at the input to the device. In these cases, consider adding some bulk capacitance like electrolytic, tantalum, or polymer type capacitors. Using a combination of bulk capacitors (to reduce overshoot or ringing) in parallel with ceramic capacitors (to meet the RMS current requirements) is helpful in these cases.

Consider the RMS current rating of the input capacitor, paralleling additional capacitors if required to meet the calculated RMS ripple current.

$$I_{CIN_RMS} = I_{OUT} \times \sqrt{D \times (1-D)}$$

The worst-case condition occurs at D = 0.5, then

$$I_{CIN_RMS,MAX} = \frac{I_{OUT}}{2}$$

For simplicity, choose an input capacitor with an RMS current rating greater than half of the maximum load current.

The input capacitor value determines the input voltage ripple of the converter. If there is an input voltage ripple requirement in the system, choose an appropriate input capacitor that meets the specification. Given the very low ESR and ESL of ceramic capacitors, the input voltage ripple can be estimated as follows:

$$V_{CIN_RIPPLE,CAP} = \frac{I_{OUT}}{f_{SW} \times C_{IN}} \times D \times (1-D)$$

The worst-case condition occurs at D = 0.5, then

$$V_{CIN_RIPPLE,CAP,MAX} = \frac{I_{OUT}}{4 \times f_{SW} \times C_{IN}}$$

The capacitance value is less important than the RMS current rating. In most applications, using three 10μF X7R capacitors connected in parallel is sufficient. Place the ceramic input capacitors as close to the IN and GND pins as possible.

Inductor Selection

The inductor is necessary to supply constant current to the output load while being driven by the switched input voltage. Selecting a low inductor value will help reduce size and cost and enhance transient response, but will increase peak inductor ripple current, reducing efficiency and increasing output voltage ripple. The low DC resistance (DCR) of these low value inductors may help reduce DC losses and increase efficiency. Higher inductor values tend to have higher DCR and slow transient response.

A reasonable compromise between size, efficiency, and transient response can be obtained by selecting a ripple current (ΔIL) approximately 20%–50% of the desired full output load current. Start calculating the approximate inductor value by selecting the input and output voltages, the operating frequency (f_{SW}), the maximum output current ($I_{OUT,MAX}$) and estimating a ΔI_L as some percentage of that current.

$$L_1 = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times f_{SW} \times \Delta I_L}$$

Use this inductance value to determine the actual inductor ripple current (ΔI_L) and required peak current inductor current $I_{L,PEAK}$ according to the following equations:

$$\Delta I_L = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times f_{SW} \times L_1}$$

$$I_{L,PEAK} = I_{OUT,MAX} + \frac{\Delta I_L}{2}$$

Select an inductor with a saturation current in excess of $I_{L,PEAK}$.

For maximum efficiency, select an inductor with a low DCR that meets the inductance, size, and cost targets. Low loss ferrite materials should be considered.

Output Capacitor C_{OUT} Selection

Select the output capacitor C_{OUT} to handle the output ripple requirements. Both steady-state ripple and transient requirements must be taken into consideration when selecting this capacitor. Ceramic and POS types are most often selected due to their small size and low cost.

Output voltage ripple at the switching frequency is caused by the inductor current ripple (ΔI_L) on the output capacitors ESR (ESR ripple) as well as the stored charge (capacitive ripple). When estimating the total ripple, both should be considered.

$$V_{RIPPLE,ESR} = \Delta I_L \times ESR$$

$$V_{RIPPLE,CAP} = \frac{\Delta I_L}{8 \times C_{OUT} \times f_{SW}}$$

Using four X7R or better grade ceramic capacitors in parallel, with at least 22μF capacitance is recommended for a typical application.

Load Transient Considerations

The device integrates compensation components to achieve good stability and fast transient responses. Adding a small ceramic capacitor C_{FF} in parallel with R_H may further speed up the load transient responses and is

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thus highly recommended for applications with large load transient step requirements.

Thermal Design Considerations

Maximum power dissipation depends on the thermal resistance of the IC package, the PCB layout, the surrounding airflow, and the difference between the junction and ambient temperatures. The maximum power dissipation may be calculated as follows:

$$P_{D,MAX} = (T_{J,MAX} - T_A) / \theta_{JA}$$

Where $T_{J,MAX}$ is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction-to-ambient thermal resistance.

To comply with the recommended operating conditions, the maximum junction temperature is 150°C. The junction-to-ambient thermal resistance θ_{JA} is layout dependent. For the QFN3.5×4-14 package, the thermal resistance θ_{JA} is 31.5°C/W when measured on a standard Silergy four-layer thermal test board. These standard thermal test layouts have a very large area with long 2-oz. copper traces connected to each pin and very large, unbroken 1oz. internal power and ground planes.

Meeting the performance of the standard thermal test board in a typical board design requires the following:

- Wide copper traces that are well connected to the IC's backside pads leading to exposed copper areas on the component side of the board
- Good thermal vias from the exposed pad connecting to a wide middle-layer ground plane and to an exposed copper area on the board's solder side.

The maximum power dissipation at T_A = 25°C may be calculated using the following formula:

$$P_{D,MAX} = (150°C - 25°C) / (31.5° / W) = 3.97W$$

Maximum power dissipation depends on operating ambient temperature for fixed $T_{J,MAX}$ and thermal resistance θ_{JA}. Use the derating curve in Figure 8 to calculate the effect of rising ambient temperature on the maximum power dissipation.

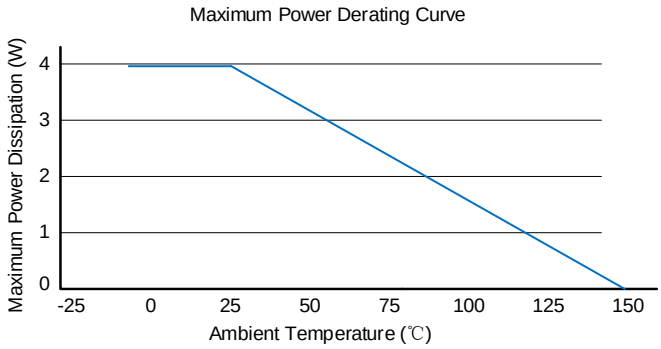

Figure 8. Derating Curve

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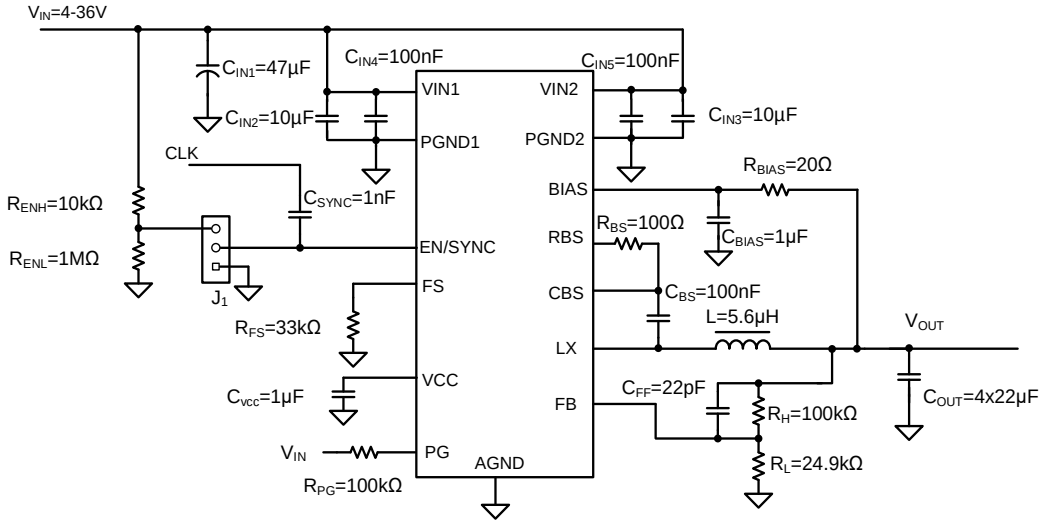
Application Schematic (V_{OUT} = 5V)



BOM List

Reference Designator	Description	Part Number	Manufacturer
C_{IN1}	47μF/100V Electrolytic Cap		
C_{IN2}, C_{IN3}	10μF/50V/X7T/0603	GCM31CD71H106KE36K	mμRata
C_{IN4}, C_{IN5}	100nF/50V/X7R/0603	GCM188R71H104KA57D	mμRata
C_{OUT}	22μF/25V/X7S/1206	GRM31CC71E226ME15L	mμRata
C_{BS}	100nF/50V/X7R/0603	GCM188R71H104KA57D	mμRata
C_{FF}	22pF/50V/C0G/0603	GRM1885C1H220JA01D	mμRata
C_{VCC}	1μF/25V/X7R/0603	GCM188R71E105KA64D	mμRata
C_{BIAS}	1μF/25V/X7R/0603	GCM188R71E105KA64D	mμRata
C_{SYNC}	1nF/50V/X7R/0603	GRM188R71H102KA01D	mμRata
L	5.6μH	PCMB104T-5R6MS	Cyntec
R_H	100kΩ, 1%, 0603		
R_L	24.9kΩ, 1%, 0603		
SR_{BS}	100Ω, 1%, 0603		
R_{BIAS}	20Ω, 1%, 0603		
R_{PG}	100kΩ, 1%, 0603		
R_{FS}	33kΩ, 1%, 0603		
R_{ENH}	10kΩ, 1%, 0603		
R_{ENL}	1MΩ, 1%, 0603		

Recommended Component Values for Typical Applications

V_{OUT} (V)	f_{SW} (kHz)	R_H (kΩ)	R_L (kΩ)	L	C_{OUT}
3.3	400	100	43	3.3μH/PCMB104T-3R3MS	22μF×4/GRM31CC71E226ME15L
5	400	100	24.9	5.6μH/PCMB104T-5R6MS	22μF×4/ GRM31CC71E226ME15L
5	2200	51	12.7	1μH/PCMB104T-1R0MS	22μF×4/ GRM31CC71E226ME15L
12	400	100	9.1	10μH/PCMB104T-100MS	22μF×4/ GRM31CC71E226ME15L

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Layout Design

Follow these PCB layout guidelines for optimal performance:

- Place C_{IN}, C_{VCC}, L, R1, and R2 as close as possible to the converter.
- To achieve the best thermal and noise performance, maximize the PCB copper area connected to the GND pin. A ground plane is highly recommended if board space allows.
- Place C_{IN} close to pins IN and GND. Minimize the loop area formed by C_{IN} and GND.
- Minimize the PCB copper area associated with the LX pin.
- To reduce noise, ensure that R_1, R_2, and the trace connecting to the FB pin are not adjacent to the LX net on the PCB layout.
- If the system chip driving the EN pin has a high impedance state during shutdown and the IN pin is connected directly to a power source such as a Li-Ion battery, add a 1MΩ pull-down resistor between the EN and GND pins to prevent the noise from falsely turning on the regulator during shutdown.

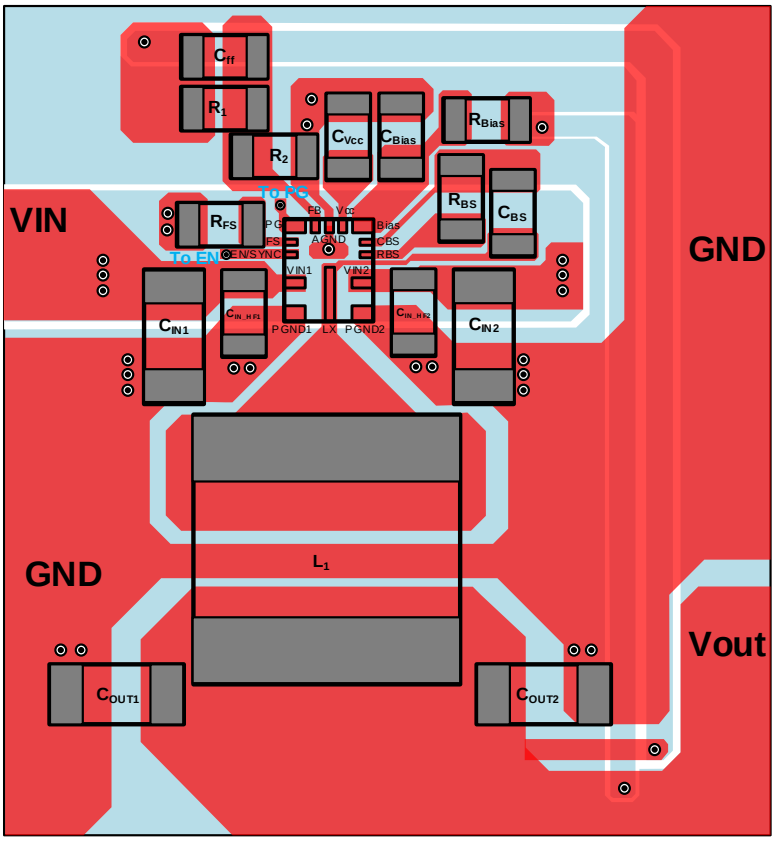

Figure 9. Suggested PCB Layout

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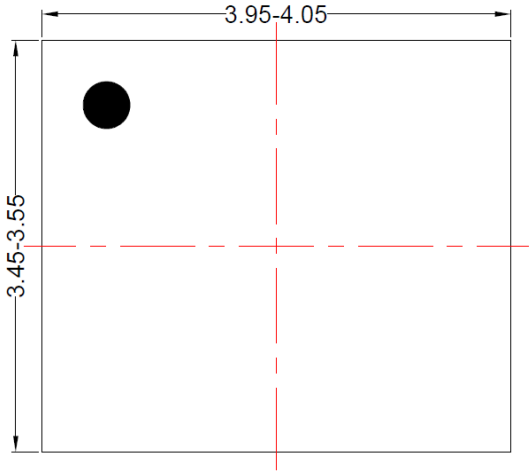
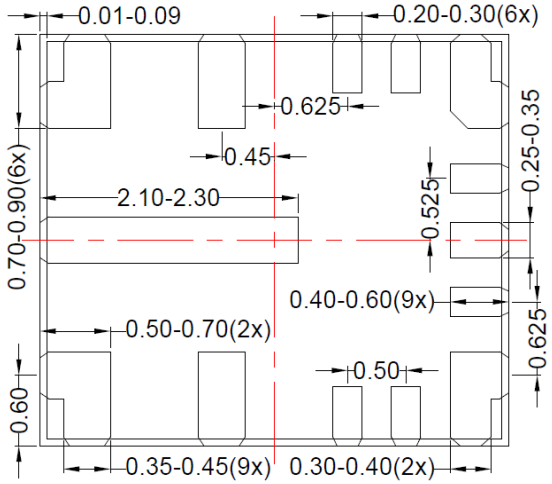
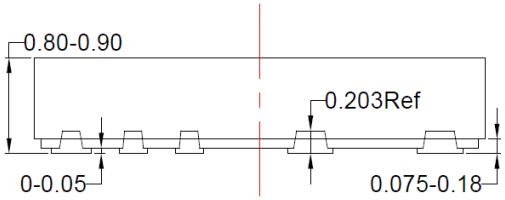
QFN3.5×4-14 Package Outline Drawing



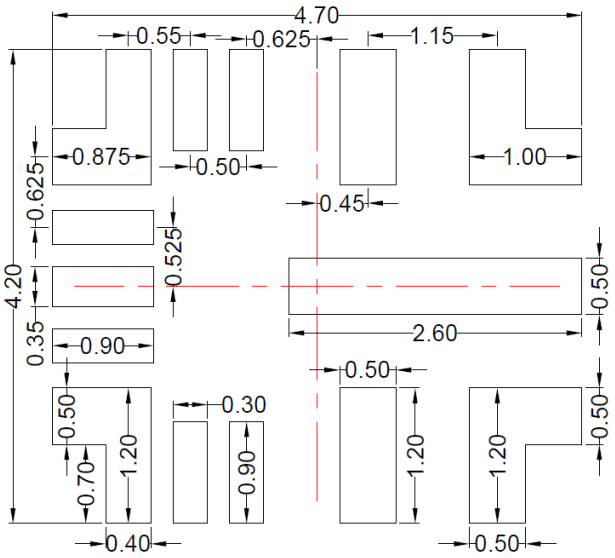
Top View



Bottom View



Front View



Recommended PCB layout
(Reference only)

Notes:

1. *All dimensions are in millimeters and exclude mold flash and metal burr.*
2. *Center line refers to the chip body center.*

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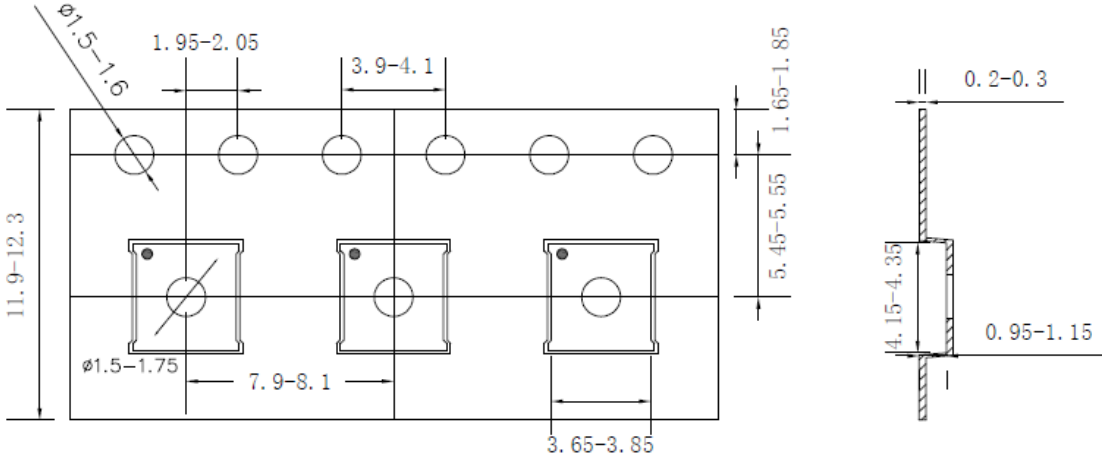
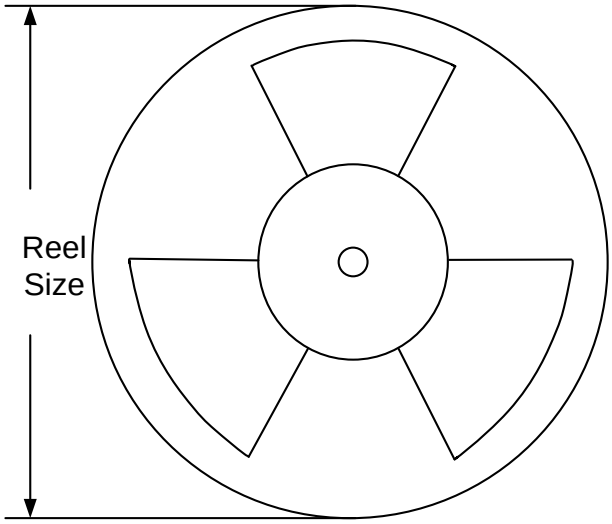
Tape and Reel Information

Tape Dimensions and Pin 1 Orientation



Direction of feed ⟶

Reel Dimensions



Package Types	Tape Width (mm)	Pocket Pitch (mm)	Reel Size (Inch)	Trailer * Length (mm)	Leader * Length (mm)	Qty per Reel (pcs)
QFN3.5×4	12	8	13"	400	400	5000

All Dimension are nominal

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Revision History

The revision history provided is for informational purposes only and is believed to be accurate, however, not warrantied. Please make sure that you have the latest revision.

Date	Revision	Change	Pages changed
Jul.02, 2024	Revision 1.0	SA244406 Initial release.	-
Apr.09, 2025	Revision 1.0	SA24406E Initial release.	-
May.28, 2025	Revision 1.0A	Update POD.	Page 20

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