SA32774

24-Channel LED Driver for Rear Light Application

General Description

The SA32774 is a 24-channel LED driver designed for rear light applications, supporting both PWM dimming and analog dimming. It integrates a 10-bit PWM generator and allows for dual-range configurable current.

It supports the UART protocol with a CAN physical layer to control the LED for fast animation, which improves the system's EMI. There are various modes for users to realize different functions. Each mode has its own current and duty cycle specifications.

The SA32774 integrates a current derating function which helps to reduce the power loss.

The SA32774 includes diagnostic features to indicate fault conditions such as LED open, LED short, and over-temperature protection (OTP).

The device is available in a 7x7 mm QFN package.

Features

- Supports LED Supply Voltage Range from 4.9V up to 16V
- 2Mbps CAN Physical Bus Interface with UART Protocol
- 10-bit Resolution PWM Generator for 24 Channels
- 100mA Maximum Channel Current
- Adjustable LED Driver Current 100μA/step
- Direct PWM Input
- 10-bit ADC for LED Open, Short and System Diagnosis
- Single Lamp Mode Behavior Option
- Automatic Supply and Temperature Dependent LED Current Derating
- LED Channel Individual bin Class Brightness Correction
- External LED bin Class Resistor Evaluation
- Available in AEC-Q100 Grade 1
- MSL3

Applications

- Rear Light for Automotive

Typical Application

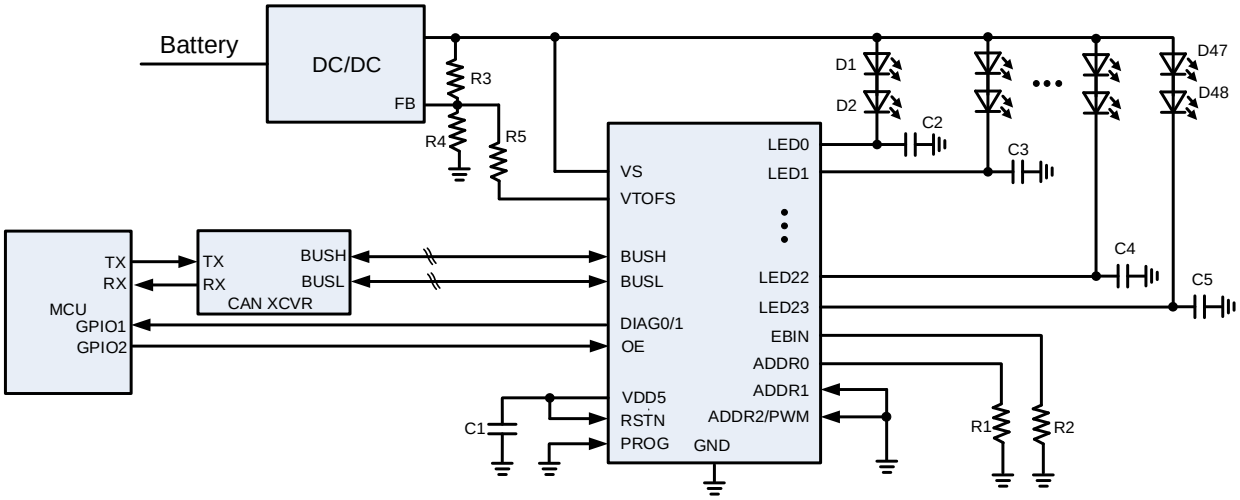

Figure.1 Schematic

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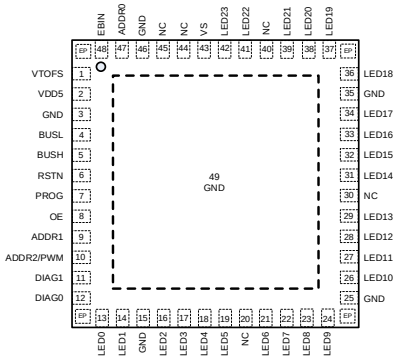
Ordering Information

Ordering Part Number	Package type	Top Mark
SA32774QJQ	QFN7×7-48 RoHS-Compliant and Halogen-Free	**GNR***xyz*

x = year code, y = week code, z = lot number code

Pinout (top view)



(QFN7*7-48)

Pin Description (A=Analog, D=Digital, S= Supply, I=Input, O=Output, B=Bidirectional, HV=high Voltage)

Pin Name	Pin number	Pin Description
VTOFS	1	VT offset output pin. Used to compensate LED drop voltage during high temperature.
VDD5	2	Internal 5V supply pin. A decoupling capacitor has to be attached to this pin.
GND	3	Ground.
BUSL	4	CAN bus L signal pin.
BUSH	5	CAN bus H signal pin.
RSTN	6	Open-drain active low reset pin.
PROG	7	Active high device programming mode pin.
OE	8	LED sink current blanking pin. Used to enable or disable the PWM generator of sink current in BUS mode and BUS timeout mode.
ADDR1	9	Device address 1 in external address mode.
ADDR2/PWM	10	Functions as device address 2 in external address mode; Functions as PWM input in internal address mode.
DIAG1	11	Diagnosis group 1 pin.
DIAG0	12	Diagnosis group 0 pin.
LED0	13	LED0 current sink.
LED1	14	LED1 current sink.
GND	15	Ground.
LED2	16	LED2 current sink pin.
LED3	17	LED3 current sink pin.

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LED4	18	LED4 current sink pin.
LED5	19	LED5 current sink pin.
NC	20	Not connected.
LED6	21	LED6 current sink pin.
LED7	22	LED7 current sink pin.
LED8	23	LED8 current sink pin.
LED9	24	LED9 current sink pin.
GND	25	Ground.
LED10	26	LED10 current sink pin.
LED11	27	LED11 current sink pin.
LED12	28	LED12 current sink pin.
LED13	29	LED13 current sink pin.
NC	30	Not connected.
LED14	31	LED14 current sink pin.
LED15	32	LED15 current sink pin.
LED16	33	LED16 current sink pin.
LED17	34	LED17 current sink pin.
GND	35	Ground.
LED18	36	LED18 current sink pin.
LED19	37	LED19 current sink pin.
LED20	38	LED20 current sink pin.
LED21	39	LED21 current sink pin.
NC	40	Not connected.
LED22	41	LED22 current sink pin.
LED23	42	LED23 current sink pin.
VS	43	Power supply for device and output current channel.
NC	44	Not connected.
NC	45	Not connected.
GND	46	Ground.
ADDR0	47	Device address 0 in external address mode.
EBIN	48	BIN class setting pin.
Exposed Pad	49	Connect to GND with multiple vias.

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Block Diagram

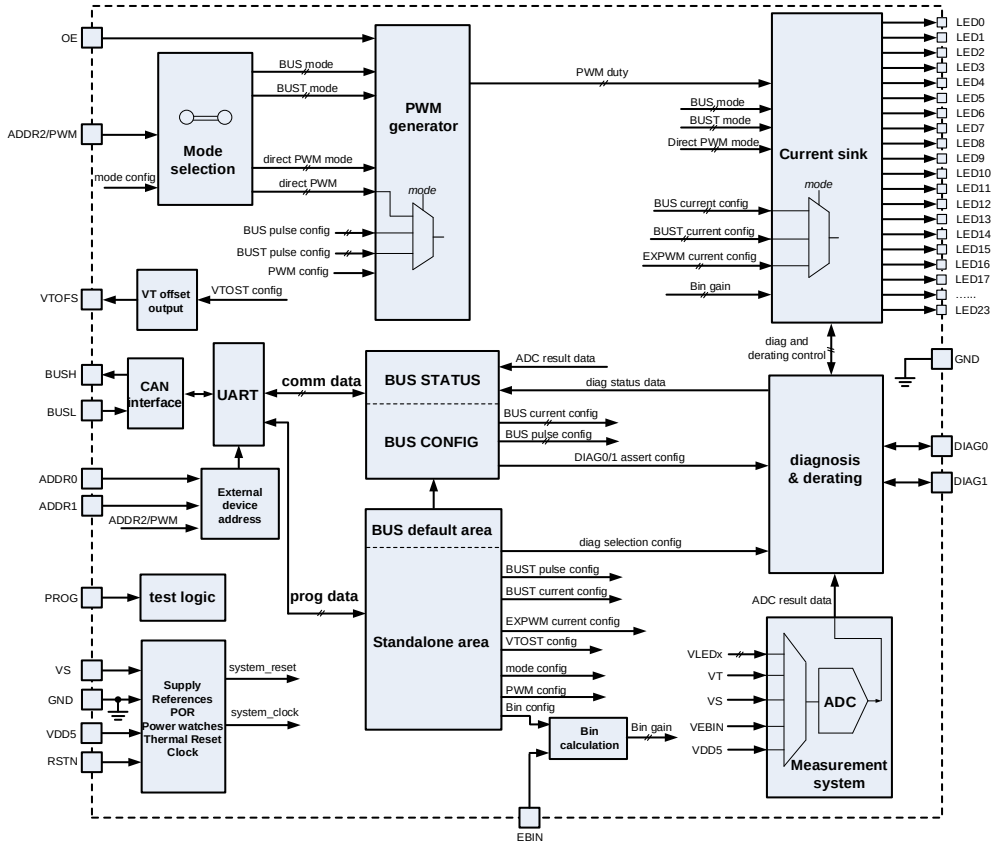

Figure.2 Functional Block Diagram

Absolute Maximum Ratings (Note 1)

Parameter	Min	Max	Unit
VS, RSTN, PROG, ADDR1, ADDR2/PWM, OE, DIAG0, DIAG1	-0.3	20	V
BUSH, BUSL, VTOFS	-0.3	20	
VDD5	-0.3	5.5	
EBIN/ADDR0	-0.3	5.5	
LEDn(n=0...23)	-0.3	20	
Maximum Junction Temperature		150	°C
Lead Temperature (Soldering, 10 sec.)		260	
Storage Temperature Range	-65	150	

Thermal Information (Note 2)

Parameter		Min	Max	Unit
$R_{\theta JA}$	Junction-to-ambient thermal resistance		19.2	°C/W
$R_{\theta JC}$	Junction-to-case (top) thermal resistance		9.5	°C/W
$R_{\theta JC}$	Junction-to-case (bottom) thermal resistance		1.6	°C/W

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Recommended Operating Conditions (Note 3)

No.	Description	Condition	Symbol	Min	Typ	Max	Unit
1	Ambient Temperature		TA	-40		125	°C
2	Voltage at Pin **VS**	during startup, at least 1 ms	V_{start_VS}	4.9		16	V
3	Voltage at Pin **VS**	after startup	V_{func_VS}	4.7		16	V
4	Voltage at Pin **RSTN**		V_{func_RSTN}	0		18	V
5	Voltage at Pin **PROG**		V_{func_PROG}	0		18	V
6	Full Functionality VDD5 Working Range (Note 6)		V_{func_VDD5}	4.5		5.4	V
7	External Capacitance at **VDD5** pin (Note7)		C_{VDD5}	400			nF
8	Tolerated Voltage at Pin **BUS**_x	x=H/L	$V_{tol_BUS_x}$	0		18	V
9	Functional Voltage Range at Pin **BUS**_x for RX Module	x=H/L	$V_{func_RX_BUS_x}$	0		5.4	V
10	Functional Voltage Range at Pin **TXD** for RX Module		$V_{func_RX_TXD}$	0		5.4	V
11	Functional Voltage Range at Pin **RXD** for RX Module		$V_{func_RX_RXD}$	0		5.4	V
12	Voltage at pin **ADDR1**		V_{func_ADDR1}	0		18	V
13	Voltage at pin **ADDR2/PWM**		$V_{func_ADDR2/PWM}$	0		18	V
14	Voltage at Pin **OE**		V_{func_OE}	0		18	V
15	Voltage at Pin **EBIN**, Full Functional Working Range		V_{func_EBIN}	0		V_{VDD5}-0.5	V
16	Voltage at pin **ADDR0**, full functional Working Range		V_{func_ADDR0}	0		V_{VDD5}-0.5	V
17	Tolerated Voltage at Pin **DIAGn**	n=0/1	V_{tol_DIAGn}	0		18	V
18	Voltage at Pin **DIAGn**, Full Functional Working Range	n=0/1	V_{func_DIAGn}	0		5.4	V
19	Voltage at Pin **LEDn**, Full Functional Working Range	I_{chn}=100mA, all channels on n=0...23	V_{func_LEDn}	0.8		16	V
20	Tolerated Voltage at Pin **LEDn**, Reduced Functionality Operating Range (Note 8)	I_{chn}=100mA, all channels on n=0...23	$V_{red_func_LEDn}$	0		0.8	V
21	Voltage at **VTOFS**, Full Functional Working Range		V_{func_VTOFS}	0		2	V

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Electrical Characteristics (Note 4)

(V_{VS} = 5V to 16V, TA = -40°C to +125°C, unless otherwise noted. Typical values are at V_{VS} = 9V and TA = +25°C. Positive currents flow into the device pins.)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Power Supply						
VS turn-on threshold	V_{VS_ON}		4.5	4.7	4.9	V
VS turn-off threshold	V_{VS_OFF}		4.3	4.5	4.7	V
Quiescent Current, All Channels off	$I_{Q(OFF)}$				20	mA
Quiescent Current, All Channels on	$I_{Q(ON)}$				26.5	mA
Voltage Regulator 5V						
Regulator Output Idle State	V_{VDD5_REG}	VS= 9V minimal internal current consumption		5.0		V
Dropout Voltage V_{VDD5}	V_{VDD5_DROP}	VS=12V, I_{VDD5} = 0 to 20mA		10		mV
VDD5 Reset Threshold, Rising supply	$V_{VDD5_OK_LH}$			4.72		V
VDD5 Reset Threshold, Falling supply	$V_{VDD5_OK_HL}$			$V_{VDD5_OK_LH-0.7}$		V
LDO Maximum Current Capacity	V_{VDD5_IMAX}	V_{VS}= 9V	15			mA
PWM System						
PWM Direct PWM Frequency (Note 5)	F_{DIRECT_PWM}			300		Hz
PWM System Clock	$F_{PWM_SYS_CLK}$			8		MHz
Internal Oscillator Clock	F_{OSC_CLK}			48		MHz
LED Current Sinks						
Minimum Headroom of CHx	V_{MIN_HR}	I_{chn}=100mA, all channels on			0.8	V
Ref of Channel Current	$V_{REF_CHX_1}$	Irange=100mA		150		mV
Ref of Channel Current	$V_{REF_CHX_2}$	Irange=50mA		75		mV
Overall Accuracy of Select Current	$I_{SINK_ACC_OVA_55}$	20mA≤I_{LED}<55mA	-5		5	%
Overall Accuracy of Select Current	$I_{SINK_ACC_OVA_100}$	55mA≤ILED≤100mA	-4		4	%
Channel Matching Accuracy	$I_{SINK_ACC_CH_55}$	20mA≤ILED<55mA	-2.5		2.5	%
Channel Matching Accuracy	$I_{SINK_ACC_CH_100}$	55mA≤ILED≤100mA	-2		2	%
Rise Time 10% to 90%	$T_{SINK_RISE_0}$	Slew=0		170		ns
Fall Time 90% to 10%	$T_{SINK_FALL_0}$	Slew=0		30		ns
Rise Time 10% to 90% (Note 5)	$T_{SINK_RISE_1}$	Slew=1		5		µs
Fall Time 90% to 10% (Note 5)	$T_{SINK_FALL_1}$	Slew=1		5		µs
Rise Time 10% to 90% (Note 5)	$T_{SINK_RISE_2}$	Slew=2		10		µs
Fall Time 90% to 10% (Note 5)	$T_{SINK_FALL_2}$	Slew=2		10		µs
Rise Time 10% to 90% (Note 5)	$T_{SINK_RISE_3}$	Slew=3		21		µs
Fall Time 90% to 10% (Note 5)	$T_{SINK_FALL_3}$	Slew=3		21		µs
Input Current When Off	I_{SINK_LEAK}	Current sink disables or PWM duty=0			5	µA

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VT Offset Output						
VTOFS Maximum Output	V_{VTOFS_MAX}			2		V
EBIN Output						
Overall Accuracy of VEBIN output Current	I_{EBIN}	I_{EBIN}=0.5,1mA	-6.5		6.5	%
ADDR0 Output						
Overall accuracy of ADDR0 output current	I_{ADDR0}	I_{ADDR}=0.5,1mA	-6.5		6.5	%
ADC & Measurement System						
Measurement System						
Gain Factor of ADC Mux, VS	A_{MEAS_VS}			46		LSB/V
Gain Factor of ADC Mux, LED Pin Voltage	A_{MEAS_VLED}			46		LSB/V
Gain Factor of ADC Mux, VDD5	A_{MEAS_VDD5}			184		LSB/V
Gain Factor of ADC Mux, EBIN	A_{MEAS_EBIN}			460		LSB/V
Gain Factor of ADC Mux, Temperature	A_{MEAS_VT}			1		LSB/K
relative error fraction of measurement, channel VLED, VS	$E_{MEAS_REL_VLED}$ $E_{MEAS_REL_VS}$				3	%
relative error fraction of measurement, VDD5/EBIN	$E_{MEAS_REL_VDD5}$ $E_{MEAS_REL_EBIN}$				2	%
uncertainty error fraction of measurement, channel VLED, VS	$E_{MEAS_UNC_VLED}$ $E_{MEAS_UNC_VS}$				300	mV
uncertainty error fraction of measurement, channel VDD5, EBIN	$E_{MEAS_UNC_VDD5}$ $E_{MEAS_UNC_EBIN}$				70	mV
SAR ADC (Note 5)						
Resolution	NADC			10		bit
Conversion Rate	F_{ADC_CONV}			67		kS/s
Digital IOs						
Input Voltage for Digital "1"	V_{DIG_IH}		2			V
Input Voltage for Digital "0"	V_{DIG_IL}				0.8	V
Input Hysteresis	V_{DIG_HYST}		0.3			V
Positive Supply of Internal Pull Resistor	V_{DIG_PULL}			3.3		V
Pull Resistor	R_{DIG_PULL}			110		kΩ
PROG Pin Pull Resistor	$R_{DIG_PULL_PROG}$			56		kΩ
Output Voltage for Digital "0"	V_{DIG_OL}	4mA load			0.5	V
Analog Low-pulse Debounce Filter for Pins RSTN and PROG	T_{DIG_DEB}			10		µs
Digital Low-pulse Debounce Filter for Pins OE, DIAG0 and DIAG1	$T_{DIG_DEB_OE_DIAG}$		40		100	µs
Digital Low-pulse Debounce filter for ADDR2/PWM pin	T_{ADDR2/PWM_RC}			0.75		µs
UART Peripheral Bus Interface						
UART Receiver						

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Differential Receiver Threshold Voltage	$V_{th(RX)dif}$		500		900	mV
Input Hysteresis	$V_{BUS_RX_HYST}$		50			mV
Internal Common Mode Level	$V_{BUS_RX_VCM}$			2.5		V
Input Resistance	$R_{BUS_RX_IN}$		10		100	kΩ
UART Transmitter						
BUS_H Voltage in Dominant State	$V_{BUS_DRV_H}$	RTERM=100Ω	3		4.5	V
BUS_L Voltage in Dominant State	$V_{BUS_DRV_L}$	RTERM=100Ω	0.8		2.25	V
Bus Differential Voltage in Dominant State	$V_{BUS_DRV_DIFF}$	RTERM=100Ω	1.5			V
BUS_H Current Limit	$I_{BUS_LIMIT_H}$	BUS_H shorted to device ground		-70		mA
BUS_L Current Limit	$I_{BUS_LIMIT_L}$	BUS_L shorted to device supply		70		mA
Thermal Section						
Thermal Shut Down Temperature	T_{SD}			170		ºC
Thermal Hysteresis for Recovery	T_{THERM_HYST}			10		ºC

Note 1: Stresses beyond the “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: θ_{JA} is measured in the natural convection at T_A = 25°C on a 2oz four-layer Silergy evaluation board. Case temperature θ_{JC} is measured at the exposed pad.

Note 3: The device is not guaranteed to function outside its operating conditions.

Note 4: Unless otherwise stated, limits are 100% production tested under pulsed load conditions such that $T_A \cong T_J$ = 25C. Limits over the operating temperature range (See recommended operating conditions) and relevant voltage range(s) are guaranteed by design, test, or statistical correlation.

Note 5: Guaranteed by design or statistical correlation and not production tested.

Note 6: VDD5 is intended to be driven by the integrated voltage regulator. It should not be driven or loaded externally

Note 7: Ceramic capacitors derate over lifetime and bias voltage. It is recommended to choose a part with a higher nominal value to ensure the minimum requirement of 680nF.

Note 8: The current sinks operate normally and provide datasheet accuracy until they reach saturation. To maintain regulation, the voltage across the sink has to be above 0.8V for the entire current range.

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Functional Description

1. Introduction

The SA32774 is a 24-channel LED driver designed for automotive rear lights or ambient lighting. It features a maximum sink current of 100 mA per channel with 10-bit resolution. There are two ways to control the PWM pulse length. The first is to adjust the pulse length with an external PWM input. The second is to adjust the internal registers using the serial interface, which also have 10-bit resolution for accurate dimming.

If the SA32774 is controlled by an MCU, there are two modes to achieve the brightness adjustment. It will operate in BUS mode during normal communication. During BUS mode, the current and the PWM pulse length follow the registers which are set by the MCU. If the MCU is idle for a long period, and the BUS Timeout is enabled, the SA32774 will enter BUS Timeout mode. In this state, the current and the PWM pulse length follow the registers stored in MTP.

The diagnosis is based on an internal 10-bit ADC. LED open, LED short, over temperature, Critical VS, VS too low, EBIN short/open, VTOFS short/open, etc., are supported. There are two diagnosis groups to select how the 24 channels behave in different situations.

The UART baud rate of up to 2Mbps helps to achieve fast dynamic dimming. The integrated CAN PHY helps improve the EMI performance.

2. Mode Selection

2. 1 Mode Configured by PWM

The ADDR2/ PWM pin is a multi-function pin is used for external PWM input signal and as device peripheral address selection pin. The register COM_DEV_ADDR [9] must be written to enable direct PWM function.

The device implements three operating modes to support different applications: BUS mode, BUS Timeout mode and direct PWM mode.

The following figure illustrates the modes controlled by the PWM pin state. Each mode features its own PWM pulse length and current sink configuration data set. Each channel includes a one-bit configuration to select the PWM pin for mode control. Detailed information is provided in the registers PWMIN_ENABLE_x_x.

The BUS mode is the default mode for MCU communication. If there is no valid communication for a long period and the BUS timeout mode is enabled, the device will enter BUS timeout mode. No valid communication means there is no data from the MCU, or the CRC verification of the data frame is incorrect. The direct PWM mode means the pulse length is controlled by the external pin PWM.

Both BUS and BUS Timeout modes have their own PWM pulse length and LED current data. The PWM pulse length in direct PWM mode is controlled by the external PWM pin. The following figure illustrates the state diagram of the three modes. The state changes are driven by the PWM pin, and the detection timing is configurable.

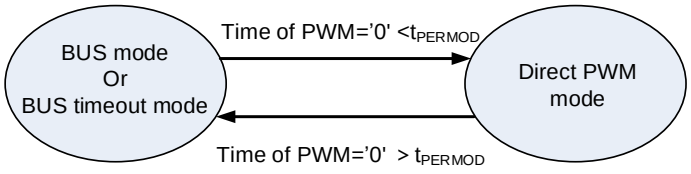

Fig 2.1.1. Mode Selection

As shown above, PWM input implements the following states:

1). BUS mode or BUS timeout mode: when the input level of PWM pin is static 0.

2). Direct PWM mode: when the PWM pin receives a valid PWM signal.

In BUS mode and BUS Timeout modes, a 2µs blanking time helps to filter noise. If the duration of a high-level signal is longer than 2µs, the device will enter direct PWM mode. If the duration of a high-level signal is less than 2µs, the signal will be ignored.

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In direct PWM mode, when the duration of the low level is longer than T_{PERMOD}, the device will enter BUS mode. When the mode changes, the corresponding PWM pulse length and LED current becomes active immediately.

2.2 Bus Communication Timeout

If the standalone area of timeout mode configuration (COM_TIMEOUT.val) is programmed to a non-zero value, the timeout detection becomes active after device startup. When a bus communication timeout occurs, all channels in BUS mode enter BUS Timeout mode. The PWM pulse length and LED current are adjusted according to the data set of BUS timeout mode, which is loaded from MTP.

The communication timeout counter is reset by a valid bus frame header from the MCU, regardless of whether it is a write or read frame. Following a correct frame header, the device remains in BUS mode or transitions from BUS Timeout mode to BUS mode. The BUS Timeout mode can only be entered from BUS mode. The LED channels operating in direct PWM mode will not be affected when a BUS Timeout occurs.

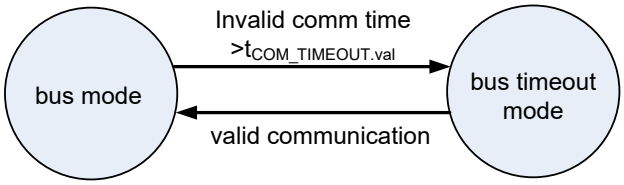

Fig 2.2.1. BUS Mode and BUS Timeout Mode

Related registers summary. For a detailed description, see the register table.

Standalone Area			
Register Name	Register Page	Address	Description
PWMIN_TIMING	1	0XFC	direct PWM mode time interval
PWMIN_ENABLE_0_7	1	0XFD	configure LED0~7 controlled by PWM pin
PWMIN_ENABLE_8_15	1	0XFE	configure LED8~15 controlled by PWM pin
PWMIN_ENABLE_16_23	1	0XFF	configure LED16~23 controlled by PWM pin
COM_TIMEOUT	2	0XE1	BUS timeout setting. BUS timeout error indicates on DIAG0/DIAG1 or not.

3. PWM System

3.1 PWM Generator of BUS/BUS Timeout Mode

The PWM system generates the PWM pulse length to adjust the brightness of the LED driver. It consists of a common PWM period generator (configured using PWM_PRESCALER and PWM_PERIOD) and 24 independent PWM pulse generators (configured using the PULSE_x registers).

The figure below illustrates the structure of the PWM generator. The PWM frequency is determined by the $f_{PWM_sys_clk}$(8MHz) system clock, the prescaler counter and the period counter. The PULSE_x represents the pulse duty-cycle for channel x.

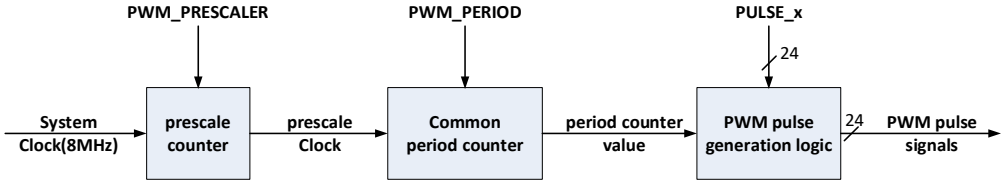

Fig 3.1.1. PWM Generator Structure

The timing figure below illustrates an example of the timing for the prescaler counter, the period counter, and the different pulse lengths of the LED channels a, b, and c.

In this example the prescaler is configured with a value of 5, resulting in a prescaler dividing factor of 6 system clock cycles.

The period counter in this example is configured with a value of 4 which results in counting from 0 to 3. The period counter will increase every time the prescaler counter resets to 0 when it reaches its configuration value. The period counter resets to 0 when it reaches its period configuration value minus one, and is configured by the register PWM_PERIOD. The PWM pulse length of channel A is configured to 2, the PWM pulse length of channel b is configured to 3 and the PWM pulse

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length of channel c is configured to 4. If the PWM pulse length of a channel is configured to be longer than the PWM period, the duty cycle of this channel will always stay at 100%.

The period counter in this example is configured with a value of 4, resulting in a count from 0 to 3. It increases each time the prescaler counter resets to 0 after reaching its configured value. The period counter resets to 0 when it reaches its configured period value minus one. It is configured by the register PWM_PERIOD. The PWM pulse length of channel A is set to 2, the PWM pulse length of channel b is set to 3, and the PWM pulse length of channel c is set to 4. If the PWM pulse length of a channel is configured to be longer than the PWM period, the duty cycle of that channel will always remain at 100%.

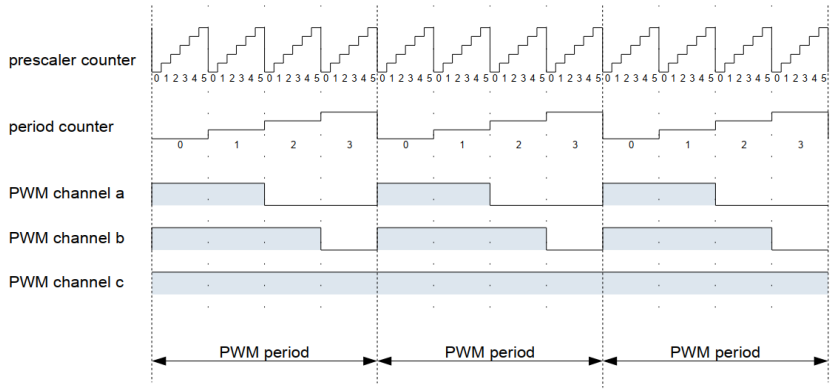

Fig 3.1.2. PWM Prescaler, Period and Pulse Timing

The maximum value of the PWM_PERIOD register should be set to 1023; otherwise, the PWM pulse adjustment will not utilize the full 10-bit resolution.

Each channel has its own PWM pulse length register to generate its duty-cycle. The PWM pulse starting points of the 24 channels can be configured in two ways using the PWM_CONFIG:

- All PWM pulses start at the same time-stamp
    - Adjacent PWM channel pulse starting point distance = 0
- All PWM pulse starting points are distributed equidistantly over the PWM period
    - Adjacent PWM channel pulse starting point distance = PWM period / 24

The following figure illustrates an example of equidistantly distributed PWM channel starting timestamps, with all PWM channels configured for a 75% duty cycle. The colored sections indicate the virtual PWM periods of the different PWM channels.

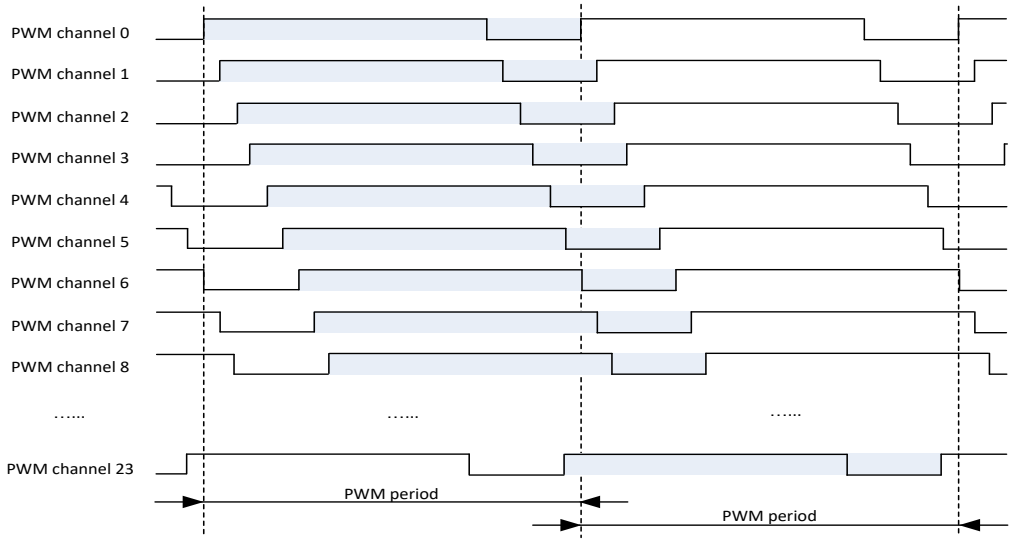

Fig 3.1.3. Equidistantly Distributed Timing Example

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The device supports combining two channels for applications requiring higher LED current. When two LED PWM channels are combined (using the PWM_COMBINE_x values), the PWM pulse length of the secondary channel will follow that of the main channel, meaning these PWM channels are active during the same time period.

The following figure illustrates an example of combined PWM channel timing. In this example, 12 groups of 2 adjacent LED PWM channels are combined.

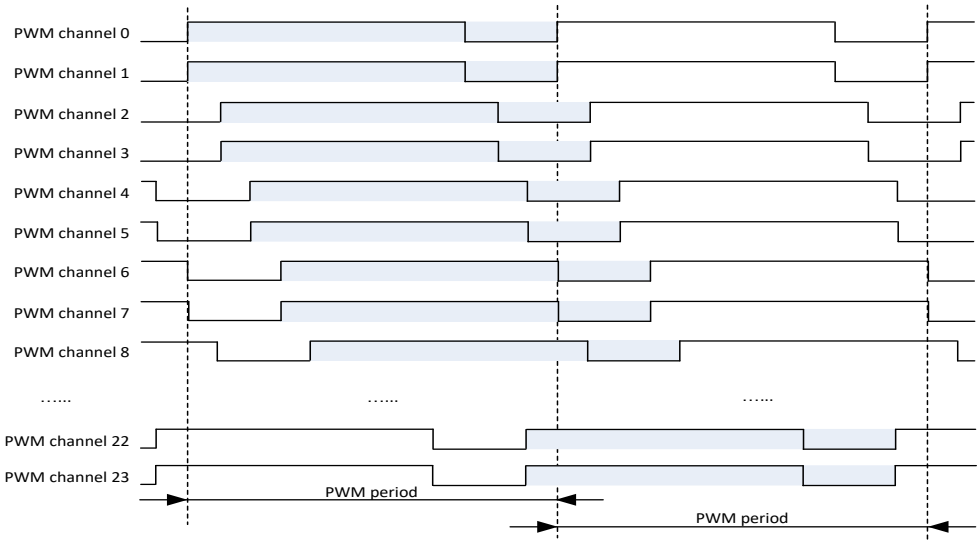

Fig 3.1.4. Combined PWM Channels Example

3.2 Direct PWM Mode PWM Generator

In direct PWM mode, the PWM signals from the external pin ADDR2/PWM are sampled by the internal system clock. The duty-cycle is recalculated to generate the PWM pulse signal, as shown below. The ADDR2/PWM and LED PWM periods are independent.

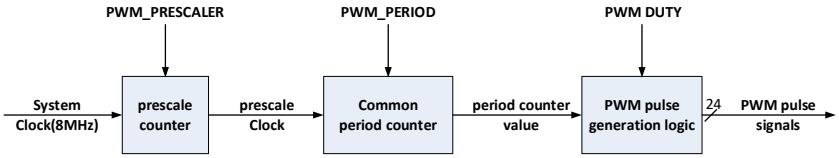

Fig 3.2.1. PWM Generator Structure

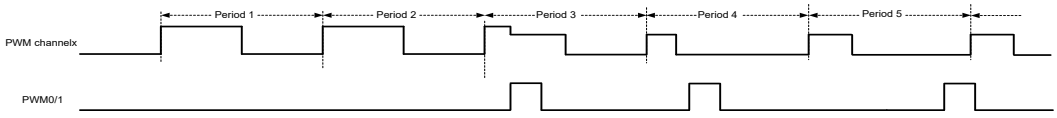

Fig 3.2.1. Direct PWM Waveform

3.3 PWM Masking by OE Pin

An option is available (using STANDALONE PWM_CONFIG) to apply masking behavior to LED channels in BUS timeout mode.

When the OE pin is inactive (the default setting is low level), the PWM signal of all LED channels in BUS timeout mode will be disabled, which means that the related LED channels are set to off-state. When the OE pin is active (the default setting is high level), this mask is removed, and PWM signals of LED channels in BUS timeout mode transition to normal operation.

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A summary of related registers is found below:

BUS_CONFIG area			
register name	register page	address	description
BUS_PULSE_0	-	0X00	LED0 pulse length setting in BUS mode
BUS_PULSE_1	-	0X01	LED1 pulse length setting in BUS mode
.....	.....	.....	.....
BUS_PULSE_23	-	0X17	LED23 pulse length setting in bus mode
BUS_PULSE_ALL	-	0X30	Update all the pulse length
standalone area			
BUST_PULSE_0	1	0XC0	LED0 pulse length setting in BUS timeout mode
BUST_PULSE_1	1	0XC1	LED1 pulse length setting in BUS timeout mode
.....	.....	.....	.....
BUST_PULSE_23	1	0XD7	LED23 pulse length setting in BUS timeout mode
PWM_PRESCALER	1	0XF6	LED PWM clock division setting
PWM_PERIOD	1	0XF7	LED PWM period setting
PWM_CONFIG	1	0XF8	Set OE function for BUST timeout and PWM pulse start timing configuration Enable Phase shift
PWM_COMBINE_1	1	0XF9	CH0~CH15 channel combine
PWM_COMBINE_2	1	0XFA	CH16~CH23 channel combine

4. LED Current Sink

4.1 Current Set

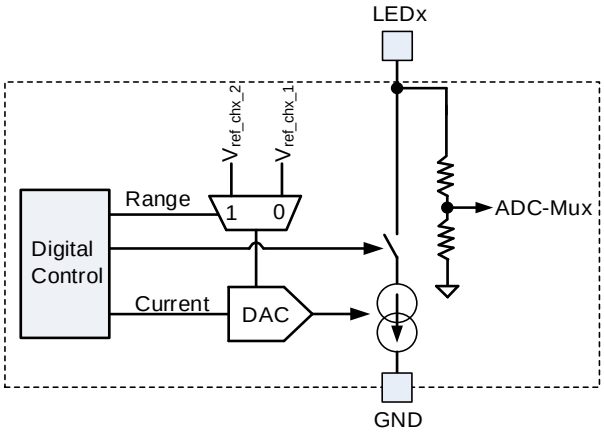

Fig 4.1.1. ISINK Block Diagram

The current sink gets the peak current information and the PWM pulse length from the digital registers.

The reference for each channel is based on a DAC with a selectable full-scale range. The range can be selected using the IDAC_REF_SEL_x.

The current slew rate is configurable by the setting ISINK_CONFIG to improve EMC performance.

The pin voltage and actual current is monitored by an internal ADC for diagnosis purpose.

It is recommended to set the unused LED channels to OFF to save power. Use LED_ENABLE_x_x (BUS mode) or LED_ENABLE2_x_x (BUS timeout/direct PWM mode) for this configuration.

The following figures show the relation between the current configuration value and the expected LED current. The LED current will saturate when the digital code is beyond the selected range maximum current value. Below the selected range minimum current value, the LED current accuracy is reduced. For this reason, it's not recommended to select a LED current outside the selected range.

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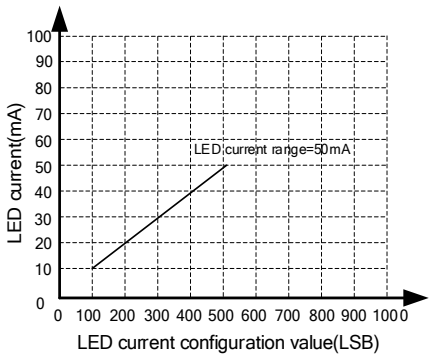

Fig. 4.1.2. LED Current Sink 40mA Range Behavior

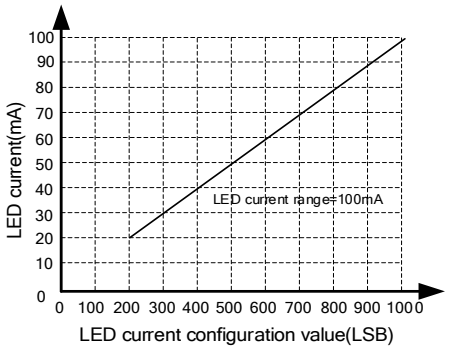

Fig. 4.1.3. LED Current Sink 100mA Range Behavior

Optimizing EMI is possible by adjusting the slew rate, with a higher value resulting in lower EMI. Each channel current can be independently configured using one of the settings below:

Setting value	slope time
ISINK_CONFIG.slew=0	0.1us
ISINK_CONFIG.slew=1	5us
ISINK_CONFIG.slew=2	10us
ISINK_CONFIG.slew=3	21us

4.2 LED Current Derating

For the device temperature protection, the SA32774 supports supply-voltage based derating of the LED currents, as well as core-temperature based derating.

• Supply voltage-based derating starts at VS_{start}, and decreases the channel current with the rate set by DERATE_GAIN.vs_gain.

• Chip junction-temperature based derating can be used to decrease the current further.

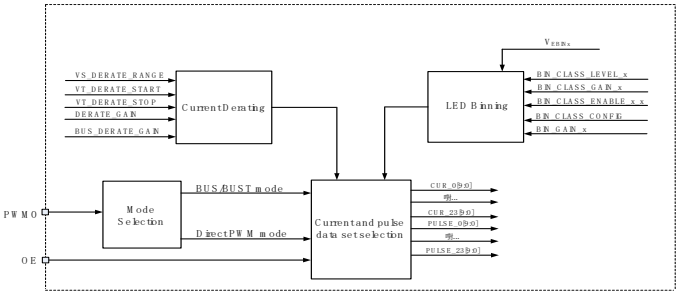

Fig. 4.2.1. LED Current Derating Diagram

These two independent derating types based on LED supply and the device temperature can be configured to derate the LED current as illustrated in the following figures. The supply voltage and junction temperature values are obtained from

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the ADC. The start and stop points for derating must be set according to the ADC gain factor.

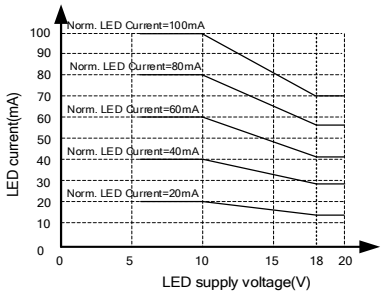

Fig. 4.2.2. LED Supply Voltage Based Derating Example

The figure above is an example about the supply voltage-based derating:

• derating start value of LED supply = 10V (VS_DERATE_RANGE.start = 9D or 09H, 0.9LSB/V)

• derating stop value of LED supply =18V (VS_DERATE_RANGE.stop = 16D or 10H, 0.9LSB/V)

• derating gain select value = 15 (DERATE_GAIN.vs_gain=15D or 0FH)

The maximum LED derating percentage:

• (18V-10V) ×15 / (16 × 25) = 30.0% ---------- (VS-VS_{start}) × vs_gain/(16×25)

Using a nominal LED current of 100mA, the derating stop current will be at:

• 100mA × (1-30.0%) =70.0mA

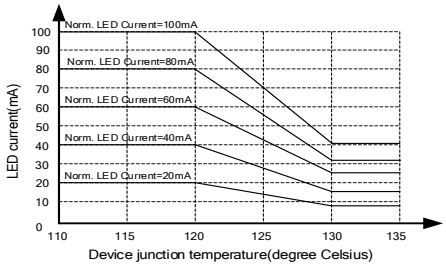

Fig. 4.2.3. Device Junction Temperature Based Derating Example

The figure above shows an example about the device junction temperature-based derating:

• derating start VT value = 120°C (VT_DERATE_ START =120+273=393D)

• derating stop VT value = 130°C (VT_DERATE_STOP=130+273=403D)

• derating gain select value = 15 (DERATE_GAIN.vt_gain=15D)

The maximum LED derating percentage:

• 15 × (403 - 393) / 256 = 58.5% ------ vt_gain × (VT_{stop} - VT_{start}) / 256

Using a nominal LED current of 100mA, the final stop current will be at:

• 100mA × (1-58.5%) =41.5mA

The external MCU can also use commands to derate the LED current by setting the register BUS_DERATE_GAIN. Therefore, the overall LED current derating factor is defined by three parameters: VS derating, temperature derating, and BUS_DERATE_GAIN.

4.3 LED Binning

To support different LED current bin classes, the device supports two configuration methods shown below:

Use the BIN_GAIN_X register for each channel.

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The second method is to set EBIN_AND_ADDR0_CUR for a selected group. The voltage drops over the external resistor connected to the EBIN pin is used for LED binning selection.

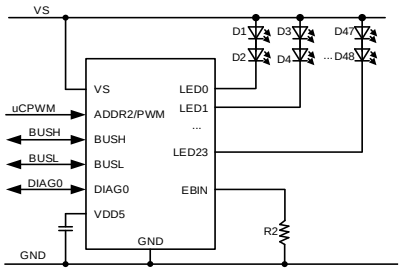

Fig. 4.3.1. Bin Class Example

The bin class function supports four settable bin class levels (configured using BIN_CLASS_LEVEL_x registers) and five settable bin class gains (configured by BIN_CLASS_GAIN_x registers). The ADC measurement value of the EBIN pin is compared to the threshold level. The resistor value and the source current (configured by EBIN_AND_ADDR0_CUR) of the EBIN pin determine the voltage drop. The corresponding bin class gain is applied to the LED channels (configured by EBIN_CLASS_ENABLE_x_x).

EBIN_CLASS_ENABLE_0_7 enable bin class with EBIN for ch0~ch7；

EBIN_CLASS_ENABLE_8_15 enable bin class with EBIN for ch8~ch15；

EBIN_CLASS_ENABLE_16_23 enable bin class with EBIN for ch16~ch23;

The following figure shows an example of the bin class function.

Suppose the EBIN source current is 1mA. The voltage drop of external resistor is sampled once per LED PWM period.

The EBIN saturation voltage is VDD5-0.5V. It's recommended to keep the EBIN under the saturation voltage.

• BIN_CLASS_LEVEL_0 = 128LSB (0.5V*460LSB/V=230LSB)

• BIN_CLASS_LEVEL_1 = 256LSB (1V*460LSB/V=460LSB)

• BIN_CLASS_LEVEL_2 = 384LSB (1.5V*460LSB/V=690LSB)

• BIN_CLASS_LEVEL_3 = 512LSB (2.0V*460LSB/V=920LSB)

• BIN_CLASS_GAIN_0 = 0x180 (-25%)

• BIN_CLASS_GAIN_1 = 0x1C0 (-12.5%)

• BIN_CLASS_GAIN_2 = 0x200 (+0%)

• BIN_CLASS_GAIN_3 = 0x240 (+12.5%)

• BIN_CLASS_GAIN_4 = 0x280 (+25%)

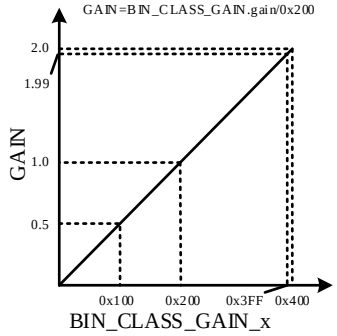

Fig. 4.3.2. BIN_CLASS_GAIN_x VS. Gain

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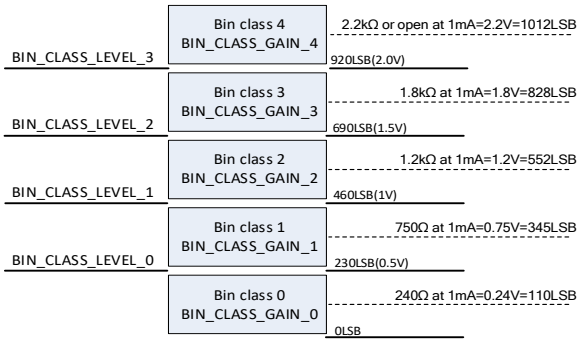

Fig. 4.3.3. Example Bin Class Table

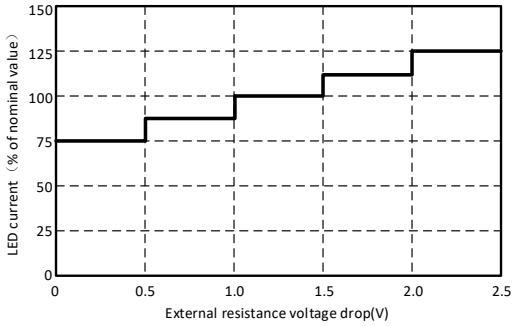

Fig. 4.3.4. LED Binning Example

If the bin class function of a LED channel (set by EBIN_CLASS_ENABLE_x_x) is enabled, the related general LED bin gain (set by BIN_GAIN_X) is not used. The bin class setting has a higher priority.

4.4 VT Offset for LED Compensation

To reduce power loss during high temperature operation, the SA32774 supports enabling an output offset voltage based on junction temperature to decrease the voltage of the external DC/DC converter.

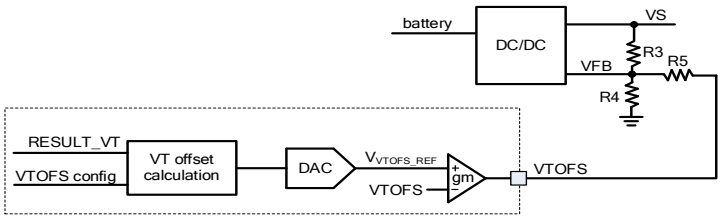

Fig. 4.4.1. VT Offset Output Diagram

To reduce the influence of the external resistor on the DC/DC circuit, the R5 value is recommended to be at least 10 times the value of R4. For example, VS=7V, R3=52.7kΩ, R4=12kΩ, R5=140kΩ, V_{FB}=1.2V. to satisfy a VS drop to 6.7V at 150℃.

$$\frac{7-6.7}{R3}=\frac{2-1.2}{R5}$$

VT_OFFSET_TSTART= (125+273) *1LSB/℃=398LSB.

VT_OFFSET_TSTOP= (150+273) *1LSB/℃=423LSB.

The VTOFS pin has only sourcing capacity and does not have sink capacity. The design curve and the actual curve do not coincide. Assuming that the DC-DC converter feedback reference voltage is 1.2V, the actual curve is represented by the blue line, while the design curve is represented by the black line.

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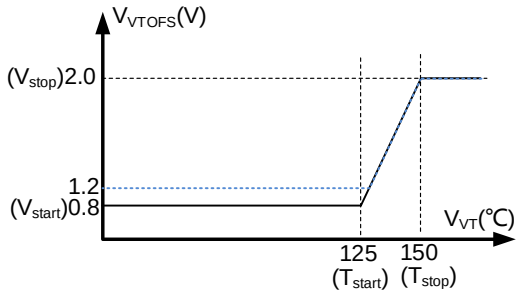

Fig. 4.4.2. VT Offset Output Curve

$$V_{VTOFS} = V_{start} + \frac{V_{stop} - V_{start}}{T_{stop} - T_{start}} \cdot (T_{real} - T_{start})$$

Vstart has a constant value of 0.8V. Vstop has a constant value of 2V.

Register Memory Map. For a detailed description, please see the register table.

BUS_CONFIG area			
register name	register page	address	description
BUS_CURRENT_0	-	0X18	LED0 current peak setting in bus mode
BUS_CURRENT_1	-	0X19	LED1 current peak setting in bus mode
.....	.....	.....	.....
BUS_CURRENT_23	-	0X2F	LED23 current peak setting in bus mode
LED_ENABLE_0_7	-	0X32	Channel enable for LED0~7 in bus mode
LED_ENABLE_8_15	-	0X33	Channel enable for LED8~15 in bus mode
LED_ENABLE_16_23	-	0X34	Channel enable for LED16~23 in bus mode
BUS_DERATE_GAIN	-	0X35	Set the overall gain of all 24 channels
BUS_CURRENT_ALL	-	0X31	Update the current peak of all 24 channels
Standalone area			
BUST_CURRENT_0	1	0XD8	LED0 current peak setting in BUS timeout mode
BUST_CURRENT_1	1	0XD9	LED1 current peak setting in BUS timeout mode
.....	.....	.....	.....
BUST_CURRENT_23	1	0XEF	LED23 current peak setting in BUS timeout mode
EXPWM_CURRENT_0	2	0XE5	LED0 current peak setting in direct PWM mode
EXPWM_CURRENT_1	2	0XE6	LED1 current peak setting in direct PWM mode
.....	.....	.....	.....
EXPWM_CURRENT_23	2	0XFC	LED23 current peak setting in direct PWM mode
LED_ENABLE2_0_7	1	0XF0	Channel enable for LED0~7 in BUS timeout and direct PWM mode
LED_ENABLE2_8_15	1	0XF1	Channel enable for LED8~15 in BUS timeout and direct PWM mode
LED_ENABLE2_16_23	1	0XF2	Channel enable for LED16~23 in BUS timeout and direct PWM mode
Standalone area			
BIN_GAIN_0	3	0XC0	LED0 bin gain setting
BIN_GAIN_1	3	0XC1	LED1 bin gain setting
.....	.....	.....	.....
BIN_GAIN_23	3	0XD7	LED23 bin gain setting
EBIN_AND_ADDR0_CUR	3	0XD8	Set the source current of EBIN and ADDR0
EBIN_CLASS_ENABLE_0_7	3	0XD9	EBIN bin class enable for LED0~7
EBIN_CLASS_ENABLE_8_15	3	0XDA	EBIN bin class enable for LED8~15
EBIN_CLASS_ENABLE_16_23	3	0XDB	EBIN bin class enable for LED16~23

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BIN_CLASS_LEVEL_0	3	0XDF	LED bin class level 0 setting
BIN_CLASS_LEVEL_1	3	0XE0	LED bin class level 1 setting
BIN_CLASS_LEVEL_2	3	0XE1	LED bin class level 2 setting
BIN_CLASS_LEVEL_3	3	0XE2	LED bin class level 3 setting
BIN_CLASS_GAIN_0	3	0XE3	LED bin class gain 0 setting
BIN_CLASS_GAIN_1	3	0XE4	LED bin class gain 1 setting
BIN_CLASS_GAIN_2	3	0XE5	LED bin class gain 2 setting
BIN_CLASS_GAIN_3	3	0XE6	LED bin class gain 3 setting
BIN_CLASS_GAIN_4	3	0XE7	LED bin class gain 4 setting
IDAC_REF_SEL_0_7	1	0XF3	Range selection for LED0~7
IDAC_REF_SEL_8_15	1	0XF4	Range selection for LED8~15
IDAC_REF_SEL_15_23	1	0XF5	Range selection for LED16~23
ISINK_CONFIG	1	0XFB	Current slew rate setting
VS_DERATE_RANGE	3	0XE8	VS derating setting
VT_DERATE_START	3	0XE9	VT derating setting
VT_DERATE_STOP	3	0XEA	VT derating setting
DERATE_GAIN	3	0XEB	Derating gain setting for VS and VT derating
VT_OFFSET_TSTART	2	0XFE	VTOFST setting
VT_OFFSET_TSTOP	2	0XFF	VTOFST setting

5. ADC and Diagnosis

5.1 Measurement System

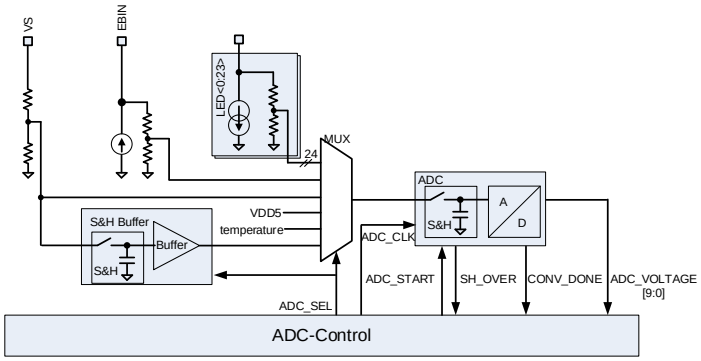

Fig. 5.1.1. Measurement System

The ADC is a 10-bit SAR ADC. The relationship between the conversion results and analog signals measured is shown below:

Sampled item	Gain factor		MAX.
LED voltage of each channel	A_{MEAS_VLED}	46LSB/V	18V
Internal temperature-sensor voltage	A_{MEAS_TEMP}	1LSB/K	453K
VDD5 voltage	A_{MEAS_VDD5}	184LSB/V	7.2V
EBIN	A_{MEAS_EBIN}	460LSB/V	2.22V
VS voltage (full range)	A_{MEAS_VS}	46LSB/V	18V

The LEDx voltages and supply voltage can be sampled simultaneously and converted in sequence. The result of the subtraction between the LEDx voltages and supply voltage is compared against the LED short detection threshold.

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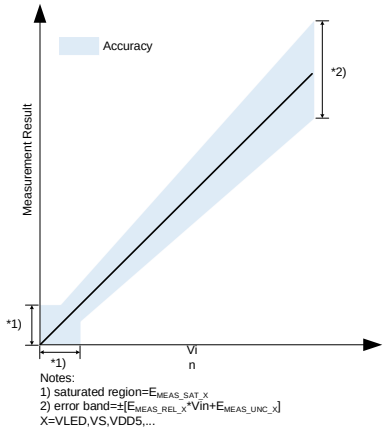

Fig. 5.1.2. Accuracy Diagram

The curve shown above shows the tolerances between the measurements and actual values:

There are two important aspects:

1) Very low input values may lead to saturation.

2) Normal input values suffer a combination of linear errors, which are a percentage value of the input plus some uncertainty.

These errors are the sum of temperature effects, ADC non-linearity and noise.

5.2 Diagnosis Operation

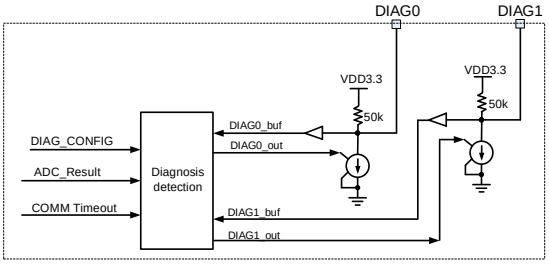

Fig. 5.2.1. DIAG0/DIAG1 Circuit

The SA32774 supports LED open and short detection for the enabled channels.

The LED short detects if the LEDn pin is shorted to VS pin. The LED open detects that the LEDn pin is open and doesn't sink a significant current, which can be caused by a damaged LED or LED disconnection.

The diagnosis runs once per PWM period. Each diagnosis event has its own error filter using a counter and a common error level value (set by DIAG_CONFIG.level).

If an LED error occurs, the filter counter will increment each PWM period. If the LED error disappears, the filter counter will decrement each PWM period until the counter reaches zero.

When the filter counter value reaches the DIAG_CONFIG.level value, an LED channel error flag will be set. If the filter counter value reaches 0, the filtered diagnosis state will recover, but the error flag is only cleared after reading corresponding status register.

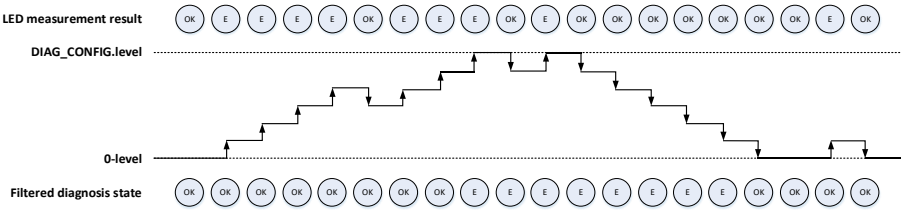

Fig. 5.2.2. Open and Short Diagnosis Filter Behavior

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An LED short is detected and signaled in case of:

• LED supply ADC measurement value is not saturated

• Short detection for the LEDn is enabled

• PWM is active and valid (LED current slewing has finished) during ADC measurement

An LED Open is Detected and Signaled in case of:

• LED supply is larger than the minimum LED supply level configured using VS_TOO_LOW

• Open detection for the LEDn is enabled

The SA32774 features two independent DIAG pins (two diagnosis groups). The device implements different modes of behavior depending on the DIAG0/1 pin configuration:

• diag_enable = 1, slm = 0:

  • an internal diagnosis error occurs:

    • The corresponding LED driver is switched to a retry measurement state

  • an external diagnosis error input from DIAG0/1:

    • This information will be ignored

• diag_enable = 1, slm = 1:

  • an internal diagnosis error occurs:

    • The corresponding LED driver is switched to a retry measurement state

    • All LED drivers of the related diagnosis group will be switched off (System Single Lamp Mode)

  • an external diagnosis error input from DIAG0/1:

    • All LED drivers of the related diagnosis group will be switched off (System Single Lamp Mode)

The LED channel retry measurement state is used to recover LED channels from an error state. In this state the LED channel is switched on for a minimum time.

In the retry measurement state, the fault channel turns on t_{on_min}(minimum-on-time, 50us) after slew rate time.

The diagnosis groups can be configured using DIAGx_CONFIG_x_x.enable values. The detailed logic diagram is shown below.

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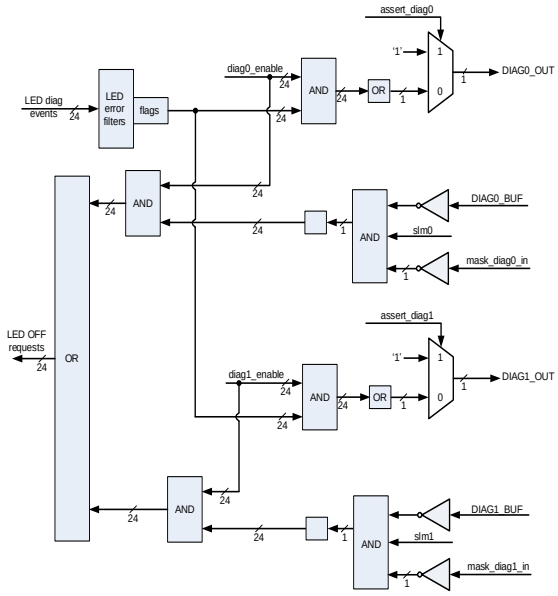

Fig. 5.2.3. Diagnostic Evaluation Structure

5.3 Diagnosis Detection

For the open diagnosis, three different voltage levels can be configured using the LED_OPEN_THR_x values, and assigned to LED channels using the LED_OPEN_SEL_x registers.

For short diagnosis, three different voltage levels can be configured using the LED_SHORT_THR_x values, and assigned to LED channels using the LED_SHORT_SEL_x registers.

An LED short condition is detected if the LEDn supply voltage minus the LEDn pin voltage is below its related LED_SHORT_THR_x level. The short error flag of related channel is set, and the common short error flag is also set in register EVENT_STATUS.

An LED open condition is detected if the LEDn pin voltage is below its related LED_OPEN_THR_x level. The open error flag of related channel is set, and the common open error flag is also set in register EVENT_STATUS. If the error event is LED open, only the flag EVENT_STATUS.led_open is set. If the LEDn pin is shorted to GND, both the EVENT_STATUS.led_open and EVENT_STATUS2.channel_short are set simultaneously, allowing the MCU to determine whether there is an LED open or a channel short error.

The device supply can be monitored by configuring registers VS_TOO_LOW and VS_CRITICAL.

• When VS voltage falls below the VS_TOO_LOW level, an error flag is set in register EVENT_STATUS.

• When VS voltage is larger than the VS_CRITICAL level, an error flag is set in register EVENT_STATUS.

• When VT temperature value is larger than the VT_CRITICAL level, an error flag is set in register EVENT_STATUS.

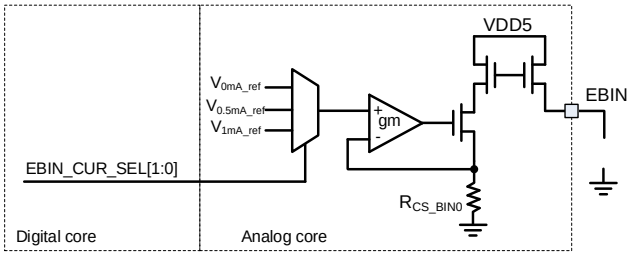

Fig. 5.3.1. EBIN Single Fault Detection

If EBIN is enabled, shorted-to-GND and resistor open errors are monitored for the EBIN pin.

If the ADC measurement of EBIN is less than EBIN_MIN_THR, or higher than EBIN_MAX_THR, an EBIN error is triggered. The gain of the error group is forced to select the minimum valid BIN CLASS level as shown below.

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{BIN_CLASS_GAIN_0, BIN_CLASS_GAIN_1, BIN_CLASS_GAIN_2, BIN_CLASS_GAIN_3, BIN_CLASS_GAIN_4}$_{minimum}$

For example,

BIN_CLASS_GAIN_0=0(disabled),

BIN_CLASS_GAIN_1=0X180(0.75),

BIN_CLASS_GAIN_2=0X200(1.00),

BIN_CLASS_GAIN_3=0X280(1.25)，

BIN_CLASS_GAIN_4=0X300(1.5).

BIN_CLASS_GAIN_1 is the minimum value. If an EBIN error is triggered, the gain of the channels controlled by EBIN are forced to BIN_CLASS_GAIN_1(0.75).

If VTOFS function is enabled, the VTOFS shorted-to-GND error is monitored. If VTOFS is less than 100mV, a VTOFS error is triggered.

Table 5.3.1. Fault events device behavior

Event	Detection Method	Device Init	Active Mode	Effect	Status bit clear
Power-on reset	Analog comparator	-	-	Reset + status bit	Read status register
5V under-voltage	Analog comparator	YES	YES	reset	-
Over-temperature	Analog comparator	YES	YES	reset	-
Communication timeout	Digital signal	NO	YES	DIAG + status bit	Read status register
Active LED current derating	ADC measurement	NO	YES	status bit	Read status register
VS too low	ADC measurement	NO	YES	status bit	Read status register
Critical VS (too high)	ADC measurement	NO	YES	status bit	Read status register
Critical temperature (too high)	ADC measurement	NO	YES	status bit	Read status register
LED short condition	ADC measurement	NO	YES	DIAG + status bit	Read status register
LED open condition	ADC measurement	NO	YES	DIAG + status bit	Read status register
EBIN short/open condition	ADC measurement	NO	YES	status bit	Read status register
VTOFS short condition	ADC measurement	NO	YES	status bit	Read status register
Channel short condition	Analog comparator	NO	YES	status bit	Read status register
BIST error condition	Digital signal	YES	NO	status bit	reset

BUS_CONFIG Area			
register name	register page	address	description
ASSERT_DIAG	-	0X38	DIAG0/1 pin input path mask DIAG0/1 pin forced pull-down
BUS_STATUS area			
RESULT_VDIF_0	-	0X80	ADC result of VS-VLED0
RESULT_VDIF_1	-	0X81	ADC result of VS-VLED1
.....	-	.....	.....
RESULT_VDIF_23	-	0X97	ADC result of VS-VLED23
RESULT_VLED_0	-	0X98	ADC result of LED0 voltage
RESULT_VLED_1	-	0X99	ADC result of LED1 voltage
.....	.....	.....	.....
RESULT_VLED_23	-	0XAF	ADC result of LED23 voltage
RESULT_VT	-	0XB0	ADC result of chip junction temperature
RESULT_VDD5	-	0XB2	ADC result of VDD5 voltage
RESULT_VSUP	-	0XB3	ADC result of VS voltage

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LED_OPEN_0_7	-	0XB4	Led open flag of LED0~7
LED_OPEN_8_15	-	0XB5	Led open flag of LED8~15
LED_OPEN_16_23	-	0XB6	Led open flag of LED16~23
LED_SHORT_0_7	-	0XB7	Led short flag of LED0~7
LED_SHORT_8_15	-	0XB8	Led short flag of LED8~15
LED_SHORT_16_23	-	0XB9	Led short flag of LED16~23
EVENT_STATUS	-	0XBA	Diagnosis event flag. 1). bus_crc_error. 2). led_open. 3). led_short. 4). vt_too_high 5). vs_too_low 6). derating 7). timeout 8). reset 9). vs_too_high
EVENT_STATUS2	-	0XBB	Diagnosis event flag. 1). bist_err 2). vtofs_err 3). channel_short 4). ebin_err
PWMIN_STATUS	-	0XBC	OE pin state ADDR1 pin state ADDR2/PWM state PROG state
DIAG_STATUS	-	0XBD	DIAG0/1 pin state
RESULT_VEBIN	0	0XD8	ADC result of EBIN voltage
Standalone Area			
LED_OPEN_THR_1	2	0XC0	LED open detection threshold 1,46LSB/V (default 0X010)
LED_OPEN_THR_2	2	0XC1	LED open detection threshold 2,46LSB/V
LED_OPEN_THR_3	2	0XC2	LED open detection threshold 3,46LSB/V
LED_OPEN_SEL_0_3	2	0XC3	Select the led open threshold for LED0~3 (default select LED_OPEN_THR_1)
LED_OPEN_SEL_4_7	2	0XC4	Select the led open threshold for LED4~7 (default select LED_OPEN_THR_1)
LED_OPEN_SEL_8_11	2	0XC5	Select the led open threshold for LED8~11 (default select LED_OPEN_THR_1)
LED_OPEN_SEL_12_15	2	0XC6	Select the led open threshold for LED12~15 (default select LED_OPEN_THR_1)
LED_OPEN_SEL_16_19	2	0XC7	Select the led open threshold for LED16~19 (default select LED_OPEN_THR_1)
LED_OPEN_SEL_20_23	2	0XC8	Select the led open threshold for LED20~23 (default select LED_OPEN_THR_1)
LED_SHORT_THR_1	2	0XC9	LED short detection threshold 1,46LSB/V (default 0X05C)
LED_SHORT_THR_2	2	0XCA	LED short detection threshold 2, 46LSB/V
LED_SHORT_THR_3	2	0XCB	LED short detection threshold 3, 46LSB/V
LED_SHORT_SEL_0_3	2	0XCC	Select the led short threshold for LED0~3 (default select LED_SHORT_THR_1)
LED_SHORT_SEL_4_7	2	0XCD	Select the led short threshold for LED4~7 (default select LED_SHORT_THR_1)
LED_SHORT_SEL_8_11	2	0XCE	Select the led short threshold for LED8~11 (default select LED_ SHORT _THR_1)

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LED_SHORT_SEL_12_15	2	0XCF	Select the led short threshold for LED12~15 (default select LED_ SHORT _THR_1)
LED_SHORT_SEL_16_19	2	0XD0	Select the led short threshold for LED16~19 (default select LED_ SHORT _THR_1)
LED_SHORT_SEL_20_23	2	0XD1	Select the led short threshold for LED20~23 (default select LED_ SHORT _THR_1)
VS_TOO_LOW	2	0XD3	The voltage threshold for VS too low detection, 23LSB/V
VS_CRITICAL	2	0XD4	The voltage threshold for VS too high detection, 46LSB/V
VT_CRITICAL	2	0XD5	The temperature threshold for VT detection,1LSB/K
EBIN_MIN_THR	2	0XD6	Set the minimum EBIN voltage,460LSB/V
EBIN_MAX_THR	2	0XD7	Set the maximum EBIN voltage,460LSB/V
DIAG_CONFIG	2	0XD8	Set single lamp or multi-lamp for diagnosis behavior. Set the error filter counter.
DIAG0_CONFIG_0_7	2	0XD9	Enable the DIAG0 for LED0~7
DIAG0_CONFIG_8_15	2	0XDA	Enable the DIAG0 for LED8~15
DIAG0_CONFIG_16_23	2	0XDB	Enable the DIAG0 for LED16~23
DIAG1_CONFIG_0_8	2	0XDC	Enable the DIAG1 for LED0~7
DIAG1_CONFIG_8_15	2	0XDD	Enable the DIAG1 for LED8~15
DIAG1_CONFIG_16_23	2	0XDE	Enable the DIAG1 for LED16~23

6. Start-up

6.1 Device States

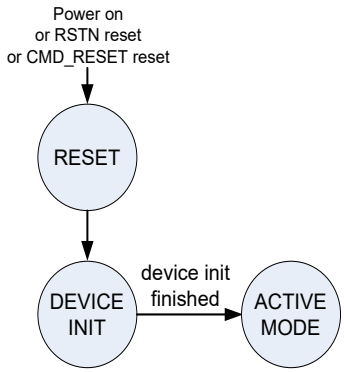

Fig. 6.1.1. Device State Diagram

The device implements the following states as shown in the figure above:

• RESET

• entered when any system reset source is active

• when all reset sources are inactive, system will transition to DEVICE INIT

• DEVICE INIT

• the device configuration register initialization load from MTP

• ADC sampling data area initialization to 0

• internal logic initialization

• when the device initialization has been finished, wait $t_{DEVICE_STARTUP}$ for the power rails to be stable. When delay is completed the device transitions to ACTIVE MODE

• ACTIVE MODE

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• normal operating mode

Standalone area			
register name	**Register page**	**address**	**description**
STARTUP_TIME	3	0XEC	Set the waiting time between DEVICE INIT state and ACTIVE MODE state.

7. Digital IOs Configuration

The reversed polarity of digital pins can be configured by the register IO_CONFIG. These digital pins include OE, ADDR1 and ADDR2/PWM. Descriptions in the previous chapters are based on the default polarity.

As shown below, OE, ADDR1, ADDR2/PWM, DIAG0, DIAG1, RSTN and PROG have default pull-down or pull-up resistor terminations, used to set a known level when these pins are open. The internal pull resistor voltage is limited to approximately V_{DIG_PULL}+0.2V. For this reason, the pull current will saturate when the input voltage is above V_{DIG_PULL}+0.2V.

PIN name	Default state, pull resistor
PROG	Pull-down, 56kΩ
ADDR1, ADDR2/PWM	Pull-down, 110kΩ
DIAG0, DIAG1	Pull-up, 110kΩ
OE	Pull-up, 110kΩ
RSTN	Pull-up, 110kΩ

Standalone area			
register name	**Register page**	**address**	**description**
IO_CONFIG	2	0XFD	Select ADDR1, ADDR2/PWM, OE pin polarity.

8. Registers Access

8.1 BUS Interface Memory Map

The device configuration and the status values can be accessed through the communication BUS interface.

The following table defines the BUS memory address mapping. The base address and area size reflect the internal organization as shown below.

When transferring data via the BUS interface, the bit 0 of memory address will always be 0, so the LSB of memory address will be skipped during communication. Consequently, only 8 address bits need to be transferred to access the complete area of 256 values.

The following table lists the 4 main access areas accessible via the BUS interface.

Table 8.1.1: BUS Base Address Table

Base address	Area size	Name	Type	Description
0x000	0x40	BUS_CONFIG	IMM_UPDATE	Immediate update after registers written.
0x040	0x40	BUS_CONFIG	CMD_UPDATE	Update by command CMD_UPDATE after registers written.
0x80	0x40	BUS_STATUS	Read only	System status and ADC result. These registers are read only.
0XC0	0x40	MAPPING (Page 0, BUS_STATUS)		
	0x40	MAPPING (Page 1)	MTP	Configuration registers load from MTP after device reset or power on.
	0x40	MAPPING	MTP	

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		(Page 2)		
	0x40	MAPPING (Page 3)	MTP	

The addresses are divided into four parts as shown above.

There are three fixed areas BUS_CONFIG area (CMD_UPDATE), BUS_CONFIG area (IMM_UPDATE), and BUS_STATUS area, which are always visible to the bus interface.

Two of these areas BUS_CONFIG area (CMD_UPDATE), BUS_CONFIG area (IMM_UPDATE) map to the same function registers. CMD_UPDATE means that the register data is updated by command after being written. IMM means that the register data is immediately updated after being written. The CMD address equals IMM address plus 0x40.

The BUS_STATUS area contains the registers for ADC result and status.

The fourth part contains four mapping pages. To access a register, the MCU must first select the corresponding page using PAGE_BASE_ADDR. Page 0 is BUS_STATUS area, too. Pages 1 to 3 are the configuration registers whose values are loaded from MTP after device reset or power on.

Below are examples which describe the address translation process.

BUS_DERATE_GAIN is in BUS_CONFIG area. The IMM address of BUS_DERATE_GAIN is 0X035, the corresponding CMD address is 0X075.

VS_CRITICAL is located on the page 2 of the MAPPING area. The BUS interface register address for VS_CRITICAL is 0X0D4. To access VS_CRITICAL, set register PAGE_BASE_ADDR to select page 2 firstly, then will read or write VS_CRITICAL with BUS interface address 0X0D4.

BIN_GAIN_20 is located on page 3 of the MAPPING area. The BUS interface register address for BIN_GAIN_20 is 0X0D4. To access BIN_GAIN_20, set register PAGE_BASE_ADDR to select page 3 firstly, then will read or write BIN_GAIN_20 with BUS interface address 0X0D4.

BUS_CONFIG Area		
CMD_UPDATE	0X3B	Make the CMD registers active.
MTP_UPDATE	0X3C	The access password to program MTP.

9. UART

9.1 UART Transmitter

The UART transmitter generates a differential voltage for communication. The generated voltage levels are compatible with standard CAN bus voltage levels. The bus is high-voltage protected, but does not support voltage levels far below local ground.

Therefore, the minimal voltage driven at BUS_L (VBUS_DRV_L) should be higher than ground to ensure correct communication.

For short-circuit-protection, a current limiter for both lines is implemented.

To minimize radiated EMI, a slew rate limit is implemented. Additionally, the maximum common mode ripple (VBUS_CM_RIPPLE) generated by a single driver will be limited, even when only a single resistor is used for termination.

Optionally, adding a small capacitor between split termination resistors, can help reduce common mode ripple, as shown below:

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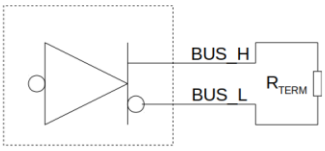

Figure 7.3.1-1: Recommended Bus Termination

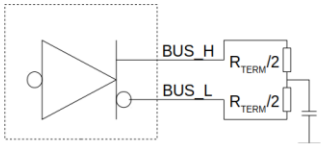

Fig. 9.1.1. Bus Termination with Additional Common Mode Stabilization

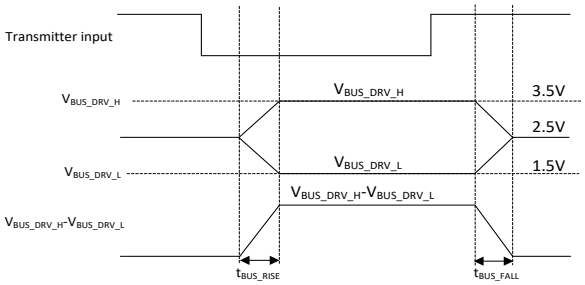

Fig. 9.1.2. Bus Voltage Levels and Timing Diagram

9.2 UART Interface

9.2.1 UART Interface Features

• Data rate of 57600 Bit/s up to 2M Bit/s

• 1 start bit, 8 data bits, 1 or 2 stop bits

• Parity bit (even, odd, zero, none)

• LSB first communication

• Break measurement counter (baud clock based) to detect concurrent break events

• Reset the communication frame after data timeout detected.

9.3 Protocol Frame Header Formats:

9.3.1 Protocol Features:

• CRC used to ensure reliable communication

• Frame-based communication

• Unambiguous communication restart by using a frame start break

• Bus peripheral device auto baud rate updated based on sync-byte

• fixed frame header size

• Peripheral device error response when any header content field is corrupted during transmission

• broadcast access to all bus peripheral devices

9.3.2 Frame Header Formats:

3-byte header format:

• 1 to 31 bus peripheral devices and broadcast access: 5 bits

• 1 to 24 data words (num_words): 4 bits

• 8-bit device internal memory address space: 8 bits

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• read / write: 1 bit

• Hamming Distance 4 CRC: 6 bits (does not contain sync byte)

The frame format figures shown below use the following abbreviations:

• ST: start bit

• PY: parity bit (optional)

• SP: stop bit(s)

• SW: switching between host and peripheral activity

• w: write bit = '1'

• r: read bit = '0'

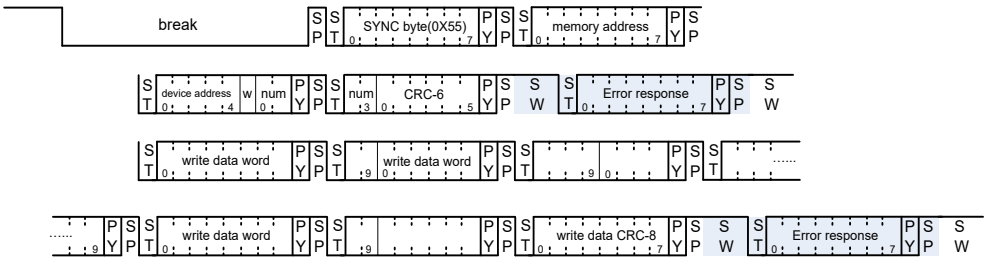

Fig. 9.3.1. Write Frame Format

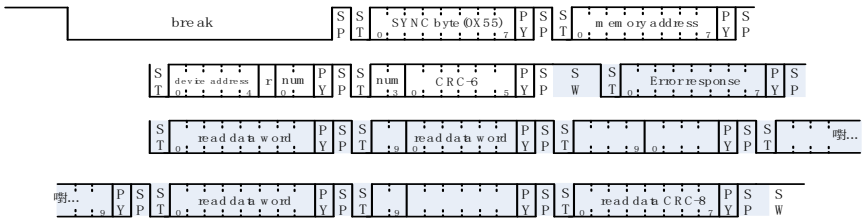

Fig. 9.3.2. Read Frame Format

The following figures show the UART protocol flow of the BUS host and peripheral devices.

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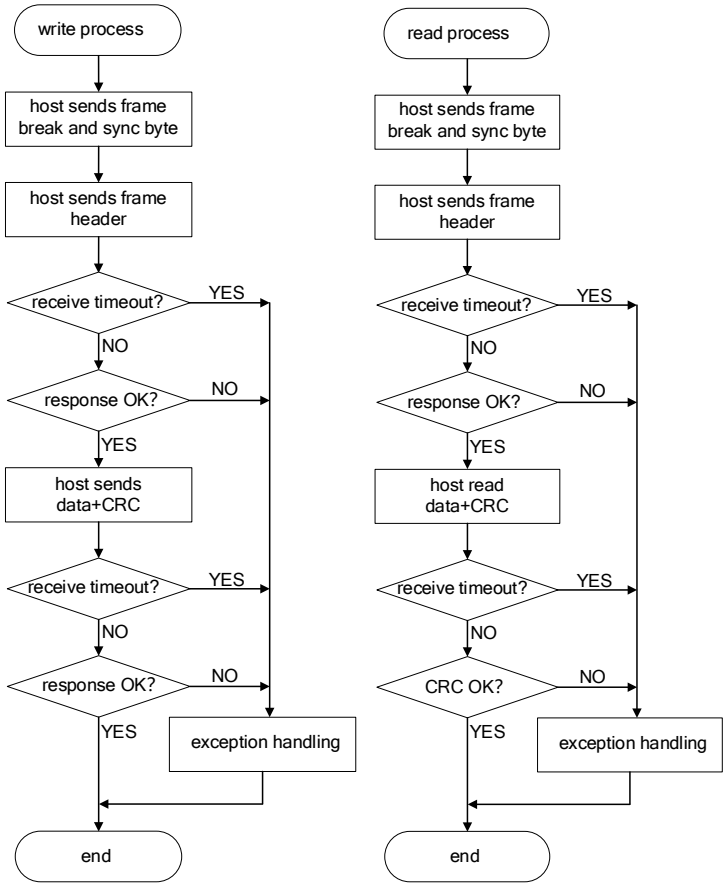

Fig. 9.3.3. BUS Host Write and Read Data Flow

9.3.3 Protocol Handling:

The length of the frame header is constant. When a BUS peripheral device receives a frame header, it checks the header CRC.

If the header CRC is correct and the BUS peripheral device is addressed by the header, whether through a broadcast address or an explicit device address match, the BUS peripheral device will send a frame header OKAY response.

If the header CRC is correct and the BUS peripheral device is not addressed by the header, the BUS peripheral device will not send a response.

If the header CRC is incorrect, regardless of whether the BUS peripheral device is addressed, the BUS peripheral device will send an ERROR response.

If the frame header CRC is correct and the device is addressed, the data part of the frame will be handled. Data is always handled in a 10-bit word format.

In the case of a read frame, the addressed BUS peripheral device sends the requested number of data words in a compact byte format followed by a data CRC byte.

If the number of 10-bit data word stream bits is not a multiple of 8, the peripheral will fill up the last send byte with zero bits before sending the data CRC byte.

In the case of a write frame, an addressed BUS peripheral device receives the given number of data words including an additional data CRC byte.

If the BUS host sends a number of data word stream bits which is not a multiple of 8, the additional bits at the end of the data stream will be ignored by the BUS peripheral device.

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If the write data CRC is correct, the BUS peripheral device will send a data OKAY response and use the received data, otherwise a data ERROR response is sent and the received data is skipped.

In the case of a broadcast write frame, all BUS peripheral devices respond simultaneously. These responses are combined by superposition on the BUS. Mixed OKAY and ERROR responses on the BUS interface result in an ERROR response, because of low level being the dominant level, with higher priority than high level.

9.3.4 Protocol Error Response Bytes:

If the peripheral device receives a string of frames, it will send the ACK signal after the UART_CONFIG.turn_around bit;

The following figure shows the two possible error response bytes generated by a BUS peripheral device.

OKAY response is 0xFC (2 zero-bits). ERROR response is 0xC0 (6 zero-bits).

The host has to evaluate a response byte. Less or equal than 4 zero-bits is considered as an OKAY response, and a response byte with more than 4 zero-bits is considered as an ERROR response.

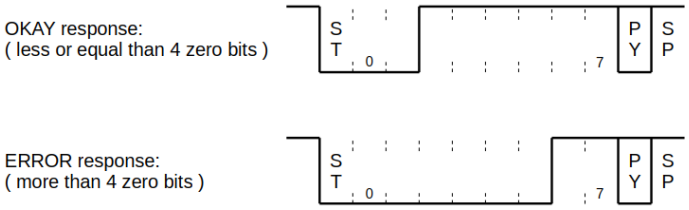

Fig. 9.3.4. Bus Peripheral Error Response

Break:

A Break is a long low-level transmission pulse. The Break pulse must be 15~40t_{bit} low level in a valid data word.

Break Timeout:

A Break longer than 40xt_{Bit} leads to a Break timeout and a Break is not detected.

Data Timeout

If a communication frame is interrupted in the middle without data toggling for a time longer than $t_{data_timeout}$, the device will reset the communication, clear receive cache and wait for next communication frame starting with a break. It is also required for idle time between bytes within $t_{data_timeout}$. $t_{data_timeout}$ is set by configuration register COM_TIMEOUT. It is recommended to use a longer timeout setting for low baud-rate communication to avoid unintended timeouts, and a shorter timeout setting for high baud-rate communication.

SYNC Byte:

The SYNC Byte value is always 0x55.

Broadcast:

Use device address 0x00 to broadcast all BUS peripheral devices.

Universal Device Address:

A peripheral with device address configured to 0x00 can be addressed with any device address.

Number of 10-bit Data Words

The number of 10 bits data words is transmitted in header frame in num_words[3:0].

num_words[3:0]	0	1	2	3	4	5	6
data words (10 bits format)	1	2	3	4	5	6	7

7	8	9	10	11	12	13	14	15

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8	10	12	14	16	18	20	22	24

CRC-Polynomials:

Three different CRC-Polynomials are implemented.

• 6-bit polynomial 0x2C (HD4 for up to 25 bits) for the header.

• 8-bit polynomial 0x97 (HD4 for up to 119 bit) when num_words < 11

• 8-bit polynomial 0xA6 (HD3 for up to 247 bit) when num_words ≥ 11

For the CRC calculations the reverse CRC-polynomials are used.

CRC-Calculation:

All CRC calculations are bytewise and LSB first.

BREAK and SYNC byte are not part of the CRC calculation.

An example of a CRC calculation sequence for a data byte is shown below (C language):

```
// calculate CRC for a data byte
uint8_t calc_crc(uint8_t crc, uint8_t rev_poly, uint8_t byte) {
uint8_t n;
for (n = 0; n < 8; n++) {
      if ((crc ^ byte) & 1) {
            crc = (crc >> 1) ^ rev_poly;
      } else {
            crc = (crc >> 1);
      }
      byte >>= 1;
   }
   return crc;
}
```

For generation of the reverse polynomial, the following sequence is used:

```
// build reverse polynomial
// example:
// polynomial 0xA6 => 1010.0110.1 (including bit 0 which is 1) => 1.0100.1101 = 0x14D
// => reversed 1.0110.0101 = 0x165 => 1011.0010.1 => 0xB2 (LSB skipped)
uint8_t calc_rev_poly(uint8_t poly) {
      uint8_t rev_poly = 1;
      while (poly > 1) {
            rev_poly = (rev_poly << 1) | (poly & 1);
            poly >>= 1;
      }
      return rev_poly;
}
```


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CRC-6 Calculation:

CRC-6 Calculation Sequence:

// use 6 bits polynomial 0x2C (HD4 for up to 25-bit)

// calculate reverse polynomial to 0x2C => 0x26

rev_poly = calc_rev_poly(0x2C)

// initialize crc variable with 0x3F

crc = 0x3F

//calculate crc with byte_1

crc = calc_crc(crc, rev_poly, byte_1)

//calculate crc with byte_2

crc = calc_crc(crc, rev_poly, byte_2)

//calculate crc with the two LSBs of byte_3 (6 MSBs must set to zero)

crc = calc_crc(crc, rev_poly, byte_3 & 0x03)

//concatenate the 6 bits CRC-6 result with the two LSBs of byte_3 to get the 3rd header byte

byte_3_crc = (crc << 2) | (byte_3 & 0x03)

CRC-8 Calculation:

The 8 bits CRC is used for all data word transmissions. The polynomial depends on the length of the transmission.

CRC-8 Calculation Sequence:

//use 8 bits polynomial 0x97 (HD4 for up to 119 bit) when num_words < 11

//calculate reverse polynomial to 0x97 => 0xF4

rev_poly = calc_rev_poly(0x97)

//use 8 bits polynomial 0xA6 (HD3 for up to 247 bit) when num_words ≥ 11

//calculate reverse polynomial to 0xA6 => 0xB2

rev_poly = calc_rev_poly(0xA6)

//initialize crc variable with 0xFF

crc = 0xFF

//calculate crc with byte_1 (first byte)

crc = calc_crc(crc, rev_poly, byte_1)

...

//calculate crc with byte_N (last byte) to get the CRC-8 result

crc = calc_crc(crc, rev_poly, byte_N)

9.4 MTP Programming

9.4.1 Device Address

If no communication device address has been previously programmed to the device STANDALONE area COM_DEV_ADDR value, the BUS interface remains inactive and will not receive or interpret BUS frames. To activate the BUS interface mode for such a device, the PROG pin must be set to an active high level during device startup.

The SA32774 offers two methods for configuring the peripheral addresses. The COM_DEV_ADDR register sets the device peripheral address using either address pin configuration or an internal MTP register code, with each method supporting a maximum of 32 peripheral devices.

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If COM_DEV_ADDR[9] is 0, the register COM_DEV_ADDR[4:0] contains codes to program the peripheral address of the SA32774. In this condition, the ADDR2/PWM pin is used for external PWM inputs to directly control the current output, as described in direct PWM mode.

If COM_DEV_ADDR[9] is set to 1, the device utilizes the register COM_DEV_ADDR[8] in conjunction with external inputs on ADDR2, ADDR1, and ADDR0, as shown in Table 9.4, and ignores the COM_DEV_ADDR[4:0] code. The output current of the ADDR0 pin can be configured using the EBIN_AND_ADDR0_CUR register. Additionally, the voltage on the ADDR0 pin can be sampled to identify different peripheral addresses. The default value of I_{ADDR0} is 0.5 mA.

Table 9.4.1.1. External Device Address Setting

ADDR[3:0]	COM_DEV_ADDR[8]	ADDR2	ADDR1	ADDR0	
				I_{ADDR0}=1mA	I_{ADDR0}=0.5mA(default)
00000B	0	GND	GND	GND	GND
00001B	0	GND	GND	680Ω	1.5kΩ
00010B	0	GND	GND	1.5kΩ	3kΩ
00011B	0	GND	GND	VDD5	VDD5
00100B	0	GND	VDD5	GND	GND
00101B	0	GND	VDD5	680Ω	1.5kΩ
00110B	0	GND	VDD5	1.5kΩ	3kΩ
00111B	0	GND	VDD5	VDD5	VDD5
01000B	0	VDD5	GND	GND	GND
01001B	0	VDD5	GND	680Ω	1.5kΩ
01010B	0	VDD5	GND	1.5kΩ	3kΩ
01011B	0	VDD5	GND	VDD5	VDD5
01100B	0	VDD5	VDD5	GND	GND
01101B	0	VDD5	VDD5	680Ω	1.5kΩ
01110B	0	VDD5	VDD5	1.5kΩ	3kΩ
01111B	0	VDD5	VDD5	VDD5	VDD5
10000B	1	GND	GND	GND	GND
10001B	1	GND	GND	680Ω	1.5kΩ
10010B	1	GND	GND	1.5kΩ	3kΩ
10011B	1	GND	GND	VDD5	VDD5
10100B	1	GND	VDD5	GND	GND
10101B	1	GND	VDD5	680Ω	1.5kΩ
10110B	1	GND	VDD5	1.5kΩ	3kΩ
10111B	1	GND	VDD5	VDD5	VDD5
11000B	1	VDD5	GND	GND	GND
11001B	1	VDD5	GND	680Ω	1.5kΩ
11010B	1	VDD5	GND	1.5kΩ	3kΩ
11011B	1	VDD5	GND	VDD5	VDD5
11100B	1	VDD5	VDD5	GND	GND
11101B	1	VDD5	VDD5	680Ω	1.5kΩ
11110B	1	VDD5	VDD5	1.5kΩ	3kΩ
11111B	1	VDD5	VDD5	VDD5	VDD5

Note: If ADDR[3:0] is configured to 0x00, the IC can be communicated with using any device address. The tolerance range of resistance accuracy should be ±1% for 680Ω, 1.5kΩ(I_{ADDR0}=1mA) or 1.5kΩ, 3kΩ(I_{ADDR0}=0.5mA).

9.4.2 MTP Programming via BUS Interface

The following description is an example of programming the standalone area via the BUS interface:

PROG pin is high active to enable MTP programming.

1. Set the PROG pin to high level.

2. Select the target page by register PAGE_BASE_ADDR.

3. Write the data to the device registers via the BUS interface.

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4. Write the program password to register MTP_UPDATE. The programming process takes 200 ms, and it is essential to ensure that there is no power loss or reset during this period.

5. Read the status register PROG_STATUS to check the busy flag.

6. When the programming busy status changes to non-busy, the PROG_STATUS error flag has to be evaluated.

7. If more data is to be programmed, repeat the above steps.

BUS_CONFIG area			
register name	register page	address	description
PAGE_BASE_ADDR	-	0X39	Mapping page selection
CMD_RESET	-	0X3A	Reset the device
CMD_UPDATE	-	0X3B	Make the CMD registers effective.
BUS_STATUS area			
PROG_STATUS	-	0xBE	Programming status
standalone area			
UART_CONFIG	2	0XDF	UART data format UART data Parity Turn-around time between host device and peripheral device
COM_DEV_ADDR	2	0XE0	Selection for external/internal device address, configure internal device address
COM_TIMEOUT	2	0XE1	BUS Timeout is reflected on DIAG1 or DIAG0 pin or not, BUS Timeout setting Data timeout setting
DEVICE_INFO	2	0XE2	Device version information
FOR_CUSTOMER_USE_0	2	0XE3	User defined
FOR_CUSTOMER_USE_1	2	0XE4	User defined

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10. Appendix 1--Register list

10.1. UART related register

10.1.1 BUS Configuration Area

Table 10.1.1-1: BUS_CONFIG

Register Name	Address	Description
PAGE_BASE_ADDR	0X39	
CMD_RESET	0X3A	
CMD_UPDATE	0X3B	
MTP_UPDATE	0X3C	

Table 10.1.1-2: Register **PAGE_BASE_ADDR** (0X39)

Bit	Name	Default	Access	Description
9:3	-	0	R	
2:0	sel	0	R/W	mapping page selection 000: selects page 0 for access 001: selects page 1 for access 010: selects page 2 for access 011: selects page 3 for access 100. 111: reserved, do not write in application

Table 10.1.1-3: Register **CMD_RESET** (0X3A)

Bit	Name	Default	Access	Description
9:0	cmd	0	R/W	writing the value 0x0259 asserts a device reset Note: if MTP is busy, this command is invalid

Table 10.1.1-4: Register **CMD_UPDATE** (0X3B)

Bit	Name	Default	Access	Description
9:0	cmd	0	R/W	writing the value 0x026A updates the received BUS command area data to the system

Table 10.1.1-5: Register **MTP_UPDATE** (0X3C)

Bit	Name	Default	Access	Description
9:0	mtp	0	R/W	writing the value 0x248 updates register data to MTP

10.1.2 Bus Status Area

Table 10.1.2-1: BUS_STATUS

Register Name	Address	Description
PROG_STATUS	0XBE	MTP programming status

Table 10.1.2-2: Register **PROG_STATUS** (0XBE) MTP programming status

Bit	Name	Default	Access	Description
9:5	-	0	R	
4:2	base_addr_sel	0	R	read-back value of selected mapping area page. This value can be used to be sure that mapping area page base address value set via BUS_CONFIG PAGE_BASE_ADDR is active, because after setting the PAGE_BASE_ADDR.sel value it takes some time to switch to the requested page. Without checking this value until it has the same value as requested, mapping area read requests may read from the previous active (incorrect) mapping area!
1	err	0	R	0: programming successful 1: programming failed
0	busy	0	R	1: programming in progress

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10.1.3 Standalone Area

Table 10.1.3-1: STANDALONE

Register Name	Register page	Address	Description
COM_DEV_ADDR	2	0XE0	communication interface device address value
COM_TIMEOUT	2	0XE1	communication timeout configuration value
DEVICE_INFO	2	0XE2	device version information
FOR_CUSTOMER_USE_0	2	0XE3	reserved for customer specific use
FOR_CUSTOMER_USE_1	2	0XE4	reserved for customer specific use

Table 10.1.3-2: Register **COM_DEV_ADDR** (0XE0, page 2) communication interface device address value

Bit	*Name*	*Default*	*Access*	*Description*
9	addr_sel	1	R/W	Selection for external/internal device address 0: BUS slave device address is configured by internal address. And PWM pin can be used as direct PWM mode. The device address is COM_DEV_ADDR.inter_addr[4:0] 1: BUS slave device address is configured by external pin. The device address is configured by COM_DEV_ADDR.ext_addr and ADDR0~2 pins
8	ext_addr	0	R/W	External device address extension bit.
7:5	-	0	R	
4:0	inter_addr	0X1F	R/W	Internal BUS slave device address address value 0 is used as broadcast address value address values 1 to 31 are used for explicit device access Note: If this register is not configured, a default value of 31 will be used.

Table 10.1.3-3: Register **COM_TIMEOUT** (0XE1, page 2) communication timeout configuration value

Bit	Name	Default	Access	Description
9	diag1_e	0	R/W	0: a BUS communication timeout has no effect on DIAG1 1: a BUS communication timeout asserts DIAG1
8	diag0_e	0	R/W	0: a BUS communication timeout has no effect on DIAG0 1: a BUS communication timeout asserts DIAG0
7:5	data_timeout	000	R/W	$t_{data_timeout}$ configuration 000 = 1ms 001 = 125µs 010 = 250µs 011 = 500µs 100 = 1.25ms 101 = 2.5ms 110 = 5ms 111 = 10ms
4	-	0	R	
3:0	val	0000	R/W	communication interface timeout before the device LEDs in BUS mode change to BUS timeout mode 0000= enters BUS mode and disables the BUS timeout 0001= 200us 0010 = 500µs 0011 = 1ms 0100 = 2ms 0101 = 5ms 0110 = 10ms 0111 = 20ms

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				1000 = 50ms 1001 = 100ms 1010 = 200ms 1011 = 500ms 1100 = 1s; 1101= 0 μs; direct enter BUS timeout mode 1110= 0 μs; direct enter BUS timeout mode 1111= 0 μs; direct enter BUS timeout mode

Table 10.1.3-4: Register **DEVICE_INFO** (0XE2, page 2) device version information

Bit	Name	Default	Access	Description
9:5	ic_version	1	R/W	Silicon version of IC
4:0	fw_version	1	R/W	Firmware version of IC

Table 10.1.3-5: Register **FOR_CUSTOMER_USE_0** (0XE3, page 2) reserved for customer specific use

Bit	Name	Default	Access	Description
9:0	val_customer	0	R/W	

Table 10.1.3-6: Register **FOR_CUSTOMER_USE_1** (0XE4, page 2) reserved for customer specific use

Bit	Name	Default	Access	Description
9:0	val_customer	0	R/W	

10.1.4 Standalone Area

Table 10.1.4-1: STANDALONE

Register Name	Register page	Address	Description
UART_CONFIG	2	0XDF	UART communication configuration

Table 10.1.4-2: Register **UART_CONFIG** (0XDF, page 2) UART communication configuration.

Bit	Name	Default	Access	Description
9:6	-	0	R	
5	stop	0	R/W	stop bit configuration 0: 1 stop bit (default) 1: 2 stop bits
4:3	parity	0	R/W	parity configuration 0: even (default) 1: odd 2: zero (parity bit is always '0') 3: none (no parity bit)
2:0	turn_around	0	R/W	additional turnaround time needed to change transmit direction from host transmit to slave transmit [Tbit] 000：0 Tbit 001：1 Tbit ... 110：6 Tbit 111：7 Tbit

10.2. PWMIN interface related register

10.2.1 Standalone Area

Table 10.2.1-1: STANDALONE

Register Name	Register page	Address	Description
PWMIN_TIMING	1	0XFC	Direct PWM mode time interval

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PWMIN_ENABLE_0_7	1	0XFD	LED channels 0 to 7, PWMIN usage enable value
PWMIN_ENABLE_8_15	1	0XFE	LED channels 8 to 15, PWMIN usage enable value
PWMIN_ENABLE_16_23	1	0XFF	LED channels 16 to 23, PWMIN usage enable value

Table 10.2.1-2: Register **PWMIN_TIMING** (0XFC, page 1) direct PWM mode time interval

Bit	Name	Default	Access	Description
9:5	-	0	R	
4:0	min	0	R/W	valid period min value (t_{PERMOD}) resulting value, t_{PERMOD} = (min + 1) * 256us

Table 10.2.1-3: Register **PWMIN_ENABLE_0_7** (0XFD, page 1) LED channels 0 to 7, PWMIN usage enable value

Bit	Name	Default	Access	Description
9:8	-	0	R	
7	Led7_pwm_e	0	R/W	'0': disable '1': PWM signal usage for LED channel 7 enable
6	Led6_pwm_e	0	R/W	'0': disable '1': PWM signal usage for LED channel 6 enable
5	Led5_pwm_e	0	R/W	'0': disable '1': PWM signal usage for LED channel 5 enable
4	Led4_pwm_e	0	R/W	'0': disable '1': PWM signal usage for LED channel 4 enable
3	Led3_pwm_e	0	R/W	'0': disable '1': PWM signal usage for LED channel 3 enable
2	Led2_pwm_e	0	R/W	'0': disable '1': PWM signal usage for LED channel 2 enable
1	Led1_pwm_e	0	R/W	'0': disable '1': PWM signal usage for LED channel 1 enable
0	led0_pwm_e	0	R/W	'0': disable '1': PWM signal usage for LED channel 0 enable

Table 10.2.1-4: Register **PWMIN_ENABLE_8_15** (0XFE, page 1) LED channels 8 to 15, PWMIN usage enable value

Bit	Name	Default	Access	Description
9:8	-	0	R	
7	Led15_pwm_e	0	R/W	'0': disable '1': PWM signal usage for LED channel 15 enable
6	Led14_pwm_e	0	R/W	'0': disable '1': PWM signal usage for LED channel 14 enable
5	Led13_pwm_e	0	R/W	'0': disable '1': PWM signal usage for LED channel 13 enable
4	Led12_pwm_e	0	R/W	'0': disable '1': PWM signal usage for LED channel 12 enable
3	Led11_pwm_e	0	R/W	'0': disable '1': PWM signal usage for LED channel 11 enable
2	Led10_pwm_e	0	R/W	'0': disable '1': PWM signal usage for LED channel 10 enable
1	Led9_pwm_e	0	R/W	'0': disable '1': PWM signal usage for LED channel 9 enable
0	Led8_pwm_e	0	R/W	'0': disable '1': PWM signal usage for LED channel 8 enable

Table 10.2.1-5: Register **PWMIN_ENABLE_16_23** (0XFF, page 1) LED channels 16 to 23, PWMIN usage enable value

Bit	Name	Default	Access	Description

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9:8	-	0	R	
7	Led23_pwm_e	0	R/W	'0': disable '1': PWM signal usage for LED channel 23 enable
6	Led22_pwm_e	0	R/W	'0': disable '1': PWM signal usage for LED channel 22 enable
5	Led21_pwm_e	0	R/W	'0': disable '1': PWM signal usage for LED channel 21 enable
4	Led20_pwm_e	0	R/W	'0': disable '1': PWM signal usage for LED channel 20 enable
3	Led19_pwm_e	0	R/W	'0': disable '1': PWM signal usage for LED channel 19 enable
2	Led18_pwm_e	0	R/W	'0': disable '1': PWM signal usage for LED channel 18 enable
1	Led17_pwm_e	0	R/W	'0': disable '1': PWM signal usage for LED channel 17 enable
0	Led16_pwm_e	0	R/W	'0': disable '1': PWM signal usage for LED channel 16 enable

10.3. Digital IOs

10.3.1 Standalone Area

Table 10.3.1-1: STANDALONE

Register Name	Register page	Address	Description
IO_CONFIG	2	0XFD	IO configuration value

Table 10.3.1-2: Register **IO_CONFIG** (0XFD, page 2) IO configuration value

Bit	Name	Default	Access	Description
9:4	-	0	R	
3	-	0	R	
2	addr2_pwm	0	R/W	addr2_pwm pin invert selection 0 : not inverted and pull-down 1 : inverted and pull-up
1	addr1	0	R/W	addr1 pin invert selection 0 : not inverted and pull-down 1 : inverted and pull-up
0	oe_inv	0	R/W	OE pin invert selection 0: not inverted and pull-down 1: inverted and pull-up

10.4. PWM generator

10.4.1 BUS Configuration Area

Table 10.4.1-1: BUS_CONFIG

Register Name	Address	Description
BUS_PULSE_0	0X00	LED0 PWM pulse length configuration value
BUS_PULSE_1	0X01	LED1 PWM pulse length configuration value
BUS_PULSE_2	0X02	LED2 PWM pulse length configuration value
BUS_PULSE_3	0X03	LED3 PWM pulse length configuration value
BUS_PULSE_4	0X04	LED4 PWM pulse length configuration value
BUS_PULSE_5	0X05	LED5 PWM pulse length configuration value
BUS_PULSE_6	0X06	LED6 PWM pulse length configuration value
BUS_PULSE_7	0X07	LED7 PWM pulse length configuration value
BUS_PULSE_8	0X08	LED8 PWM pulse length configuration value
BUS_PULSE_9	0X09	LED9 PWM pulse length configuration value
BUS_PULSE_10	0X0A	LED10 PWM pulse length configuration value

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BUS_PULSE_11	0X0B	LED11 PWM pulse length configuration value
BUS_PULSE_12	0X0C	LED12 PWM pulse length configuration value
BUS_PULSE_13	0X0D	LED13 PWM pulse length configuration value
BUS_PULSE_14	0X0E	LED14 PWM pulse length configuration value
BUS_PULSE_15	0X0F	LED15 PWM pulse length configuration value
BUS_PULSE_16	0X10	LED16 PWM pulse length configuration value
BUS_PULSE_17	0X11	LED17 PWM pulse length configuration value
BUS_PULSE_18	0X12	LED18 PWM pulse length configuration value
BUS_PULSE_19	0X13	LED19 PWM pulse length configuration value
BUS_PULSE_20	0X14	LED20 PWM pulse length configuration value
BUS_PULSE_21	0X15	LED21 PWM pulse length configuration value
BUS_PULSE_22	0X16	LED22 PWM pulse length configuration value
BUS_PULSE_23	0X17	LED23 PWM pulse length configuration value
BUS_PULSE_ALL	0X30	all LED channels PWM pulse length configuration command

Table 10.4.1-2: Register **BUS_PULSE_0** (0X00) LED0 PWM pulse length configuration value

Bit	Name	Default	Access	Description
9:0	length	0	R/W	BUS mode PWM channel pulse length [PWM cycles]

Table 10.4.1-3: Register **BUS_PULSE_1** (0X01) LED1 PWM pulse length configuration value

Bit	Name	Default	Access	Description
9:0	length	0	R/W	BUS mode PWM channel pulse length [PWM cycles]

Table 10.4.1-4: Register **BUS_PULSE_2** (0X02) LED2 PWM pulse length configuration value

Bit	Name	Default	Access	Description
9:0	length	0	R/W	BUS mode PWM channel pulse length [PWM cycles]

Table 10.4.1-5: Register **BUS_PULSE_3** (0X03) LED3 PWM pulse length configuration value

Bit	Name	Default	Access	Description
9:0	length	0	R/W	BUS mode PWM channel pulse length [PWM cycles]

Table 10.4.1-6: Register **BUS_PULSE_4** (0X04) LED4 PWM pulse length configuration value

Bit	Name	Default	Access	Description
9:0	length	0	R/W	BUS mode PWM channel pulse length [PWM cycles]

Table 10.4.1-7: Register **BUS_PULSE_5** (0X05) LED5 PWM pulse length configuration value

Bit	Name	Default	Access	Description
9:0	length	0	R/W	BUS mode PWM channel pulse length [PWM cycles]

Table 10.4.1-8: Register **BUS_PULSE_6** (0X06) LED6 PWM pulse length configuration value

Bit	Name	Default	Access	Description
9:0	length	0	R/W	BUS mode PWM channel pulse length [PWM cycles]

Table 10.4.1-9: Register **BUS_PULSE_7** (0X07) LED7 PWM pulse length configuration value

Bit	Name	Default	Access	Description
9:0	length	0	R/W	BUS mode PWM channel pulse length [PWM cycles]

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Table 10.4.1-10: Register **BUS_PULSE_8** (0X08) LED8 PWM pulse length configuration value

Bit	Name	Default	Access	Description
9:0	length	0	R/W	BUS mode PWM channel pulse length [PWM cycles]

Table 10.4.1-11: Register **BUS_PULSE_9** (0X09) LED9 PWM pulse length configuration value

Bit	Name	Default	Access	Description
9:0	length	0	R/W	BUS mode PWM channel pulse length [PWM cycles]

Table 10.4.1-12: Register **BUS_PULSE_10** (0X0A) LED10 PWM pulse length configuration value

Bit	Name	Default	Access	Description
9:0	length	0	R/W	BUS mode PWM channel pulse length [PWM cycles]

Table 10.4.1-13: Register **BUS_PULSE_11** (0X0B) LED11 PWM pulse length configuration value

Bit	Name	Default	Access	Description
9:0	length	0	R/W	BUS mode PWM channel pulse length [PWM cycles]

Table 10.4.1-14: Register **BUS_PULSE_12** (0X0C) LED12 PWM pulse length configuration value

Bit	Name	Default	Access	Description
9:0	length	0	R/W	BUS mode PWM channel pulse length [PWM cycles]

Table 10.4.1-15: Register **BUS_PULSE_13** (0X0D) LED13 PWM pulse length configuration value

Bit	Name	Default	Access	Description
9:0	length	0	R/W	BUS mode PWM channel pulse length [PWM cycles]

Table 10.4.1-16: Register **BUS_PULSE_14** (0X0E) LED14 PWM pulse length configuration value

Bit	Name	Default	Access	Description
9:0	length	0	R/W	BUS mode PWM channel pulse length [PWM cycles]

Table 10.4.1-17: Register **BUS_PULSE_15** (0X0F) LED15 PWM pulse length configuration value

Bit	Name	Default	Access	Description
9:0	length	0	R/W	BUS mode PWM channel pulse length [PWM cycles]

Table 10.4.1-18: Register **BUS_PULSE_16** (0X10) LED15 PWM pulse length configuration value

Bit	Name	Default	Access	Description
9:0	length	0	R/W	BUS mode PWM channel pulse length [PWM cycles]

Table 10.4.1-19: Register **BUS_PULSE_17** (0X11) LED15 PWM pulse length configuration value

Bit	Name	Default	Access	Description
9:0	length	0	R/W	BUS mode PWM channel pulse length [PWM cycles]

Table 10.4.1-20: Register **BUS_PULSE_18** (0X12) LED15 PWM pulse length configuration value

Bit	Name	Default	Access	Description
9:0	length	0	R/W	BUS mode PWM channel pulse length [PWM cycles]

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Table 10.4.1-21: Register **BUS_PULSE_19** (0X13) LED15 PWM pulse length configuration value

Bit	Name	Default	Access	Description
9:0	length	0	R/W	BUS mode PWM channel pulse length [PWM cycles]

Table 10.4.1-22: Register **BUS_PULSE_20** (0X14) LED15 PWM pulse length configuration value

Bit	Name	Default	Access	Description
9:0	length	0	R/W	BUS mode PWM channel pulse length [PWM cycles]

Table 10.4.1-23: Register **BUS_PULSE_21** (0X15) LED15 PWM pulse length configuration value

Bit	Name	Default	Access	Description
9:0	length	0	R/W	BUS mode PWM channel pulse length [PWM cycles]

Table 10.4.1-24: Register **BUS_PULSE_22** (0X16) LED15 PWM pulse length configuration value

Bit	Name	Default	Access	Description
9:0	length	0	R/W	BUS mode PWM channel pulse length [PWM cycles]

Table 10.4.1-25: Register **BUS_PULSE_23** (0X17) LED15 PWM pulse length configuration value

Bit	Name	Default	Access	Description
9:0	length	0	R/W	BUS mode PWM channel pulse length [PWM cycles]

Table 10.4.1-26: Register **BUS_PULSE_ALL** (0X30) all LED channels PWM pulse length configuration command

Bit	Name	Default	Access	Description
9:0	length	0	W	BUS mode PWM channel pulse length for all LED channels [PWM cycles]

10.4.2 Standalone Area

Table 10.4.2-1: STANDALONE

Register Name	Register page	Address	Description
PWM_PRESCALER	1	0XF6	PWM generator prescaler configuration value
PWM_PERIOD	1	0XF7	PWM generator period configuration value
PWM_CONFIG	1	0XF8	PWM generator configuration value
PWM_COMBINE_1	1	0XF9	CH0~CH15 PWM channel combine configuration value
PWM_COMBINE_2	1	0XFA	CH16~CH24 PWM channel combine configuration value
BUST_PULSE_0	1	0XC0	BUS timeout mode LED0 PWM pulse length configuration value
BUST_PULSE_1	1	0XC1	BUS timeout mode LED1 PWM pulse length configuration value
BUST_PULSE_2	1	0XC2	BUS timeout mode LED2 PWM pulse length configuration value
BUST_PULSE_3	1	0XC3	BUS timeout mode LED3 PWM pulse length configuration value
BUST_PULSE_4	1	0XC4	BUS timeout mode LED4 PWM pulse length configuration value
BUST_PULSE_5	1	0XC5	BUS timeout mode LED5 PWM pulse length configuration val
BUST_PULSE_6	1	0XC6	BUS timeout mode LED6 PWM pulse length configuration value
BUST_PULSE_7	1	0XC7	BUS timeout mode LED7 PWM pulse length configuration value

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BUST_PULSE_8	1	0XC8	BUS timeout mode LED8 PWM pulse length configuration value
BUST_PULSE_9	1	0XC9	BUS timeout mode LED9 PWM pulse length configuration value
BUST_PULSE_10	1	0XCA	BUS timeout mode LED10 PWM pulse length configuration value
BUST_PULSE_11	1	0XCB	BUS timeout mode LED11 PWM pulse length configuration value
BUST_PULSE_12	1	0XCC	BUS timeout mode LED12 PWM pulse length configuration value
BUST_PULSE_13	1	0XCD	BUS timeout mode LED13 PWM pulse length configuration value
BUST_PULSE_14	1	0XCE	BUS timeout mode LED14 PWM pulse length configuration value
BUST_PULSE_15	1	0XCF	BUS timeout mode LED15 PWM pulse length configuration value
BUST_PULSE_16	1	0XD0	BUS timeout mode LED16 PWM pulse length configuration value
BUST_PULSE_17	1	0XD1	BUS timeout mode LED17 PWM pulse length configuration value
BUST_PULSE_18	1	0XD2	BUS timeout mode LED18 PWM pulse length configuration value
BUST_PULSE_19	1	0XD3	BUS timeout mode LED19 PWM pulse length configuration value
BUST_PULSE_20	1	0XD4	BUS timeout mode LED20 PWM pulse length configuration value
BUST_PULSE_21	1	0XD5	BUS timeout mode LED21 PWM pulse length configuration value
BUST_PULSE_22	1	0XD6	BUS timeout mode LED22 PWM pulse length configuration value
BUST_PULSE_23	1	0XD7	BUS timeout mode LED23 PWM pulse length configuration value

Table 10.4.2-2: **Register PWM_PRESCALER** (0XF6, page 1) PWM generator prescaler configuration value

Bit	Name	Default	Access	Description
9:7	-	0	R/W	
6:0	div	0X19	R/W	PWM period prescaler This value is used by the PWM prescaler counter to create the PWM period counter increment clock. PWM period frequency = system clock frequency / (PWM_PERIOD.length* (div + 1)) Example: 8MHz / (1023 * (25+1)) = 300.8Hz Note: If this value is not configured, a default value of 25 will be used.

Table 10.4.2-3: Register **PWM_PERIOD** (0XF7, page 1) PWM generator period configuration value

Bit	Name	Default	Access	Description
9:0	length	0X3FF	R/W	PWM period length [PWM cycles] Note: If a value smaller than 1023 is configured, the PWM resolution will be less than 10 bits ! Note: If this value is not configured, a default value of 1023 will be used.

Table 10.4.2-4: Register **PWM_CONFIG** (0XF8, page 1) PWM generator configuration value

Bit	Name	Default	Access	Description
9:3	-	0	R	

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2	oe_mask_bust	0	R/W	Configuration, which selects, if the OE signal masks BUS timeout mode LED channels PWM 0: OE has no influence in BUS timeout mode LED channels 1: OE masks LED channels, which are in BUS timeout mode
1	-	0	R	
0	timing	0	R/W	PWM pulse start timing configuration 0: no PWM inter channel start delay i.e. all channel pulses start at the same time at PWM period start 1: equidistant distribution of PWM channel starting point over PWM period

Table 10.4.2-5: Register **PWM_COMBINE_1** (0XF9, page 1) primary PWM channel combine configuration value

Bit	Name	Default	Access	Description
9:8	-	0	R	
7:0	enable	0	R/W	primary PWM channel combination selection bit 0: combines channels 0 and 1 bit 1: combines channels 2 and 3 ... bit 6: combines channels 12 and 13 bit 7: combines channels 14 and 15 0: the two corresponding channels are independent (PWM_CONFIG defines inter-channel delay) 1: the two corresponding channels are combined (start delay between these channels is forced to 0)

Table 10.4.2-6: Register **PWM_COMBINE_2** (0XFA, page 1) primary PWM channel combine configuration value

Bit	Name	Default	Access	Description
9:4	-	0	R	
3:0	enable	0	R/W	primary PWM channel combination selection bit 0: combines channels 16 and 17 bit 1: combines channels 18 and 19 bit 2: combines channels 20 and 21 bit 3: combines channels 22 and 23 0: the two corresponding channels are independent (PWM_CONFIG defines inter-channel delay) 1: the two corresponding channels are combined (start delay between these channels is forced to 0)

Table 10.4.2-7: Register **BUST_PULSE_0** (0XC0, page 1) BUS timeout mode LED0 PWM pulse length configuration value

Bit	Name	Default	Access	Description
9:0	length	0	R/W	BUS timeout mode PWM channel pulse length [PWM cycles]

Table 10.4.2-8: Register **BUST_PULSE_1** (0XC1, page 1) BUS timeout mode LED1 PWM pulse length configuration value

Bit	Name	Default	Access	Description
9:0	length	0	R/W	BUS timeout mode PWM channel pulse length [PWM cycles]

Table 10.4.2-9: Register **BUST_PULSE_2** (0XC2, page 1) BUS timeout mode LED2 PWM pulse length configuration value

Bit	Name	Default	Access	Description

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9:0	length	0	R/W	BUS timeout mode PWM channel pulse length [PWM cycles]

Table 10.4.2-10: Register **BUST_PULSE_3** (0XC3, page 1) BUS timeout mode LED3 PWM pulse length configuration value

Bit	Name	Default	Access	Description
9:0	length	0	R/W	BUS timeout mode PWM channel pulse length [PWM cycles]

Table 10.4.2-11: Register **BUST_PULSE_4** (0XC4, page 1) BUS timeout mode LED4 PWM pulse length configuration value

Bit	Name	Default	Access	Description
9:0	length	0	R/W	BUS timeout mode PWM channel pulse length [PWM cycles]

Table 10.4.2-12: Register **BUST_PULSE_5** (0XC5, page 1) BUS timeout mode LED5 PWM pulse length configuration value

Bit	Name	Default	Access	Description
9:0	length	0	R/W	BUS timeout mode PWM channel pulse length [PWM cycles]

Table 10.4.2-13: Register **BUST_PULSE_6** (0XC6, page 1) BUS timeout mode LED6 PWM pulse length configuration value

Bit	Name	Default	Access	Description
9:0	length	0	R/W	BUS timeout mode PWM channel pulse length [PWM cycles]

Table 10.4.2-14: Register **BUST_PULSE_7** (0XC7, page 1) BUS timeout mode LED7 PWM pulse length configuration value

Bit	Name	Default	Access	Description
9:0	length	0	R/W	BUS timeout mode PWM channel pulse length [PWM cycles]

Table 10.4.2-15: Register **BUST_PULSE_8** (0XC8, page 1) BUS timeout mode LED8 PWM pulse length configuration value

Bit	Name	Default	Access	Description
9:0	length	0	R/W	BUS timeout mode PWM channel pulse length [PWM cycles]

Table 10.4.2-16: Register **BUST_PULSE_9** (0XC9, page 1) BUS timeout mode LED9 PWM pulse length configuration value

Bit	Name	Default	Access	Description
9:0	length	0	R/W	BUS timeout mode PWM channel pulse length [PWM cycles]

Table 10.4.2-17: Register **BUST_PULSE_10** (0XCA, page 1) BUS timeout mode LED10 PWM pulse length configuration value

Bit	Name	Default	Access	Description
9:0	length	0	R/W	BUS timeout mode PWM channel pulse length [PWM cycles]

Table 10.4.2-18: Register **BUST_PULSE_11** (0XCB, page 1) BUS timeout mode LED11 PWM pulse length configuration value

Bit	Name	Default	Access	Description
9:0	length	0	R/W	BUS timeout mode PWM channel pulse length [PWM cycles]

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Table 10.4.2-19: Register **BUST_PULSE_12** (0XCC, page 1) BUS timeout mode LED12 PWM pulse length configuration value

Bit	Name	Default	Access	Description
9:0	length	0	R/W	BUS timeout mode PWM channel pulse length [PWM cycles]

Table 10.4.2-20: Register **BUST_PULSE_13** (0XCD, page 1) BUS timeout mode LED13 PWM pulse length configuration value

Bit	Name	Default	Access	Description
9:0	length	0	R/W	BUS timeout mode PWM channel pulse length [PWM cycles]

Table 10.4.2-21: Register **BUST_PULSE_14** (0XCE, page 1) BUS timeout mode LED14 PWM pulse length configuration value

Bit	Name	Default	Access	Description
9:0	length	0	R/W	BUS timeout mode PWM channel pulse length [PWM cycles]

Table 10.4.2-22: Register **BUST_PULSE_15** (0XCF, page 1) BUS timeout mode LED15 PWM pulse length configuration value

Bit	Name	Default	Access	Description
9:0	length	0	R/W	BUS timeout mode PWM channel pulse length [PWM cycles]

Table 10.4.2-23: Register **BUST_PULSE_16** (0XD0, page 1) BUS timeout mode LED15 PWM pulse length configuration value

Bit	Name	Default	Access	Description
9:0	length	0	R/W	BUS timeout mode PWM channel pulse length [PWM cycles]

Table 10.4.2-24: Register **BUST_PULSE_17** (0XD1, page 1) BUS timeout mode LED15 PWM pulse length configuration value

Bit	Name	Default	Access	Description
9:0	length	0	R/W	BUS timeout mode PWM channel pulse length [PWM cycles]

Table 10.4.2-25: Register **BUST_PULSE_18** (0XD2, page 1) BUS timeout mode LED15 PWM pulse length configuration value

Bit	Name	Default	Access	Description
9:0	length	0	R/W	BUS timeout mode PWM channel pulse length [PWM cycles]

Table 10.4.2-26: Register **BUST_PULSE_19** (0XD3, page 1) BUS timeout mode LED15 PWM pulse length configuration value

Bit	Name	Default	Access	Description
9:0	length	0	R/W	BUS timeout mode PWM channel pulse length [PWM cycles]

Table 10.4.2-27: Register **BUST_PULSE_20** (0XD4, page 1) BUS timeout mode LED15 PWM pulse length configuration value

Bit	Name	Default	Access	Description
9:0	length	0	R/W	BUS timeout mode PWM channel pulse length [PWM cycles]

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Table 10.4.2-28: Register **BUST_PULSE_21** (0XD5, page 1) BUS timeout mode LED15 PWM pulse length configuration value

Bit	Name	Default	Access	Description
9:0	length	0	R/W	BUS timeout mode PWM channel pulse length [PWM cycles]

Table 10.4.2-29: Register **BUST_PULSE_22** (0XD6, page 1) BUS timeout mode LED15 PWM pulse length configuration value

Bit	Name	Default	Access	Description
9:0	length	0	R/W	BUS timeout mode PWM channel pulse length [PWM cycles]

Table 10.4.2-30: Register **BUST_PULSE_23** (0XD7, page 1) BUS timeout mode LED15 PWM pulse length configuration value

Bit	Name	Default	Access	Description
9:0	length	0	R/W	BUS timeout mode PWM channel pulse length [PWM cycles]

10.5. Current sinks

10.5.1 Bus Configuration Area

Table 10.5.1-1: BUS_CONFIG

Register Name	Address	Description
BUS_CURRENT_0	0X18	bus mode LED0 sink current configuration value
BUS_CURRENT_1	0X19	bus mode LED1 sink current configuration value
BUS_CURRENT_2	0X1A	bus mode LED2 sink current configuration value
BUS_CURRENT_3	0X1B	bus mode LED3 sink current configuration value
BUS_CURRENT_4	0X1C	bus mode LED4 sink current configuration value
BUS_CURRENT_5	0X1D	bus mode LED5 sink current configuration value
BUS_CURRENT_6	0X1E	bus mode LED6 sink current configuration value
BUS_CURRENT_7	0X1F	bus mode LED7 sink current configuration value
BUS_CURRENT_8	0X20	bus mode LED8 sink current configuration value
BUS_CURRENT_9	0X21	bus mode LED9 sink current configuration value
BUS_CURRENT_10	0X22	bus mode LED10 sink current configuration value
BUS_CURRENT_11	0X23	bus mode LED11 sink current configuration value
BUS_CURRENT_12	0X24	bus mode LED12 sink current configuration value
BUS_CURRENT_13	0X25	bus mode LED13 sink current configuration value
BUS_CURRENT_14	0X26	bus mode LED14 sink current configuration value
BUS_CURRENT_15	0X27	bus mode LED15 sink current configuration value
BUS_CURRENT_16	0X28	bus mode LED16 sink current configuration value
BUS_CURRENT_17	0X29	bus mode LED17 sink current configuration value
BUS_CURRENT_18	0X2A	bus mode LED18 sink current configuration value
BUS_CURRENT_19	0X2B	bus mode LED19 sink current configuration value
BUS_CURRENT_20	0X2C	bus mode LED20 sink current configuration value
BUS_CURRENT_21	0X2D	bus mode LED21 sink current configuration value
BUS_CURRENT_22	0X2E	bus mode LED22 sink current configuration value
BUS_CURRENT_23	0X2F	bus mode LED23 sink current configuration value
LED_ENABLE_0_7	0X31	LED driver channels 0 to 7 enable value in BUS mode
LED_ENABLE_8_15	0X32	LED driver channels 8 to 15 enable value in BUS mode
LED_ENABLE_16_23	0X33	LED driver channels 16 to 23 enable value in BUS mode
BUS_DERATE_GAIN	0X35	bus based derating value
BUS_CURRENT_ALL	0X31	all LED channels current configuration command

Table 10.5.1-2: Register **BUS_CURRENT_0** (0X18) bus mode LED0 sink current configuration value

Bit	Name	Default	Access	Description

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9:0	sel	0	R/W	Bus mode driver channel current selection driver current [100uA] The driver current will be limited to the related IDAC selected range maximum current.

Table 10.5.1-3: Register **BUS_CURRENT_1** (0X19) bus mode LED1 sink current configuration value

Bit	Name	Default	Access	Description
9:0	sel	0	R/W	Bus mode driver channel current selection driver current [100uA] The driver current will be limited to the related IDAC selected range maximum current.

Table 10.5.1-4: Register **BUS_CURRENT_2** (0X1A) bus mode LED2 sink current configuration value

Bit	Name	Default	Access	Description
9:0	sel	0	R/W	Bus mode driver channel current selection driver current [100uA] The driver current will be limited to the related IDAC selected range maximum current.

Table 10.5.1-5: Register **BUS_CURRENT_3** (0X1B) bus mode LED3 sink current configuration value

Bit	Name	Default	Access	Description
9:0	sel	0	R/W	Bus mode driver channel current selection driver current [100uA] The driver current will be limited to the related IDAC selected range maximum current.

Table 10.5.1-6: Register **BUS_CURRENT_4** (0X1C) bus mode LED4 sink current configuration value

Bit	Name	Default	Access	Description
9:0	sel	0	R/W	Bus mode driver channel current selection driver current [100uA] The driver current will be limited to the related IDAC selected range maximum current.

Table 10.5.1-7: Register **BUS_CURRENT_5** (0X1D) bus mode LED5 sink current configuration value

Bit	Name	Default	Access	Description
9:0	sel	0	R/W	Bus mode driver channel current selection driver current [100uA] The driver current will be limited to the related IDAC selected range maximum current.

Table 10.5.1-8: Register **BUS_CURRENT_6** (0X1E) bus mode LED6 sink current configuration value

Bit	Name	Default	Access	Description
9:0	sel	0	R/W	Bus mode driver channel current selection driver current [100uA] The driver current will be limited to the related IDAC selected range maximum current.

Table 10.5.1-9: Register **BUS_CURRENT_7** (0X1F) bus mode LED7 sink current configuration value

Bit	Name	Default	Access	Description
9:0	sel	0	R/W	Bus mode driver channel current selection driver current [100uA] The driver current will be limited to the related IDAC selected range maximum current.

Table 10.5.1-10: Register **BUS_CURRENT_8** (0X20) bus mode LED8 sink current configuration value

Bit	Name	Default	Access	Description

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9:0	sel	0	R/W	Bus mode driver channel current selection driver current [100uA] The driver current will be limited to the related IDAC selected range maximum current.

Table 10.5.1-11: Register **BUS_CURRENT_9** (0X21) bus mode LED9 sink current configuration value

Bit	Name	Default	Access	Description
9:0	sel	0	R/W	Bus mode driver channel current selection driver current [100uA] The driver current will be limited to the related IDAC selected range maximum current.

Table 10.5.1-12: Register **BUS_CURRENT_10** (0X22) bus mode LED10 sink current configuration value

Bit	Name	Default	Access	Description
9:0	sel	0	R/W	Bus mode driver channel current selection driver current [100uA] The driver current will be limited to the related IDAC selected range maximum current.

Table 10.5.1-13: Register **BUS_CURRENT_11** (0X23) bus mode LED11 sink current configuration value

Bit	Name	Default	Access	Description
9:0	sel	0	R/W	Bus mode driver channel current selection driver current [100uA] The driver current will be limited to the related IDAC selected range maximum current.

Table 10.5.1-14: Register **BUS_CURRENT_12** (0X24) bus mode LED12 sink current configuration value

Bit	Name	Default	Access	Description
9:0	sel	0	R/W	Bus mode driver channel current selection driver current [100uA] The driver current will be limited to the related IDAC selected range maximum current.

Table 10.5.1-15: Register **BUS_CURRENT_13** (0X25) bus mode LED13 sink current configuration value

Bit	Name	Default	Access	Description
9:0	sel	0	R/W	Bus mode driver channel current selection driver current [100uA] The driver current will be limited to the related IDAC selected range maximum current.

Table 10.5.1-16: Register **BUS_CURRENT_14** (0X26) bus mode LED14 sink current configuration value

Bit	Name	Default	Access	Description
9:0	sel	0	R/W	Bus mode driver channel current selection driver current [100uA] The driver current will be limited to the related IDAC selected range maximum current.

Table 10.5.1-17: Register **BUS_CURRENT_15** (0X27) bus mode LED15 sink current configuration value

Bit	Name	Default	Access	Description
9:0	sel	0	R/W	Bus mode driver channel current selection driver current [100uA] The driver current will be limited to the related IDAC selected range maximum current.

Table 10.5.1-18: Register **BUS_CURRENT_16** (0X28) bus mode LED16 sink current configuration value

Bit	Name	Default	Access	Description

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9:0	sel	0	R/W	Bus mode driver channel current selection driver current [100uA] The driver current will be limited to the related IDAC selected range maximum current.

Table 10.5.1-19: Register **BUS_CURRENT_17** (0X29) bus mode LED17 sink current configuration value

Bit	Name	Default	Access	Description
9:0	sel	0	R/W	Bus mode driver channel current selection driver current [100uA] The driver current will be limited to the related IDAC selected range maximum current.

Table 10.5.1-20: Register **BUS_CURRENT_18** (0X2A) bus mode LED18 sink current configuration value

Bit	Name	Default	Access	Description
9:0	sel	0	R/W	Bus mode driver channel current selection driver current [100uA] The driver current will be limited to the related IDAC selected range maximum current.

Table 10.5.1-21: Register **BUS_CURRENT_19** (0X2B) bus mode LED19 sink current configuration value

Bit	Name	Default	Access	Description
9:0	sel	0	R/W	Bus mode driver channel current selection driver current [100uA] The driver current will be limited to the related IDAC selected range maximum current.

Table 10.5.1-22: Register **BUS_CURRENT_20** (0X2C) bus mode LED20 sink current configuration value

Bit	Name	Default	Access	Description
9:0	sel	0	R/W	Bus mode driver channel current selection driver current [100uA] The driver current will be limited to the related IDAC selected range maximum current.

Table 10.5.1-23: Register **BUS_CURRENT_21** (0X2D) bus mode LED21 sink current configuration value

Bit	Name	Default	Access	Description
9:0	sel	0	R/W	Bus mode driver channel current selection driver current [100uA] The driver current will be limited to the related IDAC selected range maximum current.

Table 10.5.1-24: Register **BUS_CURRENT_22** (0X2E) bus mode LED22 sink current configuration value

Bit	Name	Default	Access	Description
9:0	sel	0	R/W	Bus mode driver channel current selection driver current [100uA] The driver current will be limited to the related IDAC selected range maximum current.

Table 10.5.1-25: Register **BUS_CURRENT_23** (0X2F) bus mode LED23 sink current configuration value

Bit	Name	Default	Access	Description
9:0	sel	0	R/W	Bus mode driver channel current selection driver current [100uA] The driver current will be limited to the related IDAC selected range maximum current.

Table 10.5.1-26: Register **LED_ENABLE_0_7** (0X32) LED driver channels 0 to 7 enable value in BUS mode

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Bit	Name	Default	Access	Description
9:8	-	0	R	
7:0	enable	0	R/W	Enable for driver channels 0 to 7 in BUS mode bit 0: enable for driver channel 0 ... bit 7: enable for driver channel 7 a value of 0 disables the analog section of the channel driver a value of 1 enables the analog section of the channel driver Note: Used to save current when channel drivers are OFF.

Table 10.5.1-27: Register **LED_ENABLE_8_15** (0X33) LED driver channels 8 to 15 enable value in BUS mode

Bit	Name	Default	Access	Description
9:8	-	0	R	
7:0	enable	0	R/W	Enable for driver channels 8 to 15 in BUS mode bit 0: enable for driver channel 8 ... bit 7: enable for driver channel 15 an enable bit value of 0 disables channel driver analog part an enable bit value of 1 enables channel driver analog part Note: Used to save current when channel drivers are OFF.

Table 10.5.1-28: Register **LED_ENABLE_16_23** (0X34) LED driver channels 16 to 23 enable value in BUS mode

Bit	Name	Default	Access	Description
9:8	-	0	R	
7:0	enable	0	R/W	Enable for driver channels 16 to 23 in BUS mode bit 0: enable for driver channel 16 ... bit 7: enable for driver channel 23 an enable bit value of 0 disables channel driver analog part an enable bit value of 1 enables channel driver analog part Note: Used to save current when channel drivers are OFF.

Table 10.5.1-29: Register **BUS_DERATE_GAIN** (0X35) bus based derating value

Bit	Name	Default	Access	Description
9:8	-	0	R	
7:0	gain	0	R/W	defines reduction of nominal LED current by a value settable via bus communication (derating by host controller) derating multiplier: $M_{BUS_derate} = 1 - (gain / 256)$

Table 10.5.1-30: Register **BUS_CURRENT_ALL** (0X31) all LED channels current configuration command

Bit	Name	Default	Access	Description
9:0	sel	0	W	Bus mode driver channel current selection for all LED channels driver current [100uA] The driver current will be limited to the channel related IDAC selected range maximum current.

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10.5.2 Standalone Area

Table 10.5.2-1: STANDALONE

Register Name	Register page	Address	Description
BIN_GAIN_0	3	0XC0	LED0 bin class adoption gain configuration value
BIN_GAIN_1	3	0XC1	LED1 bin class adoption gain configuration value
BIN_GAIN_2	3	0XC2	LED2 bin class adoption gain configuration value
BIN_GAIN_3	3	0XC3	LED3 bin class adoption gain configuration value
BIN_GAIN_4	3	0XC4	LED4 bin class adoption gain configuration value
BIN_GAIN_5	3	0XC5	LED5 bin class adoption gain configuration value
BIN_GAIN_6	3	0XC6	LED6 bin class adoption gain configuration value
BIN_GAIN_7	3	0XC7	LED7 bin class adoption gain configuration value
BIN_GAIN_8	3	0XC8	LED8 bin class adoption gain configuration value
BIN_GAIN_9	3	0XC9	LED9 bin class adoption gain configuration value
BIN_GAIN_10	3	0XCA	LED10 bin class adoption gain configuration value
BIN_GAIN_11	3	0XCB	LED11 bin class adoption gain configuration value
BIN_GAIN_12	3	0XCC	LED12 bin class adoption gain configuration value
BIN_GAIN_13	3	0XCD	LED13 bin class adoption gain configuration value
BIN_GAIN_14	3	0XCE	LED14 bin class adoption gain configuration value
BIN_GAIN_15	3	0XCF	LED15 bin class adoption gain configuration value
BIN_GAIN_16	3	0XD0	LED16 bin class adoption gain configuration value
BIN_GAIN_17	3	0XD1	LED17 bin class adoption gain configuration value
BIN_GAIN_18	3	0XD2	LED18 bin class adoption gain configuration value
BIN_GAIN_19	3	0XD3	LED19 bin class adoption gain configuration value
BIN_GAIN_20	3	0XD4	LED20 bin class adoption gain configuration value
BIN_GAIN_21	3	0XD5	LED21 bin class adoption gain configuration value
BIN_GAIN_22	3	0XD6	LED22 bin class adoption gain configuration value
BIN_GAIN_23	3	0XD7	LED23 bin class adoption gain configuration value
EBIN_AND_ADDR0_CUR	3	0XD8	configure EBIN or ADDR0 pin source current
EBIN_CLASS_ENABLE_0_7	3	0XD9	evaluated LED0~7 bin class assignment configuration value
EBIN_CLASS_ENABLE_8_15	3	0XDA	evaluated LED8~15 bin class assignment configuration value

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EBIN_CLASS_ENABLE_16_23	3	0XDB	evaluated LED16~23 bin class assignment configuration value
BIN_CLASS_LEVEL_0	3	0XDF	LED bin class evaluation level value
BIN_CLASS_LEVEL_1	3	0XE0	LED bin class evaluation level value
BIN_CLASS_LEVEL_2	3	0XE1	LED bin class evaluation level value
BIN_CLASS_LEVEL_3	3	0XE2	LED bin class evaluation level value
BIN_CLASS_GAIN_0	3	0XE3	evaluated LED bin class 0 gain value
BIN_CLASS_GAIN_1	3	0XE4	evaluated LED bin class 1 gain value
BIN_CLASS_GAIN_2	3	0XE5	evaluated LED bin class 2 gain value
BIN_CLASS_GAIN_3	3	0XE6	evaluated LED bin class 3 gain value
BIN_CLASS_GAIN_4	3	0XE7	evaluated LED bin class 4 gain value
BUST_CURRENT_0	1	0XD8	BUS timeout mode LED0 sink current configuration value
BUST_CURRENT_1	1	0XD9	BUS timeout mode LED1 sink current configuration value
BUST_CURRENT_2	1	0XDA	BUS timeout mode LED2 sink current configuration value
BUST_CURRENT_3	1	0XDB	BUS timeout mode LED3 sink current configuration value
BUST_CURRENT_4	1	0XDC	BUS timeout mode LED4 sink current configuration value
BUST_CURRENT_5	1	0XDD	BUS timeout mode LED5 sink current configuration value
BUST_CURRENT_6	1	0XDE	BUS timeout mode LED6 sink current configuration value
BUST_CURRENT_7	1	0XDF	BUS timeout mode LED7 sink current configuration value
BUST_CURRENT_8	1	0XE0	BUS timeout mode LED8 sink current configuration value
BUST_CURRENT_9	1	0XE1	BUS timeout mode LED9 sink current configuration value
BUST_CURRENT_10	1	0XE2	BUS timeout mode LED10 sink current configuration value
BUST_CURRENT_11	1	0XE3	BUS timeout mode LED11 sink current configuration value
BUST_CURRENT_12	1	0XE4	BUS timeout mode LED12 sink current configuration value
BUST_CURRENT_13	1	0XE5	BUS timeout mode LED13 sink current configuration value
BUST_CURRENT_14	1	0XE6	BUS timeout mode LED14 sink current configuration value
BUST_CURRENT_15	1	0XE7	BUS timeout mode LED15 sink current configuration value
BUST_CURRENT_16	1	0XE8	BUS timeout mode LED16 sink current configuration value
BUST_CURRENT_17	1	0XE9	BUS timeout mode LED17 sink current configuration value
BUST_CURRENT_18	1	0XEA	BUS timeout mode LED18 sink current configuration value
BUST_CURRENT_19	1	0XEB	BUS timeout mode LED19 sink current configuration value
BUST_CURRENT_20	1	0XEC	BUS timeout mode LED20 sink current configuration value
BUST_CURRENT_21	1	0XED	BUS timeout mode LED21 sink current configuration value

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BUST_CURRENT_22	1	0XEE	BUS timeout mode LED22 sink current configuration value
BUST_CURRENT_23	1	0XEF	BUS timeout mode LED23 sink current configuration value
EXPWM_CURRENT_0	2	0XE5	Direct PWM mode LED0 sink current configuration value
EXPWM_CURRENT_1	2	0XE6	Direct PWM mode LED1 sink current configuration value
EXPWM_CURRENT_2	2	0XE7	Direct PWM mode LED2 sink current configuration value
EXPWM_CURRENT_3	2	0XE8	Direct PWM mode LED3 sink current configuration value
EXPWM_CURRENT_4	2	0XE9	Direct PWM mode LED4 sink current configuration value
EXPWM_CURRENT_5	2	0XEA	Direct PWM mode LED5 sink current configuration value
EXPWM_CURRENT_6	2	0XEB	Direct PWM mode LED6 sink current configuration value
EXPWM_CURRENT_7	2	0XEC	Direct PWM mode LED7 sink current configuration value
EXPWM_CURRENT_8	2	0XED	Direct PWM mode LED8 sink current configuration value
EXPWM_CURRENT_9	2	0XEE	Direct PWM mode LED9 sink current configuration value
EXPWM_CURRENT_10	2	0XEF	Direct PWM mode LED10 sink current configuration value
EXPWM_CURRENT_11	2	0XF0	Direct PWM mode LED11 sink current configuration value
EXPWM_CURRENT_12	2	0XF1	Direct PWM mode LED12 sink current configuration value
EXPWM_CURRENT_13	2	0XF2	Direct PWM mode LED13 sink current configuration value
EXPWM_CURRENT_14	2	0XF3	Direct PWM mode LED14 sink current configuration value
EXPWM_CURRENT_15	2	0XF4	Direct PWM mode LED15 sink current configuration value
EXPWM_CURRENT_16	2	0XF5	Direct PWM mode LED16 sink current configuration value
EXPWM_CURRENT_17	2	0XF6	Direct PWM mode LED17 sink current configuration value
EXPWM_CURRENT_18	2	0XF7	Direct PWM mode LED18 sink current configuration value
EXPWM_CURRENT_19	2	0XF8	Direct PWM mode LED19 sink current configuration value
EXPWM_CURRENT_20	2	0XF9	Direct PWM mode LED20 sink current configuration value
EXPWM_CURRENT_21	2	0XFA	Direct PWM mode LED21 sink current configuration value
EXPWM_CURRENT_22	2	0XFB	Direct PWM mode LED22 sink current configuration value
EXPWM_CURRENT_23	2	0XFC	Direct PWM mode LED23 sink current configuration value
LED_ENABLE2_0_7	1	0XF0	LED driver channels 0 to 7 enable value in BUS timeout /direct PWM mode
LED_ENABLE2_8_15	1	0XF1	LED driver channels 8 to 15 enable value in BUS timeout direct PWM mode

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LED_ENABLE2_16_23	1	0XF2	LED driver channels 16 to 23 enable value in BUS timeout /direct PWM mode
IDAC_REF_SEL_0_7	1	0XF3	LED channels 0 to 7 IDAC reference selection value
IDAC_REF_SEL_8_15	1	0XF4	LED channels 8 to 15 IDAC reference selection value
IDAC_REF_SEL_16_23	1	0XF5	LED channels 16 to 23 IDAC reference selection value
ISINK_CONFIG	1	0XFB	LED current slew rate configuration value
VT_OFFSET_TSTART	2	0XFE	device temperature to start led drop voltage compensation during high temperature
VT_OFFSET_TSTOP	2	0XFF	device temperature to stop led drop voltage compensation during high temperature
VS_DERATE_RANGE	3	0XE8	LED supply derating range configuration value
VT_DERATE_START	3	0XE9	device temperature based derating starts configuration value
VT_DERATE_STOP	3	0XEA	device temperature based derating stops configuration value
DERATE_GAIN	3	0XEB	derating gain configuration value
STARTUP_TIME	3	0XEC	time delay to wait for stable power supply rails.

Table 10.5.2-2: Register **BIN_GAIN_0** (0XC0, page 3) LED0 bin class adoption gain configuration value

Bit	Name	Default	Access	Description
9:0	gain	0X200	R/W	LED channel binning gain gain 0.50 = 0x100 gain 1.00 = 0x200 gain 1.99 = 0x3FF Note: Gain will be applied with saturation. Note: If this value is not configured, a default value of 0x200 will be used.

Table 10.5.2-3: Register **BIN_GAIN_1** (0XC1, page 3) LED1 bin class adoption gain configuration value

Bit	Name	Default	Access	Description
9:0	gain	0X200	R/W	LED channel binning gain gain 0.50 = 0x100 gain 1.00 = 0x200 gain 1.99 = 0x3FF Note: Gain will be applied with saturation. Note: If this value is not configured, a default value of 0x200 will be used.

Table 10.5.2-4: Register **BIN_GAIN_2** (0XC2, page 3) LED2 bin class adoption gain configuration value

Bit	Name	Default	Access	Description
9:0	gain	0X200	R/W	LED channel binning gain gain 0.50 = 0x100 gain 1.00 = 0x200 gain 1.99 = 0x3FF Note: Gain will be applied with saturation. Note: If this value is not configured, a default value of 0x200 will be used.

Table 10.5.2-5: Register **BIN_GAIN_3** (0XC3, page 3) LED3 bin class adoption gain configuration value

Bit	Name	Default	Access	Description
9:0	gain	0X200	R/W	LED channel binning gain gain 0.50 = 0x100

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				gain 1.00 = 0x200 gain 1.99 = 0x3FF Note: Gain will be applied with saturation. Note: If this value is not configured, a default value of 0x200 will be used.

Table 10.5.2-6: Register **BIN_GAIN_4** (0XC4, page 3) LED4 bin class adoption gain configuration value

Bit	Name	Default	Access	Description
9:0	gain	0X200	R/W	LED channel binning gain gain 0.50 = 0x100 gain 1.00 = 0x200 gain 1.99 = 0x3FF Note: Gain will be applied with saturation. Note: If this value is not configured, a default value of 0x200 will be used.

Table 10.5.2-7: Register **BIN_GAIN_5** (0XC5, page 3) LED5 bin class adoption gain configuration value

Bit	Name	Default	Access	Description
9:0	gain	0X200	R/W	LED channel binning gain gain 0.50 = 0x100 gain 1.00 = 0x200 gain 1.99 = 0x3FF Note: Gain will be applied with saturation. Note: If this value is not configured, a default value of 0x200 will be used.

Table 10.5.2-8: Register **BIN_GAIN_6** (0XC6, page 3) LED6 bin class adoption gain configuration value

Bit	Name	Default	Access	Description
9:0	gain	0X200	R/W	LED channel binning gain gain 0.50 = 0x100 gain 1.00 = 0x200 gain 1.99 = 0x3FF Note: Gain will be applied with saturation. Note: If this value is not configured, a default value of 0x200 will be used.

Table 10.5.2-9: Register **BIN_GAIN_7** (0XC7, page 3) LED7 bin class adoption gain configuration value

Bit	Name	Default	Access	Description
9:0	gain	0X200	R/W	LED channel binning gain gain 0.50 = 0x100 gain 1.00 = 0x200 gain 1.99 = 0x3FF Note: Gain will be applied with saturation. Note: If this value is not configured, a default value of 0x200 will be used.

Table 10.5.2-10: Register **BIN_GAIN_8** (0XC8, page 3) LED8 bin class adoption gain configuration value

Bit	Name	Default	Access	Description
9:0	gain	0X200	R/W	LED channel binning gain gain 0.50 = 0x100 gain 1.00 = 0x200 gain 1.99 = 0x3FF Note: Gain will be applied with saturation. Note: If this value is not configured, a default value of 0x200 will be used.

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Table 10.5.2-11: Register **BIN_GAIN_9** (0XC9, page 3) LED9 bin class adoption gain configuration value

Bit	Name	Default	Access	Description
9:0	gain	0X200	R/W	LED channel binning gain gain 0.50 = 0x100 gain 1.00 = 0x200 gain 1.99 = 0x3FF Note: Gain will be applied with saturation. Note: If this value is not configured, a default value of 0x200 will be used.

Table 10.5.2-12: Register **BIN_GAIN_10** (0XCA, page 3) LED10 bin class adoption gain configuration value

Bit	Name	Default	Access	Description
9:0	gain	0X200	R/W	LED channel binning gain gain 0.50 = 0x100 gain 1.00 = 0x200 gain 1.99 = 0x3FF Note: Gain will be applied with saturation. Note: If this value is not configured, a default value of 0x200 will be used.

Table 10.5.2-13: Register **BIN_GAIN_11** (0XCB, page 3) LED11 bin class adoption gain configuration value

Bit	Name	Default	Access	Description
9:0	gain	0X200	R/W	LED channel binning gain gain 0.50 = 0x100 gain 1.00 = 0x200 gain 1.99 = 0x3FF Note: Gain will be applied with saturation. Note: If this value is not configured, a default value of 0x200 will be used.

Table 10.5.2-14: Register **BIN_GAIN_12** (0XCC, page 3) LED12 bin class adoption gain configuration value

Bit	Name	Default	Access	Description
9:0	gain	0X200	R/W	LED channel binning gain gain 0.50 = 0x100 gain 1.00 = 0x200 gain 1.99 = 0x3FF Note: Gain will be applied with saturation. Note: If this value is not configured, a default value of 0x200 will be used.

Table 10.5.2-15: Register **BIN_GAIN_13** (0XCD, page 3) LED13 bin class adoption gain configuration value

Bit	Name	Default	Access	Description
9:0	gain	0X200	R/W	LED channel binning gain gain 0.50 = 0x100 gain 1.00 = 0x200 gain 1.99 = 0x3FF Note: Gain will be applied with saturation. Note: If this value is not configured, a default value of 0x200 will be used.

Table 10.5.2-16: Register **BIN_GAIN_14** (0XCE, page 3) LED14 bin class adoption gain configuration value

Bit	Name	Default	Access	Description
9:0	gain	0X200	R/W	LED channel binning gain gain 0.50 = 0x100 gain 1.00 = 0x200 gain 1.99 = 0x3FF

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				Note: Gain will be applied with saturation. Note: If this value is not configured, a default value of 0x200 will be used.

Table 10.5.2-17: Register **BIN_GAIN_15** (0XCF, page 3) LED15 bin class adoption gain configuration value

Bit	Name	Default	Access	Description
9:0	gain	0X200	R/W	LED channel binning gain gain 0.50 = 0x100 gain 1.00 = 0x200 gain 1.99 = 0x3FF Note: Gain will be applied with saturation. Note: If this value is not configured, a default value of 0x200 will be used.

Table 10.5.2-18: Register **BIN_GAIN_16** (0XD0, page 3) LED16 bin class adoption gain configuration value

Bit	Name	Default	Access	Description
9:0	gain	0X200	R/W	LED channel binning gain gain 0.50 = 0x100 gain 1.00 = 0x200 gain 1.99 = 0x3FF Note: Gain will be applied with saturation. Note: If this value is not configured, a default value of 0x200 will be used.

Table 10.5.2-19: Register **BIN_GAIN_17** (0XD1, page 3) LED17 bin class adoption gain configuration value

Bit	Name	Default	Access	Description
9:0	gain	0X200	R/W	LED channel binning gain gain 0.50 = 0x100 gain 1.00 = 0x200 gain 1.99 = 0x3FF Note: Gain will be applied with saturation. Note: If this value is not configured, a default value of 0x200 will be used.

Table 10.5.2-20: Register **BIN_GAIN_18** (0XD2, page 3) LED18 bin class adoption gain configuration value

Bit	Name	Default	Access	Description
9:0	gain	0X200	R/W	LED channel binning gain gain 0.50 = 0x100 gain 1.00 = 0x200 gain 1.99 = 0x3FF Note: Gain will be applied with saturation. Note: If this value is not configured, a default value of 0x200 will be used.

Table 10.5.2-21: Register **BIN_GAIN_19** (0XD3, page 3) LED19 bin class adoption gain configuration value

Bit	Name	Default	Access	Description
9:0	gain	0X200	R/W	LED channel binning gain gain 0.50 = 0x100 gain 1.00 = 0x200 gain 1.99 = 0x3FF Note: Gain will be applied with saturation. Note: If this value is not configured, a default value of 0x200 will be used.

Table 10.5.2-22: Register **BIN_GAIN_20** (0XD4, page 3) LED20 bin class adoption gain configuration value

Bit	Name	Default	Access	Description

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9:0	gain	0X200	R/W	LED channel binning gain gain 0.50 = 0x100 gain 1.00 = 0x200 gain 1.99 = 0x3FF Note: Gain will be applied with saturation. Note: If this value is not configured, a default value of 0x200 will be used.

Table 10.5.2-23: Register **BIN_GAIN_21** (0XD5, page 3) LED21 bin class adoption gain configuration value

Bit	Name	Default	Access	Description
9:0	gain	0X200	R/W	LED channel binning gain gain 0.50 = 0x100 gain 1.00 = 0x200 gain 1.99 = 0x3FF Note: Gain will be applied with saturation. Note: If this value is not configured, a default value of 0x200 will be used.

Table 10.5.2-24: Register **BIN_GAIN_22** (0XD6, page 3) LED22 bin class adoption gain configuration value

Bit	Name	Default	Access	Description
9:0	gain	0X200	R/W	LED channel binning gain gain 0.50 = 0x100 gain 1.00 = 0x200 gain 1.99 = 0x3FF Note: Gain will be applied with saturation. Note: If this value is not configured, a default value of 0x200 will be used.

Table 10.5.2-25: Register **BIN_GAIN_23** (0XD7, page 3) LED23 bin class adoption gain configuration value

Bit	Name	Default	Access	Description
9:0	gain	0X200	R/W	LED channel binning gain gain 0.50 = 0x100 gain 1.00 = 0x200 gain 1.99 = 0x3FF Note: Gain will be applied with saturation. Note: If this value is not configured, a default value of 0x200 will be used.

Table 10.5.2-26: Register **EBIN_AND_ADDR0_CUR (**0XD8, page 3) configure EBIN or ADDR0 pin source current

Bit	Name	Default	Access	Description
9:4	-	0	R	
3:2	addr0_cur	01	R/W	00, ADDR0 pin current [mA] = 0. 01, ADDR0 pin current [mA] = 0.5mA. 11, ADDR0 pin current [mA] = 1mA
1:0	ebin_cur	00	R/W	00, EBIN pin bin class evaluation current [mA] = 0. 01, EBIN pin bin class evaluation current [mA] = 0.5mA. 11, EBIN pin bin class evaluation current [mA] = 1mA.

Table 10.5.2-27: Register **EBIN_CLASS_ENABLE_0_7** (0XD9, page 3) evaluated LED bin class assignment configuration value

Bit	Name	Default	Access	Description
9:8	-	0	R	
7:0	enable	0	R/W	‘1’, selects which LED pins (0 to 7) are supplied with determined bin class gain which is determined by EBIN. ‘0’, disable

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Table 10.5.2-28: Register **EBIN_CLASS_ENABLE_8_15** (0XDA, page 3) evaluated LED bin class assignment configuration value

Bit	Name	Default	Access	Description
9:8	-	0	R	
7:0	enable	0	R/W	'1', selects which LED pins (8 to 15) are supplied with determined bin class gain which is determined by EBIN. '0', disable

Table 10.5.2-29: Register **EBIN_CLASS_ENABLE_16_23** (0XDB, page 3) evaluated LED bin class assignment configuration value

Bit	Name	Default	Access	Description
9:8	-	0	R	
7:0	enable	0	R/W	'1', selects which LED pins (16 to 23) are supplied with determined bin class gain which is determined by EBIN. '0', disable

Table 10.5.2-30: Register **BIN_CLASS_LEVEL_0** (0XDF, page 3) LED bin class evaluation level value

Bit	Name	Default	Access	Description
9:0	level	0	R/W	bin class compare level definition

Table 10.5.2-31: Register **BIN_CLASS_LEVEL_1** (0XE0, page 3) LED bin class evaluation level value

Bit	Name	Default	Access	Description
9:0	level	0	R/W	bin class comparison level definition

Table 10.5.2-32: Register **BIN_CLASS_LEVEL_2** (0XE1, page 3) LED bin class evaluation level value

Bit	Name	Default	Access	Description
9:0	level	0	R/W	bin class comparison level definition

Table 10.5.2-33: Register **BIN_CLASS_LEVEL_3** (0XE2, page 3) LED bin class evaluation level value

Bit	Name	Default	Access	Description
9:0	level	0	R/W	bin class comparison level definition

Table 10.5.2-34: Register **BIN_CLASS_GAIN_0** (0XE3, page 3) evaluated LED bin class 0 gain value

Bit	Name	Default	Access	Description
9:0	gain	0	R/W	bin class gain value definition gain 0.50 = 0x100 gain 1.00 = 0x200 gain 1.99 = 0x3FF Note: Gain will be applied with saturation.

Table 10.5.2-35: Register **BIN_CLASS_GAIN_1** (0XE4, page 3) evaluated LED bin class 1 gain value

Bit	Name	Default	Access	Description
9:0	gain	0	R/W	bin class gain value definition gain 0.50 = 0x100 gain 1.00 = 0x200 gain 1.99 = 0x3FF Note: Gain will be applied with saturation.

Table 10.5.2-36: Register **BIN_CLASS_GAIN_2** (0XE5, page 3) evaluated LED bin class 2 gain value

Bit	Name	Default	Access	Description
9:0	gain	0	R/W	bin class gain value definition gain 0.50 = 0x100 gain 1.00 = 0x200 gain 1.99 = 0x3FF Note: Gain will be applied with saturation.

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Table 10.5.2-37: Register **BIN_CLASS_GAIN_3** (0XE6, page 3) evaluated LED bin class 3 gain value

Bit	Name	Default	Access	Description
9:0	gain	0	R/W	bin class gain value definition gain 0.50 = 0x100 gain 1.00 = 0x200 gain 1.99 = 0x3FF Note: Gain will be applied with saturation.

Table 10.5.2-38: Register **BIN_CLASS_GAIN_4** (0XE7, page 3) evaluated LED bin class 4 gain value

Bit	Name	Default	Access	Description
9:0	gain	0	R/W	bin class gain value definition gain 0.50 = 0x100 gain 1.00 = 0x200 gain 1.99 = 0x3FF Note: Gain will be applied with saturation.

Table 10.5.2-39: Register **BUST_CURRENT_0** (0XD8, page 1) BUS timeout mode LED0 sink current configuration value

Bit	Name	Default	Access	Description
9:0	sel	0	R/W	BUS timeout mode driver channel current selection driver current [100uA] The driver current will be limited to the related IDAC selected range maximum current.

Table 10.5.2-40: Register **BUST_CURRENT_1** (0XD9, page 1) BUS timeout mode LED1 sink current configuration value

Bit	Name	Default	Access	Description
9:0	sel	0	R/W	BUS timeout mode driver channel current selection driver current [100uA] The driver current will be limited to the related IDAC selected range maximum current.

Table 10.5.2-41: Register **BUST_CURRENT_2** (0XDA, page 1) BUS timeout mode LED2 sink current configuration value

Bit	Name	Default	Access	Description
9:0	sel	0	R/W	BUS timeout mode driver channel current selection driver current [100uA] The driver current will be limited to the related IDAC selected range maximum current.

Table 10.5.2-42: Register **BUST_CURRENT_3** (0XDB, page 1) BUS timeout mode LED3 sink current configuration value

Bit	Name	Default	Access	Description
9:0	sel	0	R/W	BUS timeout mode driver channel current selection driver current [100uA] The driver current will be limited to the related IDAC selected range maximum current.

Table 10.5.2-43: Register **BUST_CURRENT_4** (0XDC, page 1) BUS timeout mode LED4 sink current configuration value

Bit	Name	Default	Access	Description
9:0	sel	0	R/W	BUS timeout mode driver channel current selection driver current [100uA] The driver current will be limited to the related IDAC selected range maximum current.

Table 10.5.2-44: Register **BUST_CURRENT_5** (0XDD, page 1) BUS timeout mode LED5 sink current configuration value

Bit	Name	Default	Access	Description
9:0	sel	0	R/W	BUS timeout mode driver channel current selection driver current [100uA]

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				The driver current will be limited to the related IDAC selected range maximum current.

Table 10.5.2-45: Register **BUST_CURRENT_6** (0XDE, page 1) BUS timeout mode LED6 sink current configuration value

Bit	Name	Default	Access	Description
9:0	sel	0	R/W	BUS timeout mode driver channel current selection driver current [100uA] The driver current will be limited to the related IDAC selected range maximum current.

Table 10.5.2-46: Register **BUST_CURRENT_7** (0XDF, page 1) BUS timeout mode LED7 sink current configuration value

Bit	Name	Default	Access	Description
9:0	sel	0	R/W	BUS timeout mode driver channel current selection driver current [100uA] The driver current will be limited to the related IDAC selected range maximum current.

Table 10.5.2-47: Register **BUST_CURRENT_8** (0XE0, page 1) BUS timeout mode LED8 sink current configuration value

Bit	Name	Default	Access	Description
9:0	sel	0	R/W	BUS timeout mode driver channel current selection driver current [100uA] The driver current will be limited to the related IDAC selected range maximum current.

Table 10.5.2-48: Register **BUST_CURRENT_9** (0XE1, page 1) BUS timeout mode LED9 sink current configuration value

Bit	Name	Default	Access	Description
9:0	sel	0	R/W	BUS timeout mode driver channel current selection driver current [100uA] The driver current will be limited to the related IDAC selected range maximum current.

Table 10.5.2-49: Register **BUST_CURRENT_10** (0XE2, page 1) BUS timeout mode LED10 sink current configuration value

Bit	Name	Default	Access	Description
9:0	sel	0	R/W	BUS timeout mode driver channel current selection driver current [100uA] The driver current will be limited to the related IDAC selected range maximum current.

Table 10.5.2-50: Register **BUST_CURRENT_11** (0XE3 page 1) BUS timeout mode LED11 sink current configuration value

Bit	Name	Default	Access	Description
9:0	sel	0	R/W	BUS timeout mode driver channel current selection driver current [100uA] The driver current will be limited to the related IDAC selected range maximum current.

Table 10.5.2-51: Register **BUST_CURRENT_12** (0XE4, page 1) BUS timeout mode LED12 sink current configuration value

Bit	Name	Default	Access	Description
9:0	sel	0	R/W	BUS timeout mode driver channel current selection driver current [100uA] The driver current will be limited to the related IDAC selected range maximum current.

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Table 10.5.2-52: Register **BUST_CURRENT_13** (0XE5, page 1) BUS timeout mode LED13 sink current configuration value

Bit	Name	Default	Access	Description
9:0	sel	0	R/W	BUS timeout mode driver channel current selection driver current [100uA] The driver current will be limited to the related IDAC selected range maximum current.

Table 10.5.2-53: Register **BUST_CURRENT_14** (0XE6, page 1) BUS timeout mode LED14 sink current configuration value

Bit	Name	Default	Access	Description
9:0	sel	0	R/W	BUS timeout mode driver channel current selection driver current [100uA] The driver current will be limited to the related IDAC selected range maximum current.

Table 10.5.2-54: Register **BUST_CURRENT_15** (0XE7, page 1) BUS timeout mode LED15 sink current configuration value

Bit	Name	Default	Access	Description
9:0	sel	0	R/W	BUS timeout mode driver channel current selection driver current [100uA] The driver current will be limited to the related IDAC selected range maximum current.

Table 10.5.2-55: Register **BUST_CURRENT_16** (0XE8, page 1) BUS timeout mode LED16 sink current configuration value

Bit	Name	Default	Access	Description
9:0	sel	0	R/W	BUS timeout mode driver channel current selection driver current [100uA] The driver current will be limited to the related IDAC selected range maximum current.

Table 10.5.2-56: Register **BUST_CURRENT_17** (0XE9, page 1) BUS timeout mode LED17 sink current configuration value

Bit	Name	Default	Access	Description
9:0	sel	0	R/W	BUS timeout mode driver channel current selection driver current [100uA] The driver current will be limited to the related IDAC selected range maximum current.

Table 10.5.2-57: Register **BUST_CURRENT_18** (0XEA, page 1) BUS timeout mode LED18 sink current configuration value

Bit	Name	Default	Access	Description
9:0	sel	0	R/W	BUS timeout mode driver channel current selection driver current [100uA] The driver current will be limited to the related IDAC selected range maximum current.

Table 10.5.2-58: Register **BUST_CURRENT_19** (0XEB, page 1) BUS timeout mode LED19 sink current configuration value

Bit	Name	Default	Access	Description
9:0	sel	0	R/W	BUS timeout mode driver channel current selection driver current [100uA] The driver current will be limited to the related IDAC selected range maximum current.

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Table 10.5.2-59: Register **BUST_CURRENT_20** (0XEC, page 1) BUS timeout mode LED20 sink current configuration value

Bit	Name	Default	Access	Description
9:0	sel	0	R/W	BUS timeout mode driver channel current selection driver current [100uA] The driver current will be limited to the related IDAC selected range maximum current.

Table 10.5.2-60: Register **BUST_CURRENT_21** (0XED, page 1) BUS timeout mode LED21 sink current configuration value

Bit	Name	Default	Access	Description
9:0	sel	0	R/W	BUS timeout mode driver channel current selection driver current [100uA] The driver current will be limited to the related IDAC selected range maximum current.

Table 10.5.2-61: Register **BUST_CURRENT_22** (0XEE, page 1) BUS timeout mode LED22 sink current configuration value

Bit	Name	Default	Access	Description
9:0	sel	0	R/W	BUS timeout mode driver channel current selection driver current [100uA] The driver current will be limited to the related IDAC selected range maximum current.

Table 10.5.2-62: Register **BUST_CURRENT_23** (0XEF, page 1) BUS timeout mode LED23 sink current configuration value

Bit	Name	Default	Access	Description
9:0	sel	0	R/W	BUS timeout mode driver channel current selection driver current [100uA] The driver current will be limited to the related IDAC selected range maximum current.

Table 10.5.2-63: Register **EXPWM_CURRENT_0** (0XE5, page 2) Direct PWM mode LED0 sink current configuration value

Bit	Name	Default	Access	Description
9:0	sel	0	R/W	Direct PWM mode driver channel current selection driver current [100uA] The driver current will be limited to the related IDAC selected range maximum current.

Table 10.5.2-64: Register **EXPWM_CURRENT_1** (0XE6, page 2) Direct PWM mode LED1 sink current configuration value

Bit	Name	Default	Access	Description
9:0	sel	0	R/W	Direct PWM mode driver channel current selection driver current [100uA] The driver current will be limited to the related IDAC selected range maximum current.

Table 10.5.2-65: Register **EXPWM_CURRENT_2** (0XE7, page 2) Direct PWM mode LED2 sink current configuration value

Bit	Name	Default	Access	Description
9:0	sel	0	R/W	Direct PWM mode driver channel current selection driver current [100uA] The driver current will be limited to the related IDAC selected range maximum current.

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Table 10.5.2-66: Register **EXPWM_CURRENT_3** (0XE8, page 2) Direct PWM mode LED3 sink current configuration value

Bit	Name	Default	Access	Description
9:0	sel	0	R/W	Direct PWM mode driver channel current selection driver current [100uA] The driver current will be limited to the related IDAC selected range maximum current.

Table 10.5.2-67: Register **EXPWM_CURRENT_4** (0XE9, page 2) Direct PWM mode LED4 sink current configuration value

Bit	Name	Default	Access	Description
9:0	sel	0	R/W	Direct PWM mode driver channel current selection driver current [100uA] The driver current will be limited to the related IDAC selected range maximum current.

Table 10.5.2-68: Register **EXPWM_CURRENT_5** (0XEA, page 2) Direct PWM mode LED5 sink current configuration value

Bit	Name	Default	Access	Description
9:0	sel	0	R/W	Direct PWM mode driver channel current selection driver current [100uA] The driver current will be limited to the related IDAC selected range maximum current.

Table 10.5.2-69: Register **EXPWM_CURRENT_6** (0XEB, page 2) Direct PWM mode LED6 sink current configuration value

Bit	Name	Default	Access	Description
9:0	sel	0	R/W	Direct PWM mode driver channel current selection driver current [100uA] The driver current will be limited to the related IDAC selected range maximum current.

Table 10.5.2-70: Register **EXPWM_CURRENT_7** (0XEC, page 2) Direct PWM mode LED7 sink current configuration value

Bit	Name	Default	Access	Description
9:0	sel	0	R/W	Direct PWM mode driver channel current selection driver current [100uA] The driver current will be limited to the related IDAC selected range maximum current.

Table 10.5.2-71: Register **EXPWM_CURRENT_8** (0XED, page 2) Direct PWM mode LED8 sink current configuration value

Bit	Name	Default	Access	Description
9:0	sel	0	R/W	Direct PWM mode driver channel current selection driver current [100uA] The driver current will be limited to the related IDAC selected range maximum current.

Table 10.5.2-72: Register **EXPWM_CURRENT_9** (0XEE, page 2) Direct PWM mode LED9 sink current configuration value

Bit	Name	Default	Access	Description
9:0	sel	0	R/W	Direct PWM mode driver channel current selection driver current [100uA] The driver current will be limited to the related IDAC selected range maximum current.

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Table 10.5.2-73: Register **EXPWM_CURRENT_10** (0XEF, page 2) Direct PWM mode LED10 sink current configuration value

Bit	Name	Default	Access	Description
9:0	sel	0	R/W	Direct PWM mode driver channel current selection driver current [100uA] The driver current will be limited to the related IDAC selected range maximum current.

Table 10.5.2-74: Register **EXPWM_CURRENT_11** (0XF0, page 2) Direct PWM mode LED11 sink current configuration value

Bit	Name	Default	Access	Description
9:0	sel	0	R/W	Direct PWM mode driver channel current selection driver current [100uA] The driver current will be limited to the related IDAC selected range maximum current.

Table 10.5.2-75: Register **EXPWM_CURRENT_12** (0XF1, page 2) Direct PWM mode LED12 sink current configuration value

Bit	Name	Default	Access	Description
9:0	sel	0	R/W	Direct PWM mode driver channel current selection driver current [100uA] The driver current will be limited to the related IDAC selected range maximum current.

Table 10.5.2-76: Register **EXPWM_CURRENT_13** (0XF2, page 2) Direct PWM mode LED13 sink current configuration value

Bit	Name	Default	Access	Description
9:0	sel	0	R/W	Direct PWM mode driver channel current selection driver current [100uA] The driver current will be limited to the related IDAC selected range maximum current.

Table 10.5.2-77: Register **EXPWM_CURRENT_14** (0XF3, page 2) Direct PWM mode LED14 sink current configuration value

Bit	Name	Default	Access	Description
9:0	sel	0	R/W	Direct PWM mode driver channel current selection driver current [100uA] The driver current will be limited to the related IDAC selected range maximum current.

Table 10.5.2-78: Register **EXPWM_CURRENT_15** (0XF4, page 2) Direct PWM mode LED15 sink current configuration value

Bit	Name	Default	Access	Description
9:0	sel	0	R/W	Direct PWM mode driver channel current selection driver current [100uA] The driver current will be limited to the related IDAC selected range maximum current.

Table 10.5.2-79: Register **EXPWM_CURRENT_16** (0XF5, page 2) Direct PWM mode LED16 sink current configuration value

Bit	Name	Default	Access	Description
9:0	sel	0	R/W	Direct PWM mode driver channel current selection driver current [100uA] The driver current will be limited to the related IDAC selected range maximum current.

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Table 10.5.2-80: Register **EXPWM_CURRENT_17** (0XF6, page 2) Direct PWM mode LED17 sink current configuration value

Bit	Name	Default	Access	Description
9:0	sel	0	R/W	Direct PWM mode driver channel current selection driver current [100uA] The driver current will be limited to the related IDAC selected range maximum current.

Table 10.5.2-81: Register **EXPWM_CURRENT_18** (0XF7, page 2) Direct PWM mode LED18 sink current configuration value

Bit	Name	Default	Access	Description
9:0	sel	0	R/W	Direct PWM mode driver channel current selection driver current [100uA] The driver current will be limited to the related IDAC selected range maximum current.

Table 10.5.2-82: Register **EXPWM_CURRENT_19** (0XF8, page 2) Direct PWM mode LED19 sink current configuration value

Bit	Name	Default	Access	Description
9:0	sel	0	R/W	Direct PWM mode driver channel current selection driver current [100uA] The driver current will be limited to the related IDAC selected range maximum current.

Table 10.5.2-83: Register **EXPWM_CURRENT_20** (0XF9, page 2) Direct PWM mode LED20 sink current configuration value

Bit	Name	Default	Access	Description
9:0	sel	0	R/W	Direct PWM mode driver channel current selection driver current [100uA] The driver current will be limited to the related IDAC selected range maximum current.

Table 10.5.2-84: Register **EXPWM_CURRENT_21** (0XFA, page 2) Direct PWM mode LED21 sink current configuration value

Bit	Name	Default	Access	Description
9:0	sel	0	R/W	Direct PWM mode driver channel current selection driver current [100uA] The driver current will be limited to the related IDAC selected range maximum current.

Table 10.5.2-85: Register **EXPWM_CURRENT_22** (0XFB, page 2) Direct PWM mode LED22 sink current configuration value

Bit	Name	Default	Access	Description
9:0	sel	0	R/W	Direct PWM mode driver channel current selection driver current [100uA] The driver current will be limited to the related IDAC selected range maximum current.

Table 10.5.2-86: Register **EXPWM_CURRENT_23** (0XFC, page 2) Direct PWM mode LED23 sink current configuration value

Bit	Name	Default	Access	Description
9:0	sel	0	R/W	Direct PWM mode driver channel current selection driver current [100uA] The driver current will be limited to the related IDAC selected range maximum current.

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Table 10.5.2-87: Register **LED_ENABLE2_0_7** (0XF0, page 1) LED driver channels 0 to 7 enable value in BUS timeout /direct PWM mode

Bit	Name	Default	Access	Description
9:8	-	0	R	
7:0	enable	0	R/W	enable for driver channels 0 to 7 in BUS timeout /direct PWM mode bit 0: enable for driver channel 0 ... bit 7: enable for driver channel 7 0 disables the analog section of channel driver 1 enables the analog section of channel driver Note: Used to save current when channel drivers are OFF.

Table 10.5.2-88: Register **LED_ENABLE2_8_15** (0XF1, page 1) LED driver channels 8 to 15 enable value in BUS timeout /direct PWM mode

Bit	Name	Default	Access	Description
9:8	-	0	R	
7:0	enable	0	R/W	enable for driver channels 8 to 15 in BUS timeout/direct PWM mode bit 0: enable for driver channel 8 ... bit 7: enable for driver channel 15 an enable bit value of 0 disables channel driver analog part an enable bit value of 1 enables channel driver analog part Note: Used to save current when channel drivers are OFF.

Table 10.5.2-89: Register **LED_ENABLE2_16_23** (0XF2, page 1) LED driver channels 16 to 23 enable value in BUS timeout/direct PWM mode

Bit	Name	Default	Access	Description
9:8	-	0	R	
7:0	enable	0	R/W	enable for driver channels 16 to 23 in BUS timeout/direct PWM mode bit 0: enable for driver channel 16 ... bit 7: enable for driver channel 23 an enable bit value of 0 disables channel driver analog part an enable bit value of 1 enables channel driver analog part Note: Used to save current when channel drivers are OFF.

Table 10.5.2-90: Register **IDAC_REF_SEL_0_7** (0XF3, page 1) LED channels 0 to 7 IDAC reference selection value

Bit	Name	Default	Access	Description
9:8	-	0	R	
7:0	sel	0	R/W	IDAC reference (range) selection for driver channels 0 to 7 bit 0: select IDAC reference for driver channel 0 ... bit 7: select IDAC reference for driver channel 7 a sel bit value of 0 selects IDAC upper range a sel bit value of 1 selects IDAC lower range

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Table 10.5.2-91: Register **IDAC_REF_SEL_8_15** (0XF4, page 1) LED channels 8 to 15 IDAC reference selection value

Bit	Name	Default	Access	Description
9:8	-	0	R	
7:0	sel	0	R/W	IDAC reference (range) selection for driver channels 8 to 15 bit 0: select IDAC reference for driver channel 8 ... bit 7: select IDAC reference for driver channel 15 a sel bit value of 0 selects IDAC upper range a sel bit value of 1 selects IDAC lower range

Table 10.5.2-92: Register **IDAC_REF_SEL_16_23** (0XF5, page 1) LED channels 16 to 23 IDAC reference selection value

Bit	Name	Default	Access	Description
9:8	-	0	R	
7:0	sel	0	R/W	IDAC reference (range) selection for driver channels 16 to 23 bit 0: select IDAC reference for driver channel 16 ... bit 7: select IDAC reference for driver channel 23 a sel bit value of 0 selects IDAC upper range a sel bit value of 1 selects IDAC lower range

Table 10.5.2-93: Register **ISINK_CONFIG** (0XFB, page 1) LED current slew rate configuration value

Bit	Name	Default	Access	Description
9:2	-	0	R	
1:0	slew	0	R/W	driver slew rate configuration 00: please see $t_{SINK_RISE_0}$ and $t_{SINK_FALL_0}$ parameters 01: please see $t_{SINK_RISE_1}$ and $t_{SINK_FALL_1}$ parameter 10: please see $t_{SINK_RISE_2}$ and $t_{SINK_FALL_2}$ parameters 11: please see $t_{SINK_RISE_3}$ and $t_{SINK_FALL_3}$ parameters

Table 10.5.2-94: Register **VT_OFFSET_TSTART** (0xFE, page 2) device temperature start to configuration value compensate led drop voltage during high temperature

Bit	Name	Default	Access	Description
9:0	start	0	R/W	temperature level at which VT offset output starts [1LSB/K] Note: start = 0 disables VT offset regulation and detection

Table 10.5.2-95: Register **VT_OFFSET_TSTOP** (0xFF, page 2) device temperature stop to configuration value compensate led drop voltage during high temperature

Bit	Name	Default	Access	Description
9:0	stop	0	R/W	temperature level at which VT offset output stops [1LSB/K] Note: stop = 0 disables VT offset regulation and detection

Table 10.5.2-96: Register **VS_DERATE_RANGE** (0xE8, page 3) LED supply's based derating range configuration value

Bit	Name	Default	Access	Description
9:5	stop	0	R/W	LED supply voltage level at which derating stops [V] 0: derating disabled n (n! = 0): derating stops at LED supply = n V
4:0	start	0	R/W	LED supply voltage level at which derating starts [V] 0: derating disabled n (n! = 0): derating starts at LED supply = n V

Table 10.5.2-97: Register **VT_DERATE_START** (0XE9, page 3) device temperature-based derating start configuration value

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Bit	Name	Default	Access	Description
9:0	start	0	R/W	temperature level at which derating starts [K] Note: start = 0 disables temperature derating

Table 10.5.2-98: Register **VT_DERATE_STOP** (0XEA, page 3) device temperature-based derating stops configuration value

Bit	Name	Default	Access	Description
9:0	stop	0	R/W	temperature level at which derating stops [K] Note: stop= 0 disables temperature derating

Table 10.5.2-99: Register **DERATE_GAIN** (0XEB, page 3) derating gain configuration value

Bit	Name	Default	Access	Description
9:5	vt_gain	0	R/W	defines reduction of nominal LED current per Kelvin between VT_{start} and VT_{stop} VT derating multiplier (M_{VT_derate}) in case VT derating is enabled: • if VT <= VT_{start} : M_{VT_derate} = 1 • if VT_{start} < VT < VT_{stop} : M_{VT_derate} = 1 - (vt_gain * (VT - VT_{start}) / 256) • this equals a derating by vt_gain * 0.39% of nominal LED current per Kelvin • if VT >= VT_{stop} : M_{VT_derate} = 1 - (vt_gain * (VT_{stop} - VT_{start}) / 256) Note: If calculation of M_{VT_derate} gives a negative value, M_{VT_derate} will be set to 0.
4:0	vs_gain	0	R/W	defines reduction of nominal LED current per Volt between VS_{start} and VS_{stop} VS derating multiplier (M_{VS_derate}) in case VS derating is enabled: • if VS <= VS_{start} : M_{VS_derate} = 1 • if VS_{start} < VS < VS_{stop} : M_{VS_derate} = 1 - (vs_gain * (VS - VS_{start}) / (16 * 25)) • this equals a derating by vs_gain * 0.25% of nominal LED current per Volt • if VS >= VS_{stop} : M_{VS_derate} = 1 - (vs_gain * (VS_{stop} - VS_{start}) / (16 * 25)) Note: If calculation of M_{VS_derate} gives a negative value, M_{VS_derate} will be set to 0.

Table 10.5.2-100: Register **STARTUP_TIME** (0XEC, page 3) time configuration value to wait for DC-DC stead state

Bit	Name	Default	Access	Description
9:3	-	0	R	
2:0	wait	0X7	R/W	000: 5ms, 001: 10ms, 010: 20ms, 011: 50ms 100: 100ms, 101:1 50ms, 110: 200ms, 111: 0ms(default)

10.6. Measurement and diagnosis

Table 10.6.1-1: STANDALONE

Register Name	Register page	Address	Description
LED_OPEN_THR_1	2	0XC0	LED open detection threshold level 1 configuration value
LED_OPEN_THR_2	2	0XC1	LED open detection threshold level 2 configuration value
LED_OPEN_THR_3	2	0XC2	LED open detection threshold level 3 configuration value

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LED_OPEN_SEL_0_3	2	0XC3	LED open threshold level to LED channels 0 to 3 assignment configuration value
LED_OPEN_SEL_4_7	2	0XC4	LED open threshold level to LED channels 4 to 7 assignment configuration value
LED_OPEN_SEL_8_11	2	0XC5	LED open threshold level to LED channels 8 to 11 assignment configuration value
LED_OPEN_SEL_12_15	2	0XC6	LED open threshold level to LED channels 12 to 15 assignment configuration value
LED_OPEN_SEL_16_19	2	0XC7	LED open threshold level to LED channels 16 to 19 assignment configuration value
LED_OPEN_SEL_20_23	2	0XC8	LED open threshold level to LED channels 20 to 23 assignment configuration value
LED_SHORT_THR_1	2	0XC9	LED short detection threshold level 1 configuration value
LED_SHORT_THR_2	2	0XCA	LED short detection threshold level 2 configuration value
LED_SHORT_THR_3	2	0XCB	LED short detection threshold level 3 configuration value
LED_SHORT_SEL_0_3	2	0XCC	LED short threshold level to LED channels 0 to 3 assignment configuration value
LED_SHORT_SEL_4_7	2	0XCD	LED short threshold level to LED channels 4 to 7 assignment configuration value
LED_SHORT_SEL_8_11	2	0XCE	LED short threshold level to LED channels 8 to 11 assignment configuration value
LED_SHORT_SEL_12_15	2	0XCF	LED short threshold level to LED channels 12 to 15 assignment configuration value
LED_SHORT_SEL_16_19	2	0XD0	LED short threshold level to LED channels 16 to 19 assignment configuration value
LED_SHORT_SEL_20_23	2	0XD1	LED short threshold level to LED channels 20 to 23 assignment configuration value
VS_TOO_LOW	2	0XD3	VS too low watch configuration value
VS_CRITICAL	2	0XD4	VS too high watch configuration value
VT_CRITICAL	2	0XD5	VT too high watch configuration value
EBIN_MIN_THR	2	0XD6	EBIN minimum voltage for short-to-GND protection
EBIN_MAX_THR	2	0XD7	EBIN maximum voltage for open protection
DIAG_CONFIG	2	0XD8	Set single lamp or multi-lamp for diagnosis behavior. Set the error filter counter.
DIAG0_CONFIG_0_7	2	0XD9	diagnosis group 0 configuration for LED channels 0 to 7
DIAG0_CONFIG_8_15	2	0XDA	diagnosis group 0 configuration for LED channels 8 to 15
DIAG0_CONFIG_16_23	2	0XDB	diagnosis group 0 configuration for LED channels 16 to 23
DIAG1_CONFIG_0_7	2	0XDC	diagnosis group 1 configuration for LED channels 0 to 7
DIAG1_CONFIG_8_15	2	0XDD	diagnosis group 1 configuration for LED channels 8 to 15
DIAG1_CONFIG_16_23	2	0XDE	diagnosis group 1 configuration for LED channels 16 to 23

Table 10.6.1-2: Register **LED_OPEN_THR_1** (0XC0, page 2) LED open detection threshold level 1 configuration value

Bit	Name	Default	Access	Description
9:0	level	0X010	R/W	LED OPEN detection threshold level [46 LSB/V], default value is 0X010 (0.34V) Note: OPEN condition, if the LED pin voltage sample

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				value is smaller than the selected detection threshold level.

Table 10.6.1-3: Register **LED_OPEN_THR_2** (0XC1, page 2) LED open detection threshold level 2 configuration value

Bit	Name	Default	Access	Description
9:0	level	0	R/W	LED OPEN detection threshold level [46 LSB/V] Note: OPEN condition, if the LED pin voltage sample value is smaller than the selected detection threshold level.

Table 10.6.1-4: Register **LED_OPEN_THR_3** (0XC2, page 2) LED open detection threshold level 3 configuration value

Bit	Name	Default	Access	Description
9:0	level	0	R/W	LED OPEN detection threshold level [46 LSB/V] Note: OPEN condition, if the LED pin voltage sample value is smaller than the selected detection threshold level.

Table 10.6.1-5: Register **LED_OPEN_SEL_0_3** (0XC3, page 2) LED open threshold level to LED channels 0 to 3 assignment configuration value

Bit	Name	Default	Access	Description
9:8	-	0	R	
7:6	led3	1	R/W	OPEN level selection 0: OPEN detection disabled 1: LED_OPEN_THR_1 level is used(default) 2: LED_OPEN_THR_2 level is used 3: LED_OPEN_THR_3 level is used
5:4	led2	1	R/W	OPEN level selection 0: OPEN detection disabled 1: LED_OPEN_THR_1 level is used(default) 2: LED_OPEN_THR_2 level is used 3: LED_OPEN_THR_3 level is used
3:2	led1	1	R/W	OPEN level selection 0: OPEN detection disabled 1: LED_OPEN_THR_1 level is used(default) 2: LED_OPEN_THR_2 level is used 3: LED_OPEN_THR_3 level is used
1:0	led0	1	R/W	OPEN level selection 0: OPEN detection disabled 1: LED_OPEN_THR_1 level is used(default) 2: LED_OPEN_THR_2 level is used 3: LED_OPEN_THR_3 level is used

Table 10.6.1-6: Register **LED_OPEN_SEL_4_7** (0XC4, page 2) LED open threshold level to LED channels 4 to 7 assignment configuration value

Bit	Name	Default	Access	Description
9:8	-	0	R	
7:6	led7	1	R/W	OPEN level selection 0: OPEN detection disabled 1: LED_OPEN_THR_1 level is used(default) 2: LED_OPEN_THR_2 level is used 3: LED_OPEN_THR_3 level is used
5:4	led6	1	R/W	OPEN level selection 0: OPEN detection disabled 1: LED_OPEN_THR_1 level is used(default) 2: LED_OPEN_THR_2 level is used 3: LED_OPEN_THR_3 level is used

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3:2	led5	1	R/W	OPEN level selection 0: OPEN detection disabled 1: LED_OPEN_THR_1 level is used(default) 2: LED_OPEN_THR_2 level is used 3: LED_OPEN_THR_3 level is used
1:0	led4	1	R/W	OPEN level selection 0: OPEN detection disabled 1: LED_OPEN_THR_1 level is used(default) 2: LED_OPEN_THR_2 level is used 3: LED_OPEN_THR_3 level is used

Table 10.6.1-7: Register **LED_OPEN_SEL_8_11** (0XC5, page 2) LED open threshold level to LED channels 8 to 11 assignment configuration value

Bit	Name	Default	Access	Description
9:8	-	0	R	
7:6	led11	1	R/W	OPEN level selection 0: OPEN detection disabled 1: LED_OPEN_THR_1 level is used(default) 2: LED_OPEN_THR_2 level is used 3: LED_OPEN_THR_3 level is used
5:4	led10	1	R/W	OPEN level selection 0: OPEN detection disabled 1: LED_OPEN_THR_1 level is used(default) 2: LED_OPEN_THR_2 level is used 3: LED_OPEN_THR_3 level is used
3:2	led9	1	R/W	OPEN level selection 0: OPEN detection disabled 1: LED_OPEN_THR_1 level is used(default) 2: LED_OPEN_THR_2 level is used 3: LED_OPEN_THR_3 level is used
1:0	led8	1	R/W	OPEN level selection 0: OPEN detection disabled 1: LED_OPEN_THR_1 level is used(default) 2: LED_OPEN_THR_2 level is used 3: LED_OPEN_THR_3 level is used

Table 10.6.1-8: Register **LED_OPEN_SEL_12_15** (0XC6, page 2) LED open threshold level to LED channels 12 to 15 assignment configuration value

Bit	Name	Default	Access	Description
9:8	-	0	R	
7:6	led15	1	R/W	OPEN level selection 0: OPEN detection disabled 1: LED_OPEN_THR_1 level is used(default) 2: LED_OPEN_THR_2 level is used 3: LED_OPEN_THR_3 level is used
5:4	led14	1	R/W	OPEN level selection 0: OPEN detection disabled 1: LED_OPEN_THR_1 level is used(default) 2: LED_OPEN_THR_2 level is used 3: LED_OPEN_THR_3 level is used
3:2	led13	1	R/W	OPEN level selection 0: OPEN detection disabled 1: LED_OPEN_THR_1 level is used(default) 2: LED_OPEN_THR_2 level is used 3: LED_OPEN_THR_3 level is used

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1:0	led12	1	R/W	OPEN level selection 0: OPEN detection disabled 1: LED_OPEN_THR_1 level is used(default) 2: LED_OPEN_THR_2 level is used 3: LED_OPEN_THR_3 level is used

Table 10.6.1-9: Register **LED_OPEN_SEL_16_19** (0XC7, page 2) LED open threshold level to LED channels 12 to 15 assignment configuration value

Bit	Name	Default	Access	Description
9:8	-	0	R	
7:6	led19	1	R/W	OPEN level selection 0: OPEN detection disabled 1: LED_OPEN_THR_1 level is used(default) 2: LED_OPEN_THR_2 level is used 3: LED_OPEN_THR_3 level is used
5:4	led18	1	R/W	OPEN level selection 0: OPEN detection disabled 1: LED_OPEN_THR_1 level is used(default) 2: LED_OPEN_THR_2 level is used 3: LED_OPEN_THR_3 level is used
3:2	led17	1	R/W	OPEN level selection 0: OPEN detection disabled 1: LED_OPEN_THR_1 level is used(default) 2: LED_OPEN_THR_2 level is used 3: LED_OPEN_THR_3 level is used
1:0	led16	1	R/W	OPEN level selection 0: OPEN detection disabled 1: LED_OPEN_THR_1 level is used(default) 2: LED_OPEN_THR_2 level is used 3: LED_OPEN_THR_3 level is used

Table 10.6.1-10: Register **LED_OPEN_SEL_20_23** (0XC8, page 2) LED open threshold level to LED channels 12 to 15 assignment configuration value

Bit	Name	Default	Access	Description
9:8	-	0	R	
7:6	Led23	1	R/W	OPEN level selection 0: OPEN detection disabled 1: LED_OPEN_THR_1 level is used(default) 2: LED_OPEN_THR_2 level is used 3: LED_OPEN_THR_3 level is used
5:4	Led22	1	R/W	OPEN level selection 0: OPEN detection disabled 1: LED_OPEN_THR_1 level is used(default) 2: LED_OPEN_THR_2 level is used 3: LED_OPEN_THR_3 level is used
3:2	Led21	1	R/W	OPEN level selection 0: OPEN detection disabled 1: LED_OPEN_THR_1 level is used(default) 2: LED_OPEN_THR_2 level is used 3: LED_OPEN_THR_3 level is used
1:0	Led20	1	R/W	OPEN level selection 0: OPEN detection disabled 1: LED_OPEN_THR_1 level is used(default) 2: LED_OPEN_THR_2 level is used 3: LED_OPEN_THR_3 level is used

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Table 10.6.1-11: Register **LED_SHORT_THR_1** (0XC9, page 2) LED short detection threshold level 1 configuration value

Bit	Name	Default	Access	Description
9:0	level	0X5C	R/W	LED SHORT detection threshold level [46 LSB/V], default value is 0X5C (2V) Note: SHORT condition detected if the difference between LED supply sample and LED pin voltage sample is smaller than the detection threshold level.

Table 10.6.1-12: Register **LED_SHORT_THR_2** (0XCA, page 2) LED short detection threshold level 2 configuration value

Bit	Name	Default	Access	Description
9:0	level	0	R/W	LED SHORT detection threshold level [46 LSB/V] Note: SHORT condition detected if the difference between LED supply sample and LED pin voltage sample is smaller than the detection threshold level.

Table 10.6.1-13: Register **LED_SHORT_THR_3** (0XCB, page 2) LED short detection threshold level 3 configuration value

Bit	Name	Default	Access	Description
9:0	level	0	R/W	LED SHORT detection threshold level [46 LSB/V] Note: SHORT condition detected if the difference between LED supply sample and LED pin voltage sample is smaller than the detection threshold level.

Table 10.6.1-14: Register **LED_SHORT_SEL_0_3** (0XCC, page 2) LED short threshold level to LED channels 0 to 3 assignment configuration value

Bit	Name	Default	Access	Description
9:8	-	0	R	
7:6	led3	1	R/W	SHORT level selection 0: SHORT detection disabled 1: LED_SHORT_THR_1 level is used(default) 2: LED_SHORT_THR_2 level is used 3: LED_SHORT_THR_3 level is used
5:4	led2	1	R/W	SHORT level selection 0: SHORT detection disabled 1: LED_SHORT_THR_1 level is used(default) 2: LED_SHORT_THR_2 level is used 3: LED_SHORT_THR_3 level is used
3:2	led1	1	R/W	SHORT level selection 0: SHORT detection disabled 1: LED_SHORT_THR_1 level is used(default) 2: LED_SHORT_THR_2 level is used 3: LED_SHORT_THR_3 level is used
1:0	led0	1	R/W	SHORT level selection 0: SHORT detection disabled 1: LED_SHORT_THR_1 level is used(default) 2: LED_SHORT_THR_2 level is used 3: LED_SHORT_THR_3 level is used

Table 10.6.1-15: Register **LED_SHORT_SEL_4_7** (0XCD, page 2) LED short threshold level to LED channels 4 to 7 assignment configuration value

Bit	Name	Default	Access	Description
9:8	-	0	R	
7:6	led7	1	R/W	SHORT level selection 0: SHORT detection disabled 1: LED_SHORT_THR_1 level is used(default) 2: LED_SHORT_THR_2 level is used 3: LED_SHORT_THR_3 level is used

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5:4	led6	1	R/W	SHORT level selection 0: SHORT detection disabled 1: LED_SHORT_THR_1 level is used(default) 2: LED_SHORT_THR_2 level is used 3: LED_SHORT_THR_3 level is used
3:2	led5	1	R/W	SHORT level selection 0: SHORT detection disabled 1: LED_SHORT_THR_1 level is used(default) 2: LED_SHORT_THR_2 level is used 3: LED_SHORT_THR_3 level is used
1:0	led4	1	R/W	SHORT level selection 0: SHORT detection disabled 1: LED_SHORT_THR_1 level is used(default) 2: LED_SHORT_THR_2 level is used 3: LED_SHORT_THR_3 level is used

Table 10.6.1-16: Register **LED_SHORT_SEL_8_11** (0XCE, page 2) LED short threshold level to LED channels 8 to 11 assignment configuration value

Bit	Name	Default	Access	Description
9:8	-	0	R	
7:6	led11	1	R/W	SHORT level selection 0: SHORT detection disabled 1: LED_SHORT_THR_1 level is used(default) 2: LED_SHORT_THR_2 level is used 3: LED_SHORT_THR_3 level is used
5:4	led10	1	R/W	SHORT level selection 0: SHORT detection disabled 1: LED_SHORT_THR_1 level is used(default) 2: LED_SHORT_THR_2 level is used 3: LED_SHORT_THR_3 level is used
3:2	led9	1	R/W	SHORT level selection 0: SHORT detection disabled 1: LED_SHORT_THR_1 level is used(default) 2: LED_SHORT_THR_2 level is used 3: LED_SHORT_THR_3 level is used
1:0	led8	1	R/W	SHORT level selection 0: SHORT detection disabled 1: LED_SHORT_THR_1 level is used(default) 2: LED_SHORT_THR_2 level is used 3: LED_SHORT_THR_3 level is used

Table 10.6.1-17: Register **LED_SHORT_SEL_12_15** (0XCF, page 2) LED short threshold level to LED channels 12 to 15 assignment configuration value

Bit	Name	Default	Access	Description
9:8	-	0	R	
7:6	led15	1	R/W	SHORT level selection 0: SHORT detection disabled 1: LED_SHORT_THR_1 level is used(default) 2: LED_SHORT_THR_2 level is used 3: LED_SHORT_THR_3 level is used
5:4	led14	1	R/W	SHORT level selection 0: SHORT detection disabled 1: LED_SHORT_THR_1 level is used(default) 2: LED_SHORT_THR_2 level is used 3: LED_SHORT_THR_3 level is used

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3:2	led13	1	R/W	SHORT level selection 0: SHORT detection disabled 1: LED_SHORT_THR_1 level is used(default) 2: LED_SHORT_THR_2 level is used 3: LED_SHORT_THR_3 level is used
1:0	led12	1	R/W	SHORT level selection 0: SHORT detection disabled 1: LED_SHORT_THR_1 level is used(default) 2: LED_SHORT_THR_2 level is used 3: LED_SHORT_THR_3 level is used

Table 10.6.1-18: Register **LED_SHORT_SEL_16_19** (0XD0, page 2) LED short threshold level to LED channels 16 to 19 assignment configuration value

Bit	Name	Default	Access	Description
9:8	-	0	R	
7:6	led19	1	R/W	SHORT level selection 0: SHORT detection disabled 1: LED_SHORT_THR_1 level is used(default) 2: LED_SHORT_THR_2 level is used 3: LED_SHORT_THR_3 level is used
5:4	led18	1	R/W	SHORT level selection 0: SHORT detection disabled 1: LED_SHORT_THR_1 level is used(default) 2: LED_SHORT_THR_2 level is used 3: LED_SHORT_THR_3 level is used
3:2	led17	1	R/W	SHORT level selection 0: SHORT detection disabled 1: LED_SHORT_THR_1 level is used(default) 2: LED_SHORT_THR_2 level is used 3: LED_SHORT_THR_3 level is used
1:0	led16	1	R/W	SHORT level selection 0: SHORT detection disabled 1: LED_SHORT_THR_1 level is used(default) 2: LED_SHORT_THR_2 level is used 3: LED_SHORT_THR_3 level is used

Table 10.6.1-19: Register **LED_SHORT_SEL_20_23** (0XD1, page 2) LED short threshold level to LED channels 20 to 23 assignment configuration value

Bit	Name	Default	Access	Description
9:8	-	0	R	
7:6	Led23	1	R/W	SHORT level selection 0: SHORT detection disabled 1: LED_SHORT_THR_1 level is used(default) 2: LED_SHORT_THR_2 level is used 3: LED_SHORT_THR_3 level is used
5:4	Led22	1	R/W	SHORT level selection 0: SHORT detection disabled 1: LED_SHORT_THR_1 level is used(default) 2: LED_SHORT_THR_2 level is used 3: LED_SHORT_THR_3 level is used
3:2	Led21	1	R/W	SHORT level selection 0: SHORT detection disabled 1: LED_SHORT_THR_1 level is used(default) 2: LED_SHORT_THR_2 level is used 3: LED_SHORT_THR_3 level is used

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1:0	Led20	1	R/W	SHORT level selection 0: SHORT detection disabled 1: LED_SHORT_THR_1 level is used(default) 2: LED_SHORT_THR_2 level is used 3: LED_SHORT_THR_3 level is used

Table 10.6.1-20: Register **VS_TOO_LOW** (0XD3, page 2) VS too low watch configuration value

Bit	Name	Default	Access	Description
9:0	level	0	R/W	When the ADC result of VS measurement is lower than [23 LSB/V], a "VS too low" will be signaled. Note: LED open and short evaluation of all LED channels will be disabled in case of "VS too low". Note: A level value of 0 disables VS value evaluation for " VS too low ".

Table 10.6.1-21: Register **VS_CRITICAL** (0XD4, page 2) VS too high watch configuration value

Bit	Name	Default	Access	Description
9:0	level	0	R/W	When the ADC result of VS measurement is higher than [46 LSB/V], a "VS critical" will be signaled. Note: A level value of 0 disables VS value evaluation for "VS critical".

Table 10.6.1-22: Register **VT_CRITICAL** (0XD5, page 2) VT too high watch configuration value

Bit	Name	Default	Access	Description
9:0	level	0	R/W	When the ADC result of VT measurement is higher than this [1 LSB/K], a "VT critical" will be signaled. Note: A level value of 0 disables VT value evaluation for "VT critical".

Table 10.6.1-23: Register **EBIN_MIN_THR** (0XD6, page 2) EBIN minimum voltage for EBIN short-to-GND protection

Bit	Name	Default	Access	Description
9:0	level	0	R/W	When the ADC result of EBIN measurement is lower than this [460 LSB/V], an EBIN_err or ADDR0_err will be signaled. Note: A level value of 0 disables evaluation for EBIN/ADDR0 error protection.

Table 10.6.1-24: Register **EBIN_ADDR0_MAX_THR** (0XD7, page 2) EBIN maximum voltage for EBIN open protection

Bit	Name	Default	Access	Description
9:0	level	0	R/W	When the ADC result of EBIN measurement is higher than this [460 LSB/V], an EBIN_err will be signaled. Note: A level value of 0 disables evaluation for EBIN error protection.

Table 10.6.1-25: Register **DIAG_CONFIG** (0XD8, page 2) Set single lamp or multi-lamp for diagnosis behavior. Set the error filter counter.

Bit	Name	Default	Access	Description
9	slm1	0	R/W	diagnosis group 1 single lamp mode selection 0: multi-lamp-mode (MLM) 1: single-lamp-mode (SLM)
8	slm0	0	R/W	diagnosis group 0 single lamp mode selection 0: multi-lamp-mode (MLM) 1: single-lamp-mode (SLM)
7:5	-	0	R	
4:0	level	0X3	R/W	DIAG counter level (default value 3) DIAG error counter level which has to be reached before

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				asserting a diagnosis error Note: If level is 0, the filter will block all diagnosis events received from the measurement system and its output will not show diagnosis errors. Set level to at least 1 to enable the filter.

Table 10.6.1-26: Register **DIAG0_CONFIG_0_7** (0XD9, page 2) diagnosis group 0 configuration for LED channels 0 to 7

Bit	Name	Default	Access	Description
9:8	-	0	R	
7:0	enable	0	R/W	DIAG0 diagnosis enable for driver channels 0 to 7

Table 10.6.1-27: Register **DIAG0_CONFIG_8_15** (0XDA, page 2) diagnosis group 0 configuration for LED channels 8 to 15

Bit	Name	Default	Access	Description
9:8	-	0	R	
7:0	enable	0	R/W	DIAG0 diagnosis enable for driver channels 8 to 15

Table 10.6.1-28: Register **DIAG0_CONFIG_16_23** (0XDB, page 2) diagnosis group 0 configuration for LED channels 16 to 23

Bit	Name	Default	Access	Description
9:8	-	0	R	
7:0	enable	0	R/W	DIAG0 diagnosis enable for driver channels 16 to 23

Table 10.6.1-29: Register **DIAG1_CONFIG_0_7** (0XDC, page 2) diagnosis group 1 configuration for LED channels 0 to 7

Bit	Name	Default	Access	Description
9:8	-	0	R	
7:0	enable	0	R/W	DIAG1 diagnosis enable for driver channels 0 to 7

Table 10.6.1-30: Register **DIAG1_CONFIG_8_15** (0XDD, page 2) diagnosis group 1 configuration for LED channels 8 to 15

Bit	Name	Default	Access	Description
9:8	-	0	R	
7:0	enable	0	R/W	DIAG1 diagnosis enable for driver channels 8 to 15

Table 10.6.1-31: Register **DIAG1_CONFIG_16_23** (0XDE, page 2) diagnosis group 1 configuration for LED channels 16 to 23

Bit	Name	Default	Access	Description
9:8	-	0	R	
7:0	enable	0	R/W	DIAG1 diagnosis enable for driver channels 16 to 23

10.6.2 Bus Config Area

Table 10.6.2-1: BUS_CONFIG

Register Name	Address	Description
ASSERT_DIAG	0X38	DIAG pin assertion via bus

Table 10.6.2-2: Register **ASSERT_DIAG** (0X38) DIAG pin assertion via bus

Bit	Name	Default	Access	Description
9:4	pass	0	R/W	write password This bitfield has to be written as 0x26 to enable the evaluation of bits 0 to 3, otherwise the written value will be ignored.
3	mask_diag1_in	0	R/W	0: DIAG1 pin input path behaves like set up by STANDALONE configuration 1: DIAG1 pin input path disabled

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2	mask_diag0_in	0	R/W	0: DIAG0 pin input path behaves like set up by STANDALONE configuration 1: DIAG0 pin input path disabled
1	assert_diag1	0	R/W	0: device internal DIAG pin functionality only 1: DIAG1 pin is asserted
0	assert_diag0	0	R/W	0: device internal DIAG pin functionality only 1: DIAG0 pin is asserted

Table 10.6.3-1: BUS_STATUS

Register Name	Address	Description
RESULT_VDIF_0	0X80	The ADC measurement result of LED0 related external load voltage drop value
RESULT_VDIF_1	0X81	The ADC measurement result of LED1 related external load voltage drop value
RESULT_VDIF_2	0X82	The ADC measurement result of LED2 related external load voltage drop value
RESULT_VDIF_3	0X83	The ADC measurement result of LED3 related external load voltage drop value
RESULT_VDIF_4	0X84	The ADC measurement result of LED4 related external load voltage drop value
RESULT_VDIF_5	0X85	The ADC measurement result of LED5 related external load voltage drop value
RESULT_VDIF_6	0X86	The ADC measurement result of LED6 related external load voltage drop value
RESULT_VDIF_7	0X87	The ADC measurement result of LED7 related external load voltage drop value
RESULT_VDIF_8	0X88	The ADC measurement result of LED8 related external load voltage drop value
RESULT_VDIF_9	0X89	The ADC measurement result of LED9 related external load voltage drop value
RESULT_VDIF_10	0X8A	The ADC measurement result of LED10 related external load voltage drop value
RESULT_VDIF_11	0X8B	The ADC measurement result of LED11 related external load voltage drop value
RESULT_VDIF_12	0X8C	The ADC measurement result of LED12 related external load voltage drop value
RESULT_VDIF_13	0X8D	The ADC measurement result of LED13 related external load voltage drop value
RESULT_VDIF_14	0X8E	The ADC measurement result of LED14 related external load voltage drop value
RESULT_VDIF_15	0X8F	The ADC measurement result of LED15 related external load voltage drop value
RESULT_VDIF_16	0X90	The ADC measurement result of LED16 related external load voltage drop value
RESULT_VDIF_17	0X91	The ADC measurement result of LED17 related external load voltage drop value
RESULT_VDIF_18	0X92	The ADC measurement result of LED18 related external load voltage drop value
RESULT_VDIF_19	0X93	The ADC measurement result of LED19 related external load voltage drop value
RESULT_VDIF_20	0X94	The ADC measurement result of LED20 related external load voltage drop value
RESULT_VDIF_21	0X95	The ADC measurement result of LED21 related external load voltage drop value
RESULT_VDIF_22	0X96	The ADC measurement result of LED22 related external load voltage drop value

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RESULT_VDIF_23	0X97	The ADC measurement result of LED23 related external load voltage drop value
RESULT_VLED_0	0X98	LED0 voltage ADC measurement result value
RESULT_VLED_1	0X99	LED1 voltage ADC measurement result value
RESULT_VLED_2	0X9A	LED2 voltage ADC measurement result value
RESULT_VLED_3	0X9B	LED3 voltage ADC measurement result value
RESULT_VLED_4	0X9C	LED4 voltage ADC measurement result value
RESULT_VLED_5	0X9D	LED5 voltage ADC measurement result value
RESULT_VLED_6	0X9E	LED6 voltage ADC measurement result value
RESULT_VLED_7	0X9F	LED7 voltage ADC measurement result value
RESULT_VLED_8	0XA0	LED8 voltage ADC measurement result value
RESULT_VLED_9	0XA1	LED9 voltage ADC measurement result value
RESULT_VLED_10	0XA2	LED10 voltage ADC measurement result value
RESULT_VLED_11	0XA3	LED11 voltage ADC measurement result value
RESULT_VLED_12	0XA4	LED12 voltage ADC measurement result value
RESULT_VLED_13	0XA5	LED13 voltage ADC measurement result value
RESULT_VLED_14	0XA6	LED14 voltage ADC measurement result value
RESULT_VLED_15	0XA7	LED15 voltage ADC measurement result value
RESULT_VLED_16	0XA8	LED16 voltage ADC measurement result value
RESULT_VLED_17	0XA9	LED17 voltage ADC measurement result value
RESULT_VLED_18	0XAA	LED18 voltage ADC measurement result value
RESULT_VLED_19	0XAB	LED19 voltage ADC measurement result value
RESULT_VLED_20	0XAC	LED20 voltage ADC measurement result value
RESULT_VLED_21	0XAD	LED21 voltage ADC measurement result value
RESULT_VLED_22	0XAE	LED22 voltage ADC measurement result value
RESULT_VLED_23	0XAF	LED230 voltage ADC measurement result value
RESULT_VT	0XB0	device temperature ADC measurement result value
RESULT_VDD5	0XB2	VDD5 voltage ADC measurement result value
RESULT_VSUP	0XB3	VS voltage ADC measurement result value
LED_OPEN_0_7	0XB4	LED channels 0 to 7 open detection status value
LED_OPEN_8_15	0XB5	LED channels 8 to 15 open detection status value
LED_OPEN_16_23	0XB6	LED channels 16 to 23 open detection status value
LED_SHORT_0_7	0XB7	LED channels 0 to 7 short detection status value
LED_SHORT_8_15	0XB8	LED channels 8 to 15 short detection status value
LED_SHORT_16_23	0XB9	LED channels 16 to 23 short detection status value
EVENT_STATUS	0XBA	device events status value
EVENT_STATUS2	0XBB	device events status value
PWMIN_STATUS	0XBC	IO interface state value
DIAG_STATUS	0XBD	diagnosis groups status

Table 10.6.3-2: Register **RESULT_VDIF_0** (0X80) the ADC measurement result of VS-LED0 voltage drop value

Bit	Name	Default	Access	Description
9:0	data	0	R	LED drop voltage ADC result data value [46 LSB/V]

Table 10.6.3-3: Register **RESULT_VDIF _1** (0X81) the ADC measurement result of VS-LED1 voltage drop value

Bit	Name	Default	Access	Description
9:0	data	0	R	LED drop voltage ADC result data value [46 LSB/V]

Table 10.6.3-4: Register **RESULT_ VDIF _2** (0X82) the ADC measurement result of VS-LED2 voltage drop value

Bit	Name	Default	Access	Description
9:0	data	0	R	LED drop voltage ADC result data value [46 LSB/V]

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Table 10.6.3-5: Register **RESULT_ VDIF _3** (0X83) the ADC measurement result of VS-LED3 voltage drop value

Bit	Name	Default	Access	Description
9:0	data	0	R	LED drop voltage ADC result data value [46 LSB/V]

Table 10.6.3-6: Register **RESULT_ VDIF _4** (0X84) the ADC measurement result of VS-LED4 voltage drop value

Bit	Name	Default	Access	Description
9:0	data	0	R	LED drop voltage ADC result data value [46 LSB/V]

Table 10.6.3-7: Register **RESULT_ VDIF _5** (0X85) the ADC measurement result of VS-LED5 voltage drop value

Bit	Name	Default	Access	Description
9:0	data	0	R	LED drop voltage ADC result data value [46 LSB/V]

Table 10.6.3-8: Register **RESULT_ VDIF _6** (0X86) the ADC measurement result of VS-LED6 voltage drop value

Bit	Name	Default	Access	Description
9:0	data	0	R	LED drop voltage ADC result data value [46 LSB/V]

Table 10.6.3-9: Register **RESULT_ VDIF _7** (0X87) the ADC measurement result of VS-LED7 voltage drop value

Bit	Name	Default	Access	Description
9:0	data	0	R	LED drop voltage ADC result data value [46 LSB/V]

Table 10.6.3-10: Register **RESULT_ VDIF _8** (0X88) the ADC measurement result of VS-LED8 voltage drop value

Bit	Name	Default	Access	Description
9:0	data	0	R	LED drop voltage ADC result data value [46 LSB/V]

Table 10.6.3-11: Register **RESULT_ VDIF _9** (0X89) the ADC measurement result of VS-LED9 voltage drop value

Bit	Name	Default	Access	Description
9:0	data	0	R	LED drop voltage ADC result data value [46 LSB/V]

Table 10.6.3-12: Register **RESULT_ VDIF _10** (0X8A) the ADC measurement result of VS-LED10 voltage drop value

Bit	Name	Default	Access	Description
9:0	data	0	R	LED drop voltage ADC result data value [46 LSB/V]

Table 10.6.3-13: Register **RESULT_ VDIF _11** (0X8B) the ADC measurement result of VS-LED11 voltage drop value

Bit	Name	Default	Access	Description
9:0	data	0	R	LED drop voltage ADC result data value [46 LSB/V]

Table 10.6.3-14: Register **RESULT_ VDIF _12** (0X8C) the ADC measurement result of VS-LED12 voltage drop value

Bit	Name	Default	Access	Description
9:0	data	0	R	LED drop voltage ADC result data value [46 LSB/V]

Table 10.6.3-15: Register **RESULT_ VDIF _13** (0X8D) the ADC measurement result of VS-LED13 voltage drop value

Bit	Name	Default	Access	Description
9:0	data	0	R	LED drop voltage ADC result data value [46 LSB/V]

Table 10.6.3-16: Register **RESULT_ VDIF _14** (0X8E) the ADC measurement result of VS-LED14 voltage drop value

Bit	Name	Default	Access	Description
9:0	data	0	R	LED drop voltage ADC result data value [46 LSB/V]

Table 10.6.3-17: Register **RESULT_ VDIF _15** (0X8F) the ADC measurement result of VS-LED15 voltage drop value

Bit	Name	Default	Access	Description
9:0	data	0	R	LED drop voltage ADC result data value [46 LSB/V]

Table 10.6.3-18: Register **RESULT_ VDIF _16** (0X90) the ADC measurement result of VS-LED16 voltage drop value

Bit	Name	Default	Access	Description

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9:0	data	0	R	LED drop voltage ADC result data value [46 LSB/V]

Table 10.6.3-19: Register **RESULT_ VDIF _17** (0X91) the ADC measurement result of VS-LED17 voltage drop value

Bit	Name	Default	Access	Description
9:0	data	0	R	LED drop voltage ADC result data value [46 LSB/V]

Table 10.6.3-20: Register **RESULT_ VDIF _18** (0X92) the ADC measurement result of VS-LED18 voltage drop value

Bit	Name	Default	Access	Description
9:0	data	0	R	LED drop voltage ADC result data value [46 LSB/V]

Table 10.6.3-21: Register **RESULT_ VDIF _19** (0X93) the ADC measurement result of VS-LED19 voltage drop value

Bit	Name	Default	Access	Description
9:0	data	0	R	LED drop voltage ADC result data value [46 LSB/V]

Table 10.6.3-22: Register **RESULT_ VDIF _20** (0X94) the ADC measurement result of VS-LED20 voltage drop value

Bit	Name	Default	Access	Description
9:0	data	0	R	LED drop voltage ADC result data value [46 LSB/V]

Table 10.6.3-23: Register **RESULT_ VDIF _21** (0X95) the ADC measurement result of VS-LED21 voltage drop value

Bit	Name	Default	Access	Description
9:0	data	0	R	LED drop voltage ADC result data value [46 LSB/V]

Table 10.6.3-24: Register **RESULT_ VDIF _22** (0X96) the ADC measurement result of VS-LED22 voltage drop value

Bit	Name	Default	Access	Description
9:0	data	0	R	LED drop voltage ADC result data value [46 LSB/V]

Table 10.6.3-25: Register **RESULT_ VDIF _23** (0X97) the ADC measurement result of VS-LED23 voltage drop value

Bit	Name	Default	Access	Description
9:0	data	0	R	LED drop voltage ADC result data value [46 LSB/V]

Table 10.6.3-26: Register **RESULT_VLED_0** (0X98) LED0 voltage ADC measurement result value

Bit	Name	Default	Access	Description
9:0	data	0	R	LED pin voltage ADC result data value [46 LSB/V]

Table 10.6.3-27: Register **RESULT_VLED_1** (0X99) LED1 voltage ADC measurement result value

Bit	Name	Default	Access	Description
9:0	data	0	R	LED pin voltage ADC result data value [46 LSB/V]

Table 10.6.3-28: Register **RESULT_VLED_2** (0X9A) LED2 voltage ADC measurement result value

Bit	Name	Default	Access	Description
9:0	data	0	R	LED pin voltage ADC result data value [46 LSB/V]

Table 10.6.3-29: Register **RESULT_VLED_3** (0X9B) LED3 voltage ADC measurement result value

Bit	Name	Default	Access	Description
9:0	data	0	R	LED pin voltage ADC result data value [46 LSB/V]

Table 10.6.3-30: Register **RESULT_VLED_4** (0X9C) LED4 voltage ADC measurement result value

Bit	Name	Default	Access	Description
9:0	data	0	R	LED pin voltage ADC result data value [46 LSB/V]

Table 10.6.3-31: Register **RESULT_VLED_5** (0X9D) LED5 voltage ADC measurement result value

Bit	Name	Default	Access	Description
9:0	data	0	R	LED pin voltage ADC result data value [46 LSB/V]

Table 10.6.3-32: Register **RESULT_VLED_6** (0X9E) LED6 voltage ADC measurement result value

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Bit	Name	Default	Access	Description
9:0	data	0	R	LED pin voltage ADC result data value [46 LSB/V]

Table 10.6.3-33: Register **RESULT_VLED_7** (0X9F) LED7 voltage ADC measurement result value

Bit	Name	Default	Access	Description
9:0	data	0	R	LED pin voltage ADC result data value [46 LSB/V]

Table 10.6.3-34: Register **RESULT_VLED_8** (0XA0) LED8 voltage ADC measurement result value

Bit	Name	Default	Access	Description
9:0	data	0	R	LED pin voltage ADC result data value [46 LSB/V]

Table 10.6.3-35: Register **RESULT_VLED_9** (0XA1) LED9 voltage ADC measurement result value

Bit	Name	Default	Access	Description
9:0	data	0	R	LED pin voltage ADC result data value [46 LSB/V]

Table 10.6.3-36: Register **RESULT_VLED_10** (0XA2) LED10 voltage ADC measurement result value

Bit	Name	Default	Access	Description
9:0	data	0	R	LED pin voltage ADC result data value [46 LSB/V]

Table 10.6.3-37: Register **RESULT_VLED_11** (0XA3) LED11 voltage ADC measurement result value

Bit	Name	Default	Access	Description
9:0	data	0	R	LED pin voltage ADC result data value [46 LSB/V]

Table 10.6.3-38: Register **RESULT_VLED_12** (0XA4) LED12 voltage ADC measurement result value

Bit	Name	Default	Access	Description
9:0	data	0	R	LED pin voltage ADC result data value [46 LSB/V]

Table 10.6.3-39egister **RESULT_VLED_13** (0XA5) LED13 voltage ADC measurement result value

Bit	Name	Default	Access	Description
9:0	data	0	R	LED pin voltage ADC result data value [46 LSB/V]

Table 10.6.3-40: Register **RESULT_VLED_14** (0XA6) LED14 voltage ADC measurement result value

Bit	Name	Default	Access	Description
9:0	data	0	R	LED pin voltage ADC result data value [46 LSB/V]

Table 10.6.3-41Register **RESULT_VLED_15** (0XA7) LED15 voltage ADC measurement result value

Bit	Name	Default	Access	Description
9:0	data	0	R	LED pin voltage ADC result data value [46 LSB/V]

Table 10.6.3-42 Register **RESULT_VLED_16** (0XA8) LED16 voltage ADC measurement result value

Bit	Name	Default	Access	Description
9:0	data	0	R	LED pin voltage ADC result data value [46 LSB/V]

Table 10.6.3-43: Register **RESULT_VLED_17** (0XA9) LED17 voltage ADC measurement result value

Bit	Name	Default	Access	Description
9:0	data	0	R	LED pin voltage ADC result data value [46 LSB/V]

Table 10.6.3-44 Register **RESULT_VLED_18** (0XAA) LED18 voltage ADC measurement result value

Bit	Name	Default	Access	Description
9:0	data	0	R	LED pin voltage ADC result data value [46 LSB/V]

Table 10.6.3-45Register **RESULT_VLED_19** (0XAB) LED19 voltage ADC measurement result value

Bit	Name	Default	Access	Description
9:0	data	0	R	LED pin voltage ADC result data value [46 LSB/V]

Table 10.6.3-46 Register **RESULT_VLED_20** (0xAC) LED20 voltage ADC measurement result value

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Bit	Name	Default	Access	Description
9:0	data	0	R	LED pin voltage ADC result data value [46 LSB/V]

Table 10.6.3-47 Register **RESULT_VLED_21** (0xAD) LED21 voltage ADC measurement result value

Bit	Name	Default	Access	Description
9:0	data	0	R	LED pin voltage ADC result data value [46 LSB/V]

Table 10.6.3-48 Register **RESULT_VLED_22** (0xAE) LED22 voltage ADC measurement result value

Bit	Name	Default	Access	Description
9:0	data	0	R	LED pin voltage ADC result data value [46 LSB/V]

Table 10.6.3-49 Register **RESULT_VLED_23** (0xAF) LED23 voltage ADC measurement result value

Bit	Name	Default	Access	Description
9:0	data	0	R	LED pin voltage ADC result data value [46 LSB/V]

Table 10.6.3-50: Register **RESULT_VT** (0XB0) device temperature ADC measurement result value

Bit	Name	Default	Access	Description
9:0	data	0	R	VT (temperature) ADC channel result data value in Kelvin [1LSB/K] Example: T = 25°C -> data = 273 + 25 = 298

Table 10.6.3-51: Register **RESULT_VDD5** (0XB2) VDD5 voltage ADC measurement result value

Bit	Name	Default	Access	Description
9:0	data	0	R	VDD5 voltage ADC measurement result value [184 LSB/V]

Table 10.6.3-52: Register **RESULT_VSUP** (0XB3) VS voltage ADC measurement result value

Bit	Name	Default	Access	Description
9:0	data	0	R	VS voltage ADC measurement result value [46 LSB/V]

Table 10.6.3-53: Register **LED_OPEN_0_7** (0XB4) LED channels 0 to 7 open detection status value

Bit	Name	Default	Access	Description
9:8	-	0	R	
7:0	status	0	R	LED channels 0 to 7 OPEN status

Table 10.6.3-54: Register **LED_OPEN_8_15** (0XB5) LED channels 8 to 15 open detection status value

Bit	Name	Default	Access	Description
9:8	-	0	R	
7:0	status	0	R	LED channels 8 to 15 OPEN status

Table 10.6.3-55: Register **LED_OPEN_16_23** (0XB6) LED channels 16 to 23 open detection status value

Bit	Name	Default	Access	Description
9:8	-	0	R	
7:0	status	0	R	LED channels 16 to 23 OPEN status

Table 10.6.3-56: Register **LED_SHORT_0_7** (0XB7) LED channels 0 to 7 short detection status value

Bit	Name	Default	Access	Description
9:8	-	0	R	
7:0	status	0	R	LED channels 0 to 7 SHORT status

Table 10.6.3-57: Register **LED_SHORT_8_15** (0XB8) LED channels 8 to 15 short detection status value

Bit	Name	Default	Access	Description
9:8	-	0	R	
7:0	status	0	R	LED channels 8 to 15 SHORT status

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Table 10.6.3-58: Register **LED_SHORT_16_23** (0XB9) LED channels 16 to 23 short detection status value

Bit	Name	Default	Access	Description
9:8	-	0	R	
7:0	status	0	R	LED channels 16 to 23 SHORT status

Table 10.6.3-59: Register **EVENT_STATUS** (0XBA) device events status value

Bit	Name	Default	Access	Description
9	-	0	R	
8	bus_crc_error	0	R	communication CRC error flag
7	led_open	0	R	LED open condition flag
6	led_short	0	R	LED short condition flag
5	vt_too_high	0	R	critical temperature (too high) flag
4	vs_too_high	0	R	critical VS (too high) flag
3	vs_too_low	0	R	VS too low flag
2	derating	0	R	LED current derating active flag
1	timeout	0	R	communication timeout flag
0	reset	1	R	reset flag

Table 10.6.3-60: Register **EVENT_STATUS2** (0XBB) device events status value

Bit	Name	Default	Access	Description
9:6	-	0	R	
5:4	bist_err	0	R	the BIST result of MTPs bit [4]=1: MTP0 err bit [5]=1: MTP1 err
3	vtofs err	0	R	vtofs short to GND error flag
2	channel_short	0	R	channel short to GND flag
1	-	0	R	
0	ebin_err	0	R	EBIN error flag

Table 10.6.3-61: Register **PWMIN_STATUS** (0XBC) IO interface state value

Bit	Name	Default	Access	Description
9	oe_state	0	R	OE pin state
8	prog_state	0	R	PROG pin state
7	addr1_state	0	R	ADDR1 pin state
6	addr2/pwm_state	0	R	ADDR2/PWM pin state
5:4	-	0	R	
3	PWM_state_direct	0	R	PWM evaluated state is "direct PWM state"
2	-	0	R	
1	PWM_state_bus	1	R	PWM evaluated state is "bus state"
0	-	1	R	

Table 10.6.3-62: Register **DIAG_STATUS** (0XBD) diagnosis groups status

Bit	Name	Default	Access	Description
9:4	-	0	R	
3	diag1_buf	0	R	DIAG1 buf state 1: if DIAG1 pin is 0
2	diag0_buf	0	R	DIAG0 buf state 1: if DIAG0 pin is 0
1	diag1_out	0	R	DIAG1 internal (outgoing) state 1: if an LED of device diagnosis group 1 shows an error
0	diag0_out	0	R	DIAG0 internal (outgoing) state 1: if an LED of device diagnosis group 0 shows an error

Table 10.6.4-1: BUS_STATUS

Register Name	Register page	Address	Description

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RESULT_VEBIN	0	0XD8	EBIN voltage ADC measurement result value

Table 10.6.4-2: Register **RESULT_VEBIN** (0XD8, page 0) EBIN voltage ADC measurement result value

Bit	Name	Default	Access	Description
9:0	data	0	R	EBIN voltage ADC result data value [460 LSB/V]

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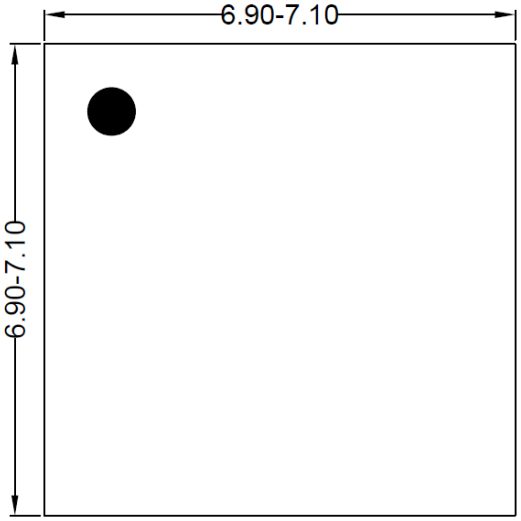
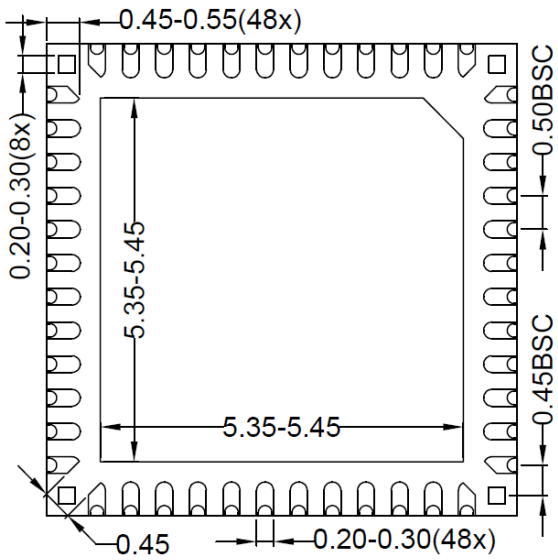
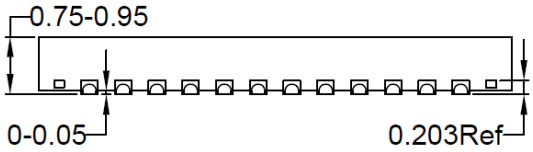
QFN7x7-48 Package Outline Drawing



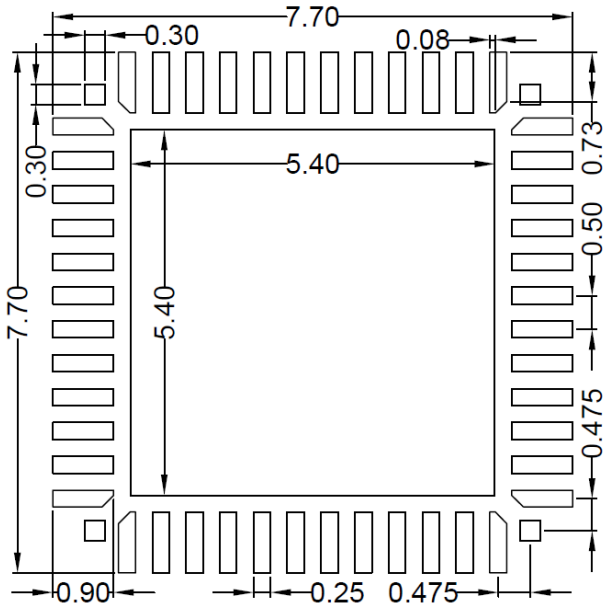
Top View



Bottom View



Front View



Recommended PCB Layout
(Reference only)

Notes：All dimension in millimeter and exclude mold flash & metal burr.

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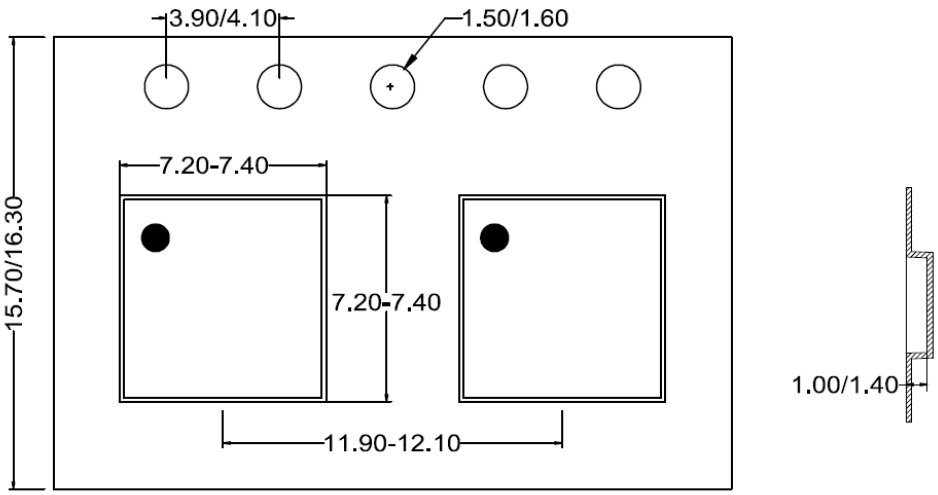
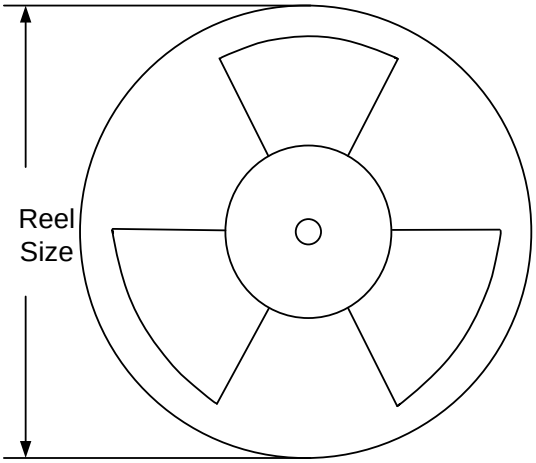
Tape and Reel Specification

Tape Orientation



Reel dimensions



Package types	Tape width (mm)	Pocket pitch(mm)	Reel size (Inch)	Trailer * length(mm)	Leader * length (mm)	Qty per reel (pcs)
QFN7x7	16	12	13"	400	400	3000

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Revision History

The revision history provided is for informational purpose only and is believed to be accurate, however, not warranted. Please make sure that you have the latest revision.

Date	Revision	Change
July 29,2025	Revision 1.0	Initial Release

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