SY7T213H
Electricity Metering SoCs for Polyphase Systems

General Description

The SY7T213H is a versatile electricity metering SoC for polyphase electricity meters and power monitoring systems, featuring Silergy's proprietary Teridian power measurement technology.

The part contains three dedicated ADCs (ADCS) for current measurement and one multiplexed ADC (ADCM) for phase voltages and neutral current. CTs or Rogowski coils can be used as current sensors, and shunts can be connected using up to three SY7M007 capacitively coupled remote interface ICs.

An embedded 64-bit Compute Engine (CE) operating at 20MHz performs computations, data formatting, and reporting of metrology parameters to the Cortex M0 core, which operates at 10MHz. With 256KB integrated flash memory for storing code, nonvolatile calibration coefficients and device configuration settings, the parts offer an autonomous metrology solution and can interface to a host processor through its SPI, UART, or I^2C ports.

The SY7T213H is available in a 100-pin LQFP package.

Applications

- Smart Meters and sub-meters
- Metrology front ends
- Building Automation Systems
- Inverters and Renewable Energy Systems
- Level 1 and 2 EV Charging Systems
- Grid-Friendly Appliances and Smart Plugs

Features

- Powerful 32-bit ARM Cortex M0 core, up to 10MHz clock
- 256KB of Flash memory with copy/debug protection
- 24KB RAM plus 4KB NV-RAM
- Dedicated 64-bit 20MHz Compute Engine (CE) core
- Optimized CE code image provided by Silergy, suitable for most metering applications and adaptable to specific applications
- Compatible with capacitively coupled isolated remote sensor ICs (SY7M007)
- 3.0V to 3.6V supply in Mission Mode
- 1µA current draw in Sleep Mode
- Brownout Mode including analog features functional with 2.5V V_{BAT} supply
- On-chip digital temperature sensor (±1°C)
- Configurable ADC sampling rate, up to 8kHz
- On-chip RTC with accurate 1-second pulse output
- ±0.1% Wh accuracy over 5,000:1 current range in CT mode
- Multiple wake sources for anti-tamper:
  - Wake on timer
  - Wake on edge at GPIO pins (4 GPIO wake pins)
  - Wake on UART receive signal (RX0, RX1)
  - Wake on voltage comparator event and reset
- Single 32kHz crystal provides all operating clocks
- Internal R/C backup oscillator
- Up to 63 LCD segment pins, up to 8 commons, 6 pages
- Up to 73 GPIO pins, all are interrupt-capable
- Two master SPI ports, one slave SPI port
- One independent I^2C port, one I^2C port shared with SPI pins
- Six UARTs
- Four PWM outputs, up to 2.5MHz, programmable duty cycle
- Two pulse generator outputs with programmable frequency and duty cycle for the optional supply of capacitively coupled isolated remote sensor ICs (SY7M007) via a transformer

9/2025

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Ordering Information

Ordering Number	Carrier Type	Temperature Range	Package	Flash Memory	Top Mark
SY7T213HBGEF	Bulk/Tray	-40°C to +85°C	100 LQFP	256KB	See page 32
SY7T213HGEF	Reel				

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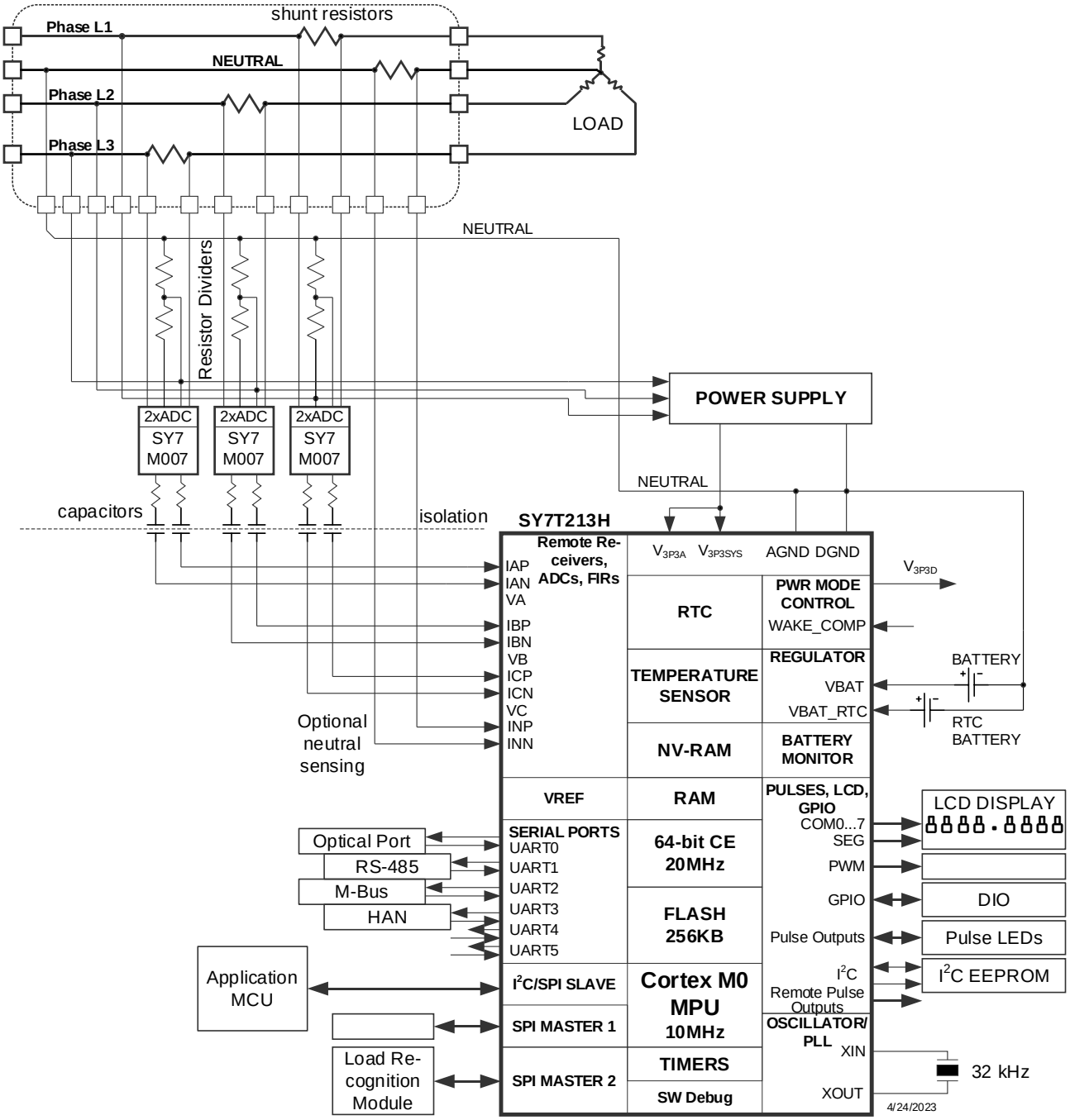
Typical Application Circuit (SY7T213H with Shunts and SY7M007 Remotes)



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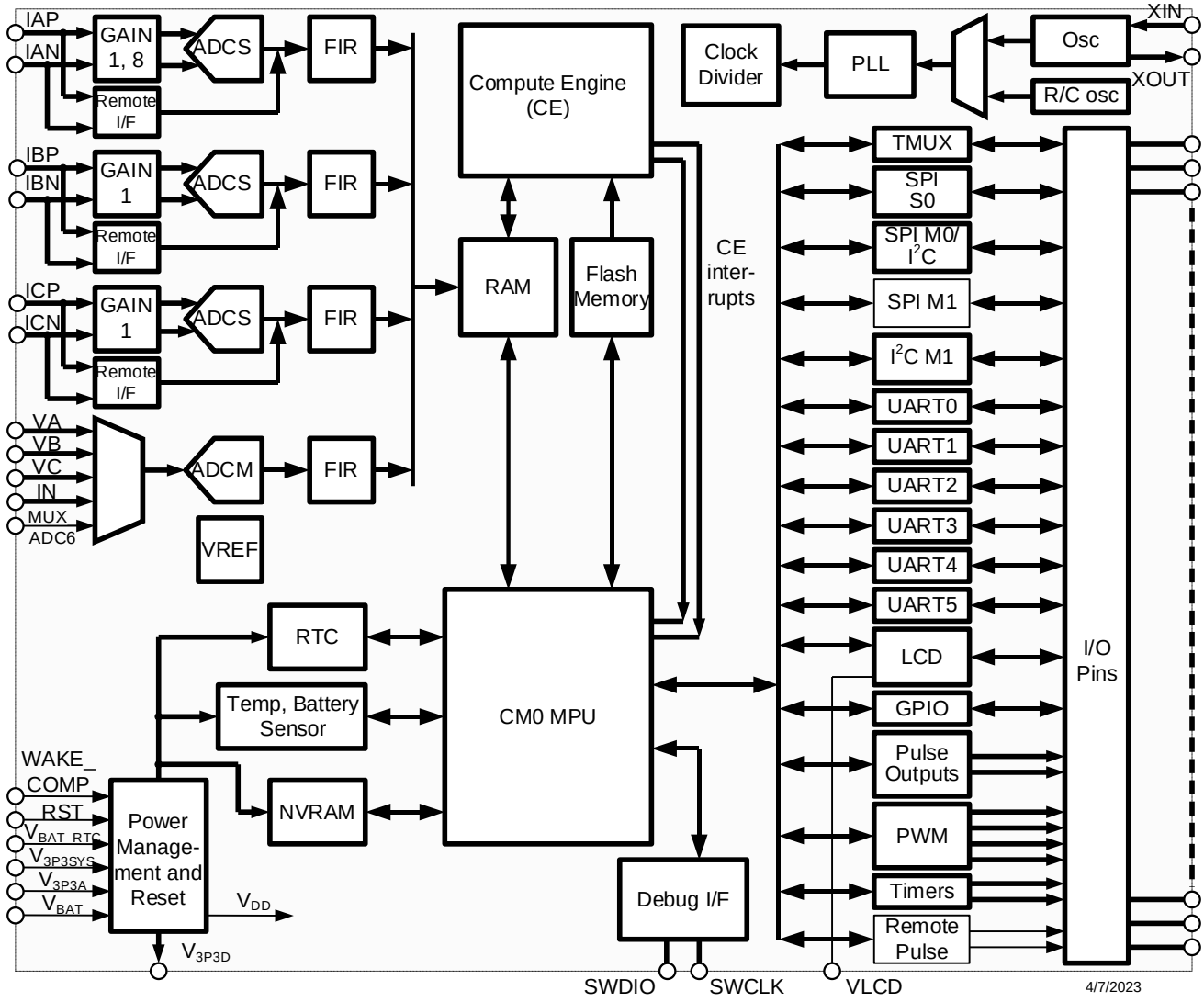
Block Diagram (SY7T213H)



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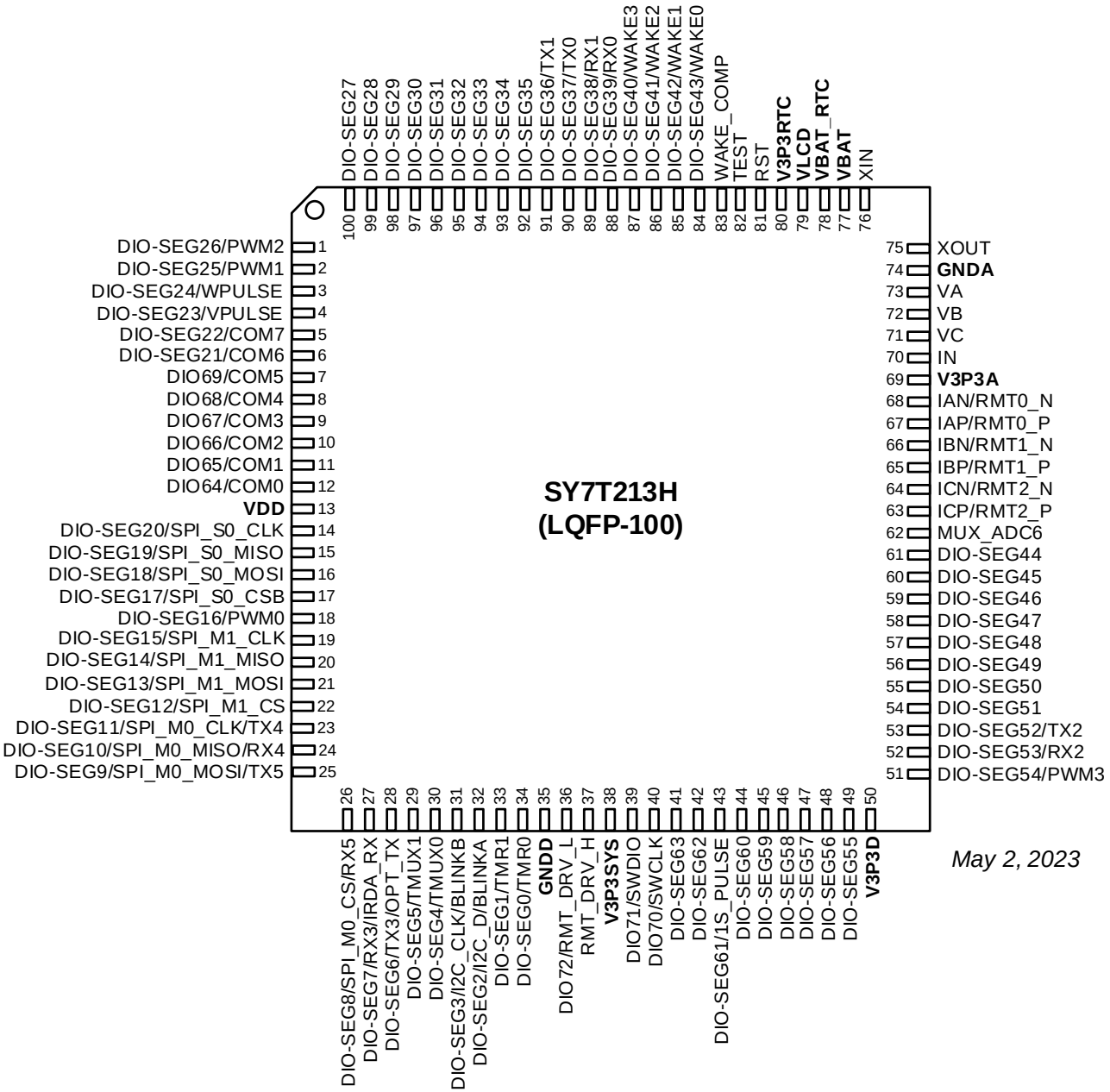
Pinout (SY7T213H, LQFP100, top view)



May 2, 2023

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Pin Description

Pin No.	Pin Name	Primary Function	Alt. Function 1	Alt. Function 2	Alt. Function 3
1	DIO-SEG26/PWM2	GPIO26	SEG26	PWM2	
2	DIO-SEG25/PWM1	GPIO25	SEG25	PWM1	
3	DIO-SEG24/WPULSE	GPIO24	SEG24	WPULSE	
4	DIO-SEG23/VPULSE	GPIO23	SEG23	VPULSE	
5	DIO-SEG22/COM7	GPIO22	SEG22	COM7	
6	DIO-SEG21/COM6	GPIO21	SEG21	COM6	
7	DIO69/COM5	GPIO69	COM5		
8	DIO68/COM4	GPIO68	COM4		
9	DIO67/COM3	GPIO67	COM3		
10	DIO66/COM2	GPIO66	COM2		
11	DIO65/COM1	GPIO65	COM1		
12	DIO64/COM0	GPIO64	COM0		
13	VDD. Bypass pin for internal voltage.				
14	DIO-SEG20/SPI_S0_CLK	GPIO20	SEG20	SPI_S0_ CLK	
15	DIO-SEG19/ SPI_S0_MISO	GPIO19	SEG19	SPI_S0_ MISO	
16	DIO-SEG18/ SPI_S0_MOSI	GPIO18	SEG18	SPI_S0_ MOSI	
17	DIO-SEG17/SPI_S0_CSB	GPIO17	SEG17	SPI_S0_ CSB	
18	DIO-SEG16/PWM0	GPIO16	SEG16	PWM0	
19	DIO-SEG15/ SPI_M1_CLK	GPIO15	SEG15	SPI_M1_ CLK	
20	DIO-SEG14/ SPI_M1_MISO	GPIO14	SEG14	SPI_M1_ MISO	
21	DIO-SEG13/ SPI_M1_MOSI	GPIO13	SEG13	SPI_M1_ MOSI	
22	DIO-SEG12/SPI_M1_CS	GPIO12	SEG12	SPI_M1_ CS	
23	DIO-SEG11/ SPI_M0_CLK/TX4	GPIO11	SEG11	SPI_M0_ CLK	TX4
24	DIO-SEG10/ SPI_M0_MISO/RX4	GPIO10	SEG10	SPI_M0_ MISO	RX4
25	DIO-SEG9/ SPI_M0_MOSI/TX5	GPIO9	SEG9	SPI_M0_ MOSI	TX5
26	DIO-SEG8/ SPI_M0_CS/RX5	GPIO8	SEG8	SPI_M0_CS	RX5
27	DIO-SEG7/RX3_OPT	GPIO7	SEG7	RX3	IrDA_RX
28	DIO-SEG6/TX3_OPT	GPIO6	SEG6	TX3	OPT_TX
29	DIO-SEG5/TMUX1	GPIO5	SEG5	TMUX1	
30	DIO-SEG4/TMUX0	GPIO4	SEG4	TMUX0	
31	DIO-SEG3/I2C_CLK/BLINKB	GPIO3	SEG3/BLINKB	I2C_CLK	
32	DIO-SEG2/I2C_CLK/BLINKA	GPIO2	SEG2/BLINKA	I2C_DATA	
33	DIO-SEG1/TMR1	GPIO1	SEG1	TMR1	
34	DIO-SEG0/TMR0	GPIO0	SEG0	TMR0	
35	GNDD. Digital ground.				
36	DIO72/RMT_DRIVE_L	DIO72	RMT_ DRIVE_L		
37	RMT_DRIVE_H	*Not for DIO use*	RMT_ DRIVE_H		
38	V3P3SYS. Digital supply voltage. This pin should be connected to the V3P3A pin (69).				
39	DIO71/SWDIO	GPIO71	SWDIO		

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Pin No.	Pin Name	Primary Function	Alt. Function 1	Alt. Function 2	Alt. Function 3
40	DIO70/SWCLK	GPIO70	SWCLK		
41	DIO-SEG63	GPIO63	SEG63		
42	DIO-SEG62	GPIO62	SEG62		
43	DIO-SEG61/1_SEC_PLS	GPIO61	SEG61	1_SEC_ PLS	
44	DIO-SEG60	GPIO60	SEG60		
45	DIO-SEG59	GPIO59	SEG59		
46	DIO-SEG58	GPIO58	SEG58		
47	DIO-SEG57	GPIO57	SEG57		
48	DIO-SEG56	GPIO56	SEG56		
49	DIO-SEG55	GPIO55	SEG55		
50	V3P3D. DIO bypass point. Connect a 100nF capacitor. This pin should not be used to power external compo-nents.				
51	DIO-SEG54/PWM3	GPIO54	SEG54	PWM3	
52	DIO-SEG53/RX2	GPIO53	SEG53	RX2	
53	DIO-SEG52/TX2	GPIO52	SEG52	TX2	
54	DIO-SEG51	GPIO51	SEG51		
55	DIO-SEG50	GPIO50	SEG50		
56	DIO-SEG49	GPIO49	SEG49		
57	DIO-SEG48	GPIO48	SEG48		
58	DIO-SEG47	GPIO47	SEG47		
59	DIO-SEG46	GPIO46	SEG46		
60	DIO-SEG45	GPIO45	SEG45		
61	DIO-SEG44	GPIO44	SEG44		
62	MUX_ADC6. Additional input to ADCM.				
63	ICP/RMT2_P	ICP	RMT2_P		
64	ICN/RMT2_N	ICN	RMT2_N		
65	IBP/RMT1_P	IBP	RMT1_P	MUX_ADC3	
66	IBN/RMT1_N	IBN	RMT1_N	MUX_ADC2	
67	IAP/RMT0_P	IAP	RMT0_P	MUX_ADC1	
68	IAN/RMT0_N	IAN	RMT0_N	MUX_ADC0	
69	V3P3A. Analog supply voltage. This pin should be connected to the V3P3SYS pin (38).				
70	IN. Input for signal from neutral current sensor.				
71	VC. Input for divided phase voltage C/L3.				
72	VB. Input for divided phase voltage B/L2.				
73	VA. Input for divided phase voltage A/L1.				
74	GNDA. Analog ground.				
75	XOUT. Crystal oscillator output, 32.768kHz				
76	XIN. Crystal oscillator input, 32.768kHz				
77	VBAT. Battery voltage for BRN mode. Connect to the positive terminal of a battery or to V3P3SYS.				
78	VBAT_RTC. Battery y voltage NV supply (RTC). Connect to the positive terminal of a battery or to V3P3SYS.				
79	VLCD. Bypass point for the LCD voltage. Connect to a 100nF capacitor. An external DC voltage for the LCD system may be applied.				
80	V3P3RTC. Bypass point for NV voltage. Connect to a 1.0µF capacitor.				
81	RST. Reset (active high). Can be connected to a pushbutton, if desired.				
82	TEST. Test/program mode input (active high). Pull high to program or connect the emulator. Pull low for normal operation.				

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Pin No.	Pin Name	Primary Function	Alt. Function 1	Alt. Function 2	Alt. Function 3
83	WAKE_COMP. Wake comparator input				
84	DIO-SEG43/WAKE0	GPIO43	SEG43	WAKE0	
85	DIO-SEG42/WAKE1	GPIO42	SEG42	WAKE1	
86	DIO-SEG41/WAKE2	GPIO41	SEG41	WAKE2	
87	DIO-SEG40/WAKE3	GPIO40	SEG40	WAKE3	
88	DIO-SEG39/RX0	GPIO39	SEG39	RX0	
89	DIO-SEG38/RX1	GPIO38	SEG38	RX1	
90	DIO-SEG37/TX0	GPIO37	SEG37	TX0	
91	DIO-SEG36/TX1	GPIO36	SEG36	TX1	
92	DIO-SEG35	GPIO35	SEG35		
93	DIO-SEG34	GPIO34	SEG34		
94	DIO-SEG33	GPIO33	SEG33		
95	DIO-SEG32	GPIO32	SEG32		
96	DIO-SEG31	GPIO31	SEG31		
97	DIO-SEG30	GPIO30	SEG30		
98	DIO-SEG29	GPIO29	SEG29		
99	DIO-SEG28	GPIO28	SEG28		
100	DIO-SEG27	GPIO27	SEG27		

Battery Connection Options

VBAT Pin Connection	VBAT_RTC Pin Connection	BRN Mode *)	SLP Mode *)	Description
Battery 1	Battery 2	Supported	Supported	RTC and NV-RAM are maintained by battery 2 when battery 1 loses charge and board supply is down.
Battery		Supported	Supported	Support for BRN mode (VBAT) and SLP mode (VBAT_RTC). RTC and NV-RAM are not maintained when the battery loses charge and board supply is down.
V3P3SYS	Battery	--	Supported	RTC and NV-RAM are maintained by the battery. BRN mode is not supported when board supply is down.
Battery	V3P3SYS	Supported	--	RTC and NV-RAM are not maintained when board supply is down.
V3P3SYS	V3P3SYS	--	--	RTC and NV-RAM are not maintained when board supply is down. There is no BRN mode capability. This connection option is typical for a panel meter.

*) See Power Modes section (page 26) for an explanation of BRN and SLP modes.

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Unused Pins

Pin Type	Connection when Unused	Application Code	Comment
DIO-SEG	GND or V3P3	Configure as input	GND or V3P3 direct or via resistor. Pins can also be configured as output/low when GND or as output/high when V3P3
DIO-COM	GND or V3P3	Configure as input	
RMT_DRIVE_H	GND or V3P3	Configure as input	
DIO71/SWDIO, DIO70/SWCLK	GND		Programming pins are inactive when TEST = LOW. These pins are normally connected to the programming header if in-circuit flash programming is used.
MUX_ADC6	GND		Auxiliary ADC input should be grounded
VA, VB, VC	GND		ADC muxed inputs should be grounded
RST	GND		Reset input – may not be connected to a PB in a production me-ter. Apply GND direct or via pull-down resistor
TEST	GND		Test input - may not be used in a production meter if programmed ICs are inserted into the PCB. Apply GND direct or via pull-down resistor.
WAKE_COMP	GND	Clear *ew_wcomp* bit in SYS_WAKE register	Apply direct GND or via pull-down resistor
UART Wake pins (RX0, RX1)	V3P3	Configure as DIO pins, clear associ-ated wake bit in *SYS_WAKE* register	Pin must be low or high in SLP and LCD-ONLY modes to prevent leakage
PB Wake pins (WAKE0, WAKE1, WAKE2, WAKE3)	GND		

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Absolute Maximum Ratings

Stresses beyond Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation at these or other conditions beyond those indicated under “Operating Conditions” is not implied. Exposure to these Absolute Maximum Rated conditions for extended periods may affect device reliability.

	Min	Max	Unit
Supply and Ground Pins:			
V_{3P3SYS}, V_{3P3A}	-0.5	3.6	V
V_{BAT}, V_{BAT_RTC}	-0.5	3.8	V
GNDA, GNDD	-0.1	0.1	V
Analog Output Pins:			
V_{3P3D}, V_{3P3RTC}	-10	10	mA
	-0.5	3.6	V
V_{DD}	-10	10	mA
	-0.5	3.0	V
V_{LCD}	-10	10	mA
	-0.5	3.6	V
Analog Input Pins:			
IAP, IAN, IBP, IBN, ICP, ICN, VA, VB, VC, IN, MUX_ADC6	-10	10	mA
	-0.5	V_{3P3A}+0.5	V
WAKE_COMP	-10	10	mA
	-0.5	V_{3P3RTC}+0.5	V
Crystal Oscillator Pins:			
XIN, XOUT	-10	10	mA
	-0.5	3.0	V
LCD Segment and DIO Pins:			
Configured as Digital Inputs/Outputs (All DIO pins except DIO16 – DIO20 and DIO39 – DIO43)	-10	10	mA
	-0.5	V_{3P3D}+ 0.5	V
Configured as Digital Inputs/Outputs (DIO pins DIO16 – DIO20), 5V-tolerant pins	-10	10	mA
	-0.5	5.5	V
Configured as Digital Inputs/Outputs (DIO pins DIO39 – DIO43)	-10	10	mA
	-0.5	V_{3P3RTC}+0.5	V
Digital Control Pins:			
Inputs (RST, TEST)	-10	10	mA
	-0.5	V_{3P3RTC}+ 0.5	V

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	Min	Max	Unit
Temperature Ratings:			
Operating junction temperature, peak, 100ms		+140	°C
Operating junction temperature, continuous		+125	°C
Storage temperature	-45	+165	°C
Solder temperature, 10s duration		+260	°C
Electrostatic Discharge (ESD) Ratings:			
ESD Stress on All Pins (HBM)		±2	kV

Thermal Ratings

Parameter	Value	Unit
LQFP-100		
Θ_{JA} Junction-to-Ambient Thermal Resistance	53.26	$\frac{°C}{W}$
Θ_{JC} Junction-to-Case (bottom) Thermal Resistance	9.03	
Maximum Power Dissipation T_A = 25°C	2.35	W

Θ_{JA} is measured with natural convection at T_A = 25°C on a four-layer Silergy Evaluation Board.

Recommended Operating Conditions

The device is not guaranteed to function outside of its operating conditions.

Parameter	Conditions	Min	Max	Unit
Supply Voltage V_{3P3A}, V_{3P3SYS}	Mission (MSN) mode	3.0	3.6	V
Supply Voltage V_{BAT}	Brownout (BRN) mode	2.5	3.6	V
Supply Voltage V_{BAT_RTC}	Sleep (SLP) mode/LCD_ONLY mode	2.0	3.6	V
Operating Temperature	All modes	-40	+85	°C

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Recommended External Components

Name	From Pin	To Pin	Function	Value	Unit
XTAL	XIN	XOUT	32.768kHz crystal	32.768	kHz
CXS	XIN	GND	Load capacitors for the crystal. Exact values depend on crystal specifications and parasitic capacitance of the PCB (4pF assumed).	22 ±10%	pF
CXL	XOUT	GND		33 ±10%	pF
CV3P3A	V3P3A	GND	Analog supply bypass capacitor	1.0±30%	µF
CV3P3S	V3P3SYS	GND	Digital supply bypass capacitor	1.0±30%	µF
CV3P3D	V3P3D	GND	V3P3D bypass capacitor (10µF, if low-power modes are used)	0.1±20%	µF
CVDD	VDD	GND	Core voltage supply bypass capacitor	1.0±20%	µF
CVLCD	VVLCD	GND	LCD supply bypass capacitor	0.1±20%	µF
CVRTC	V3P3RTC	GND	Non-volatile supply bypass capacitor	1.0±30%	µF
RSPIPD	14, 15, 16, 17	GND	Pull-down resistors for DIO17- DIO20, if not used for SPI or to drive external components.	100	kΩ

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Electrical Characteristics

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Digital Input Logic Levels:						
Digital Low-Level Input Voltage (All DIO pins except DIO39 – DIO43, RST, TEST) †	V_{IL}				$0.15*V_{3P3D}$	V
Digital Low-Level Input Voltage (DIO pins DIO39 – DIO43, RST, TEST) †					$0.15*V_{3P3RTC}$	
Digital High-Level Input Voltage (All DIO pins except DIO39 – DIO43, RST, TEST) †	V_{IH}		$0.7*V_{3P3D}$			V
Digital High-Level Input Voltage (DIO pins DIO39 – DIO43, RST, TEST) †			$0.75*V_{3P3RTC}$			
Schmitt Trigger Hysteresis (all DIO pins except DIO16-DIO20, RST, TEST)	V_{HYS}			0.4		V
Schmitt Trigger Hysteresis (DIO pins DIO16-DIO20, RST, TEST)	V_{HYS}			0		V
Input Leakage Current	I_{IN}	Pull-Up Resistor Disabled	-1		1	µA
Input Current, DIO16 – DIO20	I_{IH}	With +5.5V applied to pin		16	40	µA
Pull-Up Resistance, all DIO pins except DIO16-20 which are 5V-tolerant and have no pull up/down	R_{PU}		45	72	105	kΩ
Pull-Down Resistance, all DIO pins except DIO16-20 which are 5V-tolerant and have no pull up/down	R_{PD}		45	72	110	µA
Pull-Down Current, RESET, TEST	I_{PD}			75	150	µA
Low Leakage Current, RESET, TEST	I_{LL}			0.5	2	µA

† In battery powered modes, digital inputs should be below 0.1V or above the battery voltage minus 0.1V to minimize battery current.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Digital Output Logic Levels:						
Digital Low-Level Output Voltage	V_{OL}	I_{OL} = 8mA			0.5	V
Digital High-Level Output Voltage (All DIO pins except DIO39 – DIO43, RST, TEST) ††	V_{OH}	I_{OH} = 8mA	V_{3P3D}-0.6			V
Digital High-Level Output Voltage (DIO pins DIO39 – DIO43, RST, TEST)	V_{OH}	I_{OH} = 0.5 mA	V_{3P3RTC}-0.5			V

†† Caution: The sum of all drive high currents will cause a voltage drop across the relevant V_{3P3D} switch resistance, which will reduce the V_{3P3D} and V_{OH} level, and will also decrease the margin of the V3P3DOK threshold.

††† Caution: The sum of all drive high currents will cause a voltage drop across the relevant V_{3P3RTC} switch resistance, which will reduce V_{OH} level.

$$V_{3P3D}(I_{SUM}) = V_{3P3D}(0) - I_{SUM} \cdot R_{SWITCH}$$

$$V_{OH}(I_{SUM}) = V_{OH}(0) - I_{SUM} \cdot R_{SWITCH}$$

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Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Analog Input Signal Levels						
Analog Low-Level Input Voltage	V_{ILA}		-125			mV
Analog High-Level Input Voltage	V_{IHA}				125	mV
Transient Spike Width Tolerance						
Transient Spike Width Tolerance DIO pins DIO39 – DIO43 †	T_{SPIKE_DIO}	Positive Spike	1.2	4	11.5	µs
Transient Spike Width Tolerance RST †	T_{SPIKE_RST}		1.2	4	11.5	
Transient Spike Width Tolerance TEST ††, †††	T_{SPIKE_TEST}		1.2	4	11.5	

† Positive spikes narrower than the minimum limit will be ignored by these pins. When asserted high, these pins must be held at least as long as the maximum limit.

†† The TEST spike width tolerance is not measurable.

††† Not tested in production.

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Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Supply Currents						
V_{3P3SYS} Current in MSN Mode	I_{3P3SYS_1}	ADCM (4 slots): *adcm_spd*=5.111MHz, *adcm_low_bias*=0, *adcm_bias*[3:0]=0b110, *mux_div*[2:0]=0b100, FIR lengths set to 384 ADCS (3 enabled): *adcs_spd*=1.704MHz, *adcs0_low_bias*=0, *adcs1_low_bias*=0, *adcs2_low_bias*=0, *adcs0_bias*[3:0]=0b111, *adcs1_bias*[3:0]=0b111, *adcs2_bias*[3:0]=0b111, ***pre_en*=1**, CE halted, *adc_vls*=0, *mpu_spd*=10.224MHz		2	2.5	mA
V_{3P3A} Current in MSN Mode	I_{3P3A_1}			5.2	6.6	mA
V_{3P3SYS} Current in MSN Mode	I_{3P3SYS_2}	ADCM (4 slots): *adcm_spd*=5.111MHz, *adcm_low_bias*=0, *adcm_bias*[3:0]=0b110, *mux_div*[2:0]=0b100, FIR lengths set to 384 ADCS (3 enabled): *adcs_spd*=1.704MHz, *adcs0_low_bias*=0, *adcs1_low_bias*=0, *adcs2_low_bias*=0, *adcs0_bias*[3:0]=0b111, *adcs1_bias*[3:0]=0b111, *adcs2_bias*[3:0]=0b111, ***pre0_en*=0**, CE halted, *adc_vls*=0, *mpu_spd*=10.224MHz		2	2.5	mA
V_{3P3A} Current in MSN Mode	I_{3P3A_2}			5	6.5	mA
V_{3P3SYS} Current in MSN Mode	I_{3P3SYS_3}	ADCM (4 slots): *adcm_spd*=2.556MHz, *adcm_low_bias*=0, *adcm_bias*[3:0]=0b101, *mux_div*[2:0]=0b100, FIR lengths set to 384 ADCS (3 enabled): *adcs_spd*=0.852MHz, *adcs0_low_bias*=0, *adcs1_low_bias*=0, *adcs2_low_bias*=0, *adcs0_bias*[3:0]=0b100, *adcs1_bias*[3:0]=0b100, *adcs2_bias*[3:0]=0b100, ***pre_en*=1**, CE halted, *adc_vls*=0, *mpu_spd*=10.224MHz		1.6	2.1	mA
V_{3P3A} Current in MSN Mode	I_{3P3A_3}			2.3	3.3	mA

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Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Battery Currents						
V_{BAT} Current in MSN Mode	I_{VBAT_1}	Remote disabled, ADCM disabled, ADCS disabled, CE off, *adc_vls*=0, *mpu_spd*=10.224MHz		0	100	nA
V_{BAT} Current in BRN Mode	I_{VBAT_2}	ADCM (4 slots): *adcm_spd*=5.111MHz, *adcm_low_bias*=0, *adcm_bias*[3:0]=0b110, *mux_div*[2:0]=0b100, FIR lengths set to 384 ADCS (3 enabled): *adcs_spd*=1.704MHz, *adcs0_low_bias*=0, *adcs1_low_bias*=0, *adcs2_low_bias*=0, *adcs0_bias*[3:0]=0b111, *adcs1_bias*[3:0]=0b111, *adcs2_bias*[3:0]=0b111, *pre_en*=1, standard CE code pass, *adc_vls*=0, *mpu_spd*=10.224MHz		7	8.6	mA
V_{BAT} Current in LCD_ONLY Mode	I_{VBAT_10}	Minimum LCD clock frequency, LCD DAC disabled, no LCD SRAM access		8	16	µA
V_{BAT} Current in LCD_ONLY Mode	I_{VBAT_11}	Minimum LCD clock frequency, LCD DAC enabled, no LCD SRAM access		19	28	µA
V_{BAT} Current in SLP Mode, VBAT_RTC = VBAT	I_{VBAT_14}	RTC compensation disabled		3.5	8	µA
V_{BAT_RTC} Current in MSN Mode	$I_{VBAT_RTC_1}$	Remote disabled, ADCM and ADCS disabled, CE off, *adc_vls*=0, *mpu_spd*=10.224MHz		0	100	nA
V_{BAT_RTC} Current in BRN Mode	$I_{VBAT_RTC_2}$	Remote disabled, ADCM and ADCS disabled, CE off, *adc_vls*=0, *mpu_spd*=10.224MHz		0	100	nA
V_{BAT_RTC} Current in LCD_ONLY Mode	$I_{VBAT_RTC_3}$	Minimum LCD clock frequency, LCD DAC disabled, no LCD SRAM access,		0	100	nA
V_{BAT_RTC} Current in SLP Mode, VBAT = VBAT_RTC	$I_{VBAT_RTC_4}$	RTC compensation disabled		0	100	nA
V_{BAT_RTC} Current in SLP Mode, VBAT = 0V	$I_{VBAT_RTC_7}$	RTC compensation disabled		1.7	4	µA

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Parameter	Symbol	Conditions	Min	Typ	Max	Unit
V_{3P3D} Switch						
On Resistance V_{3P3SYS} to V_{3P3D}		$\|I_V3P3D\| \leq 7mA$		5	8	Ω
On Resistance V_{BAT} to V_{3P3D}		$\|I_V3P3D\| \leq 7mA$ V_{BAT} > 2.5V		10	15	Ω
V_{3P3D} I_{OH}, MSN Mode		V_{3P3SYS} = 3.0V V_{3P3D} = 2.9V	8			mA
V_{3P3D} I_{OL}, BRN Mode		V_{BAT} = 2.6V V_{3P3D} = 2.5V	5			mA
Note that the sum of all pull-up currents in all DIOs except DIO39 – DIO43 will cause a voltage drop across the relevant V_{3P3D} switch resistance, which will reduce V_{3P3D} and the V_{OH} level. $$V_3P3D\ (I_SUM\ ) = V_3P3D\ (0) - I_SUM \cdot R_SWITCH$$ $$V_OH\ (I_SUM\ ) = V_OH\ (0) - I_SUM \cdot R_SWITCH$$						
V_{3P3RTC} Switch						
On Resistance – V_{3P3SYS} to V_{3P3RTC}		$\|I_VP3RTC\ \| \leq 1mA$		50	80	Ω
On Resistance – V_{BAT} to V_{3P3RTC}		$\|I_VP3RTC\| \leq 1mA$ V_{BAT} > 2.5V		50	80	Ω
On Resistance – V_{BAT_RTC} to V_{3P3RTC}		$\|I_V3P3RTC\| \leq 1mA$ V_{BAT_RTC} > 2.5V		50	80	Ω
Note that the sum of all pull-up currents in DIO39 – DIO43 will cause a voltage drop across the relevant V_{3P3RTC} switch resistance, which will reduce V_{3P3RTC} and the V_{OH} level. $$V_3P3RTC\ (I_SUM\ ) = V_3P3NV\ (0) - I_SUM \cdot R_SWITCH$$ $$V_OH\ (I_SUM\ ) = V_OH\ (0) - I_SUM \cdot R_SWITCH$$						
Power Fault Comparators						
V3AOK Voltage Threshold		V_{3P3SYS}/V_{3P3A} falling V_{3P3SYS}/V_{3P3A} rising	2.7	2.8 2.83	 2.93	V V
V3OK Voltage Threshold		V_{3P3SYS}/V_{3P3A} falling V_{3P3SYS}/V_{3P3A} rising	2.28	2.43 2.45	 2.62	V V
V3P3DOK Voltage Threshold		V_{3P3D} falling V_{3P3D} rising	2.09	2.28 2.36	 2.55	V V
VDDOK Voltage Threshold Internal design specification only, not measurable		V_{3P3D} falling V_{3P3D} rising	1.9		 2.2	V V
VBATOK Voltage Threshold		V_{BAT} falling V_{BAT} rising	2.26	2.42 2.45	 2.62	V V
Hysteresis V3AOK V3OK V3P3DOK VDDOK, not measurable VBATOK				 35 30 80 45 30		mV
V3AOK Response Time, Including Filters		100mV overdrive falling 100mV overdrive rising	30 30		90 90	µs
V3OK Response Time, Including Filters		100mV overdrive falling 100mV overdrive rising	30 30		90 90	µs

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Parameter	Symbol	Conditions	Min	Typ	Max	Unit
V3P3DOK Response Time, Including Filters		100mV overdrive falling 100mV overdrive rising	30 30		90 90	µs
VBATOK Response Time, Including Filters		100mV overdrive falling 100mV overdrive rising	30 30		90 90	µs
Cold Start Threshold (Supply Voltage below limit causes a Cold Start)		Lower all supplies from 2.3V until cold start wake flag asserts	0.9	1.3	1.95	V
WAKE_COMP Comparator						
Voltage Threshold		V at WAKE_COMP rising, part exits SLP mode	1.05	1.2	1.35	V
V_{BAT}, V_{BAT_RTC} Battery Voltage Monitor						
Measurement Equation		$V_B = Y + (Z \cdot bsense) + (W \cdot stemp)$ Y=-0.092, Z=0.025, W=45.9*10^{-6}				V
Nominal Value for *bsense*		V_{3P3SYS}=V_{3P3A}=3.3V, T_A=22°C, V_{BAT}, V_{BAT_RTC}=3.0V, *temp_pwr*=1	120	124	128	LSB
Measurement Resolution		T_A=22°C		25		$\frac{mV}{LSB}$
Measurement Error		2.4V ≤ V_{BAT}, V_{BAT_RTC} ≤ 3.8V *temp_pwr*=1, *temp_pwr*=0	-100		100	mV
De-passivation Load I_{BAT}(*temp_bcur* = 1) – I_{BAT}(*temp_bcur* = 0)		V_{3P3SYS}=V_{3P3A}=3.3V	60	100	140	µA
Battery Monitor VCO Frequency		V_{3P3SYS}=V_{3P3A}=3.3V, V_{BAT}, V_{BAT_RTC}=3.3V	0.8		3.6	MHz
Battery Monitor Input Impedance		V_{3P3SYS}=V_{3P3A}=3.3V, V_{BAT}, V_{BAT_RTC}=3.6V, in continuous measurement mode with *temp_bsel*=0, *temp_per*=111	270	400	530	kΩ
Temperature Monitor						
Measurement Equation		T = T_{CAL} + 0.08286*(*stemp* – $stemp_{CAL}$) -2.1287*10^{-6} *(*stemp* – $stemp_{CAL}$)^2				°C
Nominal Value at T_A=22°C (this value is with reference to the value stored in the *stemp_22* trim fuse)	$stemp_{22}$	V_{3P3SYS}=V_{3P3A}=3.3V, T_A=22°C, *temp_pwr*=1	-200	0	+200	LSB
Measurement Error at T_A=-40, -20, 0, 22, 45, 65, 85°C †††		V_{BAT}, V_{BAT_RTC}=2.4V to 3.8V *temp_pwr*=0	-1.9		+1.9	°C
Temperature Measurement Standard Deviation †††		T_A=22°C		0.12		°C
Measurement Time †††				26	60	ms
Measurement Current †††				100		µA

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Parameter	Symbol	Conditions	Min	Typ	Max	Unit
32.768kHz Internal Oscillator						
Nominal Frequency	f_{nom}	V_{3P3SYS}=V_{3P3A}=3.3V, T_A=22°C		32.8		kHz
Frequency Error	e_f		-2		2	%
Frequency Variation with Supply Voltage	df/dV		-0.4		+0.4	$\frac{kHz}{V}$
32.768kHz Crystal Oscillator						
Nominal Frequency		V_{3P3SYS}=V_{3P3A}=3.3V, T_A=22°C		32.768		kHz
Transconductance		V_{IN}=32.768kHz, 10mV peak-to-peak sinewave, measure voltage across 100kΩ resistor	8		50	µS
Peak Output Source Current		I_{XOUT} when XOUT=0V	0.4	0.97	1.7	µA
Frequency Variation with Supply Voltage V_{BAT_RTC} with respect to V_{BAT_RTC}=3.3V †††		V_{3P3SYS}=V_{3P3A}=3.3V, T_A=22°C, at V_{BAT_RTC}=3.8V, 3.0V, 2.5V			±0.5	ppm
Metrology Bandgap Reference (VREF) and Buffer						
V_{REF} Voltage	V_{REF}(22)	T_A=22°C, trimmed	1.199	1.2017	1.205	V
V_{REF} Power Supply Rejection Ratio (PSRR) $\Delta V_{REF}/\Delta V_{3P3A}$			-1.5		1.5	$\frac{mV}{V}$
V_{NOM} Definition, with respect to *stemp*	V_{NOM}(S)	$VNOM(S) = VREF_{22} + (S - S_{22}) \times TC1_S + (S - S_{22})^2 \times TC2_S$ $S = stemp, \quad S_{22} = stemp(22°C)$				V
V_{REF}(T) Deviation from V_{NOM}(T) $\frac{(V_{REF}(T) - V_{NOM}(T)) \cdot 10^6}{V_{NOM}(T) \cdot 62}$		-40°C to -17°C -17°C to +85°C	-64 -58		+64 +58	$\frac{ppm}{°C}$
V_{NOM} Temperature Coefficient, linear †††, with respect to *stemp*	$TC1_S$	$-9.4135 - 0.35183 \times TRIM_BGT$ *TRIM_BGT* is available in the Info Block (range = -128 to +127). The number must be inverted, e.g., if it reads 0x10 (=0b00011010, decimal 16), the inverted value is 0b11101111 (with a leading 1). Then, *TRIM_BGT* is -17 or 111 (=0b01101111) – 128				$\frac{\mu V}{stemp}$
V_{NOM} Temperature Coefficient, quadratic †††, with respect to *stemp*	$TC2_S$	$-0.00080892 + 0.000084712 \times TRIM_BGT$				$\frac{\mu V}{stemp^2}$

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Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Multiplexed ADC (ADCM)						
Usable Input Range			-125		125	mV Peak
Supply Current (Staring ADC Disabled)		*adcm_spd*=2.555904MHz, *adcm_low_bias*=0 *adcm_bias*[3:0]=101		1	1.35	mA
Input Impedance			14		27	kΩ
LSB Size $V_{LSB} = \frac{V_{REF}}{2} \cdot \frac{1.25}{4.75} \cdot \left\{\frac{3}{L}\right\}^3 \cdot \frac{4}{5}$ L = FIR Length (Number of Multiplexed ADC clock cycles)		*firx_len*[3:0]=0xF, 384 cycles *firx_len*[3:0]=0xE, 360 cycles *firx_len*[3:0]=0xD, 336 cycles *firx_len*[3:0]=0xC, 312 cycles *firx_len*[3:0]=0xB, 288 cycles *firx_len*[3:0]=0xA, 264 cycles		60.8 73.8 90.8 113.4 144.2 187.2		$\frac{nV}{LSB}$
Digital Full Scale $DFS = \left(\frac{L}{3}\right)^3 * \left(\frac{5}{4}\right)$ L = FIR Length (Number of Multiplexed ADC clock cycles)		*firx_len*[3:0]=0xF, 384 cycles *firx_len*[3:0]=0xE, 360 cycles *firx_len*[3:0]=0xD, 336 cycles *firx_len*[3:0]=0xC, 312 cycles *firx_len*[3:0]=0xB, 288 cycles *firx_len*[3:0]=0xA, 264 cycles		2,621,440 2,160,000 1,756,160 1,406,080 1,105,920 851,840		LSB
Input Offset			-10		10	mV
Gain Error vs Power Supply Variation $\frac{10^6 \Delta Nout_{PK}\ 357nV/V_{IN}}{100 \Delta V_{3P3A}/3.3}$		V_{in}=200mVpk, 65Hz, V_{3P3A} 3.0V to 3.6V, FIR Length=288			±50	$\frac{ppm}{\%}$
Gain Error over Temperature		LSB variation over temperature, *firx_len*[3:0]=0xF	-0.005		+0.005	$\frac{nV}{°C}$
Total Harmonic Distortion (THD)		Vin=10mVpk, 55Hz, 64kpts FFT, Blackman-Harris window		-85		dB
		Vin=125mVpk, 55Hz, 64kpts FFT, Blackman-Harris window		-85		
ADC Noise		Vin=20mVpk, 55Hz, *firx_len*[3:0]=0xF		400		LSB
ADC Input Equivalent Noise Density		Vin=20mVpk, 55Hz, *firx_len*[3:0]=0xF		2,000		$\frac{nV}{\sqrt{Hz}}$
Staring ADCs (ADCS)						
Usable Input Range		Preamp off	-125		125	mV Peak
		Preamp on †††	-15.62		15.62	
Supply Current for 3 ADCs, Multiplexed ADC Disabled, Preamp Disabled		*adcs_spd*=851.968kHz *adcsx_low_bias*=0 *adcsx_bias*[3:0]=0b101		1.1	1.41	mA
Preamp Supply Current (IAP/IAN) †††		*adcsx_bias*[3:0]=0b100		0.11	0.14	mA
Input Impedance		Preamp off	28		85	kΩ
		Preamp on †††	2.5		10	

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Parameter	Symbol	Conditions	Min	Typ	Max	Unit
LSB Size $V_{LSB} = \frac{V_{REF}}{2} \cdot \frac{1.25}{4.75} \cdot \left\{\frac{1}{L}\right\}^3$ L = Number of Staring ADC clock cycles in one sample period (sample period equals the duration of one Multiplexed ADC frame)		*adcs_spd*[1:0]=851.968kHz Sample Rate / ADC clock cycles 2521Hz 338 2731Hz 312 2979Hz 286 3277Hz 260 3641Hz 234 4096Hz 208 4681Hz 182 5461Hz 156 6554Hz 130 8192Hz 104		4.13 5.25 6.82 9.07 12.45 17.72 26.45 42.01 75.59 141.77		$\frac{nV}{LSB}$
Digital Full Scale $DFS = L^3$ L = Number of Staring ADC clock cycles in one Multiplexed ADC frame (sample period equals the duration of one Multiplexed ADC frame)		*adcs_spd*[1:0]=851.968kHz Sample Rate / ADC clock cycles 2521Hz 338 2731Hz 312 2979Hz 286 3277Hz 260 3641Hz 234 4096Hz 208 4681Hz 182 5461Hz 156 6554Hz 130 8192Hz 104		38,614,472 30,371,328 23,393,656 17,576,000 12,812,904 8.998,912 6,028,568 3,796,416 2,197,000 1,124,864		LSB
Input Offset		Preamp off	-4		+4	mV
		Preamp on, input referenced †††	-4		+4	
Preamp Input Current			18	31	42	µA
Preamp Gain †††			7.7	7.9	8.1	V/V
Preamp Gain Variation vs Supply †††			-240		+240	$\frac{ppm}{\%}$
Preamp Gain Variation vs Temperature †††			-110		+110	$\frac{ppm}{°C}$
Preamp Phase Shift †††				9		m°
Preamp Phase Shift Variation vs Supply †††			-65		+65	$\frac{m°}{V}$
Preamp Phase Shift Variation vs Temperature †††			-0.3		+0.3	$\frac{m°}{°C}$
ADC Gain Error vs %Power Supply Variation ††† $\frac{10^6 \, \Delta Nout_{PK} \, 357nV/V_{IN}}{100 \, \Delta V3P3A/3.3}$		V_{in}=200mVpk, 65Hz, V_{3P3A} = 3.3V, sample rate 2521Hz, *adcs_spd*[1:0] = 851.968kHz ADCS0, adc_bias=0110 ADCS1/2, adc_bias=0110	-200 -132		200 132	$\frac{ppm}{\%}$
Total Channel Gain Error vs Power Supply Variation (same as above, but with preamp enabled) †††		ADCS0 adc_bias=0110	-291		291	$\frac{ppm}{\%}$
ADC Gain Error over Temperature †††		LSB=85nV. Change in LSB from -40C to 85C. Vref change over temperature is included.	-0.007		0.007	$\frac{nV}{°C}$

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Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Total Channel Gain Error over Temperature (same as above, but with preamp enabled) †††		LSB=10.8nV. Change in LSB from -40C to 85C. Vref change over temperature is included.	-0.002		0.002	$\frac{nV}{°C}$
Total Harmonic Distortion (THD), Preamp enabled †††		Preamp on, Vin=10mVpk, 55Hz, 64kpts FFT, Blackman-Harris window		-85		dB
Total Harmonic Distortion (THD), Preamp disabled		Preamp off, Vin=125mVpk, 55Hz, 64kpts FFT, Blackman-Harris window		-85		dB
Preamp Noise †††		Preamp on, Vin=10mVpk, 55Hz, sample rate 2521Hz, *adcs_spd*[1:0]= 851.968kHz		425		LSB
Preamp Input Equivalent Noise Density †††		Preamp on, Vin=10mVpk, 55Hz, sample rate 2521Hz, *adcs_spd*[1:0]=851.968kHz		300		$\frac{\mathrm{nV}}{\sqrt{\mathrm{Hz}}}$
ADC Noise †††		Preamp off, Vin=10mVpk, 55Hz, sample rate 2521Hz, *adcs_spd*[1:0]= 851.968kHz		400		LSB
ADC Input Equivalent Noise Density †††		Preamp off, Vin=10mVpk, 55Hz, sample rate 2521Hz, *adcs_spd*[1:0]= 851.968kHz		300		$\frac{\mathrm{nV}}{\sqrt{\mathrm{Hz}}}$
Remote Receivers						
Supply Current		$I(V_{3P3A})$ receiver enabled – $I(V_{3P3A})$ receiver disabled, V_{IN}=0V, V_{CM}=1.8V 3 remotes enabled		1400	1700	µA
Input Bias Voltage		V_{CM}=open, *r2k_en*=1	1.7	1.8	1.9	V
Differential Input Resistance, *r2k_en*=1		V_{CM}=1.8V, V_{IN}=±100mV	3.2	5	7	kΩ
Differential Input Resistance, *r2k_en*=0		V_{CM}=1.8V, V_{IN}=±100mV	100	160	220	kΩ
Input Resistance Mismatch, V_{CM}=0V		V_{CM}=10V, *r2k_en*=0	-1.1		1.1	%
Input Resistance Mismatch, V_{CM}=3.3V		V_{CM}=1.8V, *r2k_en*=0	-1.3		1.3	%
Propagation Delay, RX Rising		V_{IN}=10mV peak, V_{CM}=1.8V		25		ns
Propagation Delay, RX Falling		V_{IN}=10mV peak, V_{CM}=1.8V		25		ns
Input Offset, V_{CM}=0V			-14		14	mV
Input Offset, V_{CM}=1.8V			-12		12	mV
Input Offset, V_{CM}=V_{3P3A}			-15		15	mV
Remote Power Pulse Driver						
Power pulse output VOH, DIO73, positive pin		I_{OH} = 20mA. Vdoh=V3P3SYS- V(DIO73)			.4	V
Power pulse output VOL, DIO72, negative pin		I_{OL} = 20mA. Vdol=V(DIO73)- V(GNDD)			.4	V

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Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Synchronous Serial Interface (I²C Master, SPI Master)						
I²C Master Frequency, *dio_eex*[1:0]=01		*high_spd*=0		100		kHz
		high_spd=1		400		
SPI Master0 Frequency, *dio_eex*[1:0]=11		*high_spd*=0		100		kHz
		high_spd=1		1		MHz
SPI Master1 Frequency, *dio_eex*[1:0]=11		*spi_clk*[1:0]=00		10		MHz
		spi_clk[1:0]=01		6.8		
		spi_clk[1:0]=10		3.4		
		spi_clk[1:0]=11		2.5		
SPI Slave Port †††						
SPI Setup Time	t_{SU}	SPI_SDIN to SPI_SCLK rise	10			ns
SPI Hold Time	t_{HLD}	SPI_SCLK rise to SPI_SDIN	10			ns
SPI Output Delay	t_{DEL}	SPI_SCLK fall to SPI_SDOUT			40	ns
SPI Recovery Time	t_{rec}	SPI_SCSB fall to SPI_SCLK rise	10			ns
SPI Removal Time	t_{REM}	SPI_SCLK rise to SPI_SCSB rise	15			ns
SPI Clock High Time	t_H		40			ns
SPI Clock Low Time	t_L		40			ns
SPI Clock Frequency Ratio	Rf_{CLK}	MPU frequency/SPI_SCLK frequency	2			$\frac{MHz}{MHz}$
SPI Transaction Space	t_{TRA}	SPI_SCSB rise to SPI_SCSB fall	4.5			MPU cycles
LCD Drivers – Specifications apply to all COM and SEG (DIO38 – DIO43: 2.5V ≤ V_{LCD} ≤ V_{3P3D}, DIO38 – DIO43: 2.5V ≤ V_{LCD} ≤ V_{3P3RTC}.						
V_{LCD} Current	I_{LCD}	V_{LCD}=3.3V, *en*=1, m*ode*[2:0] = 110, *on*=1, *clk*=[1:0]00, *vmode*[1:0]=11, all map bits=0		4	9.6	µA
V_{LC2} Voltage	V_{LC2}	With respect to V_{LCD}	-0.1		0.1	V
V_{LC1} Voltage, 2/3 bias	V_{LC1}	With respect to 2*(V_{LC2}/3)	-2.25		2.25	%V_{LC2}
V_{LC1} Voltage, 1/2 bias	V_{LC1}	With respect to V_{LC2}/2	-2.6		2.6	%V_{LC2}
V_{LC0} Voltage, 1/3 bias	V_{LC0}	With respect to V_{LC2}/3	-2.6		2.6	%V_{LC2}
V_{LC0} Voltage, 0V	V_{LC0}	With respect to GND	-0.1		0.1	V
V_{LC1} Impedance, 2/3 bias	V_{LC}	ΔI_{LOAD} = 10µA		9	15	kΩ
V_{LC1} Impedance, 1/2 bias	V_{LC}	ΔI_{LOAD} = -10µA		9	16	kΩ
V_{LC0} Impedance, 1/3 bias	V_{LC0}	ΔI_{LOAD} = 10µA		9	15	kΩ
V_{LC0} Impedance, 3/3 bias	V_{LC0}	ΔI_{LOAD} = -10µA		9	15	kΩ

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Parameter	Symbol	Conditions	Min	Typ	Max	Unit
LCD DAC						
LCD DAC Voltage Adjustment DAC accuracy can be improved by calibration in meter production (see the Hardware Reference Manual)		*lcd_dac* = number in LCD DAC register. v*mode*[1:0]=00 means 4 states, 1/3 bias, v*mode*[1:0]=01 means 3 states, 1/3 bias.	$V_{LCD_DAC} = 2.55\frac{1 + lcd_dac[4:0]}{33.5}$			V
V_{3P3SYS} to V_{LCD} Switch Impedance		V_{3P3SYS}=V_{3P3A}=3.3V, no resistive load on VLCD, v*mode*[1:0]=00, ΔI_{LCD}=10μA			900	Ω
V_{BAT} to V_{LCD} Switch Impedance		V_{3P3SYS}=V_{3P3A}=0V, V_{BAT}=2.5V, no resistive load on VLCD, v*mode*[1:0]=00, ΔI_{LCD}=10μA			900	Ω
V_{LCD} I_{OH} Current ($V_{LCD}(0) - V_{LCD}(I_{OH}) < 0.25$)		V_{3P3SYS}=V_{3P3A}=0V, no resistive load on VLCD, v*mode*[1:0]=01, *lcd_dac*[4:0]=0x1F		275		μA
LCD DAC Full Scale V_{3P3SYS}=V_{3P3A}=3.6V, MSN V_{3P3SYS}=V_{3P3A}=3.0V, MSN V_{BAT}=3.8V,V_{3P3SYS}=V_{3P3A}=0V, BRN V_{BAT}=2.5V,V_{3P3SYS}=V_{3P3A}=0V, BRN		v*mode*[1:0]=01, *lcd_dac*[4:0]=0x1F	 3.5 2.9 3.7 2.4	 3.57 2.97 3.76 2.46	 3.6 3.0 3.8 2.5	V
LCD DAC Mid Scale V_{3P3SYS}=V_{3P3A}=3.6V, MSN V_{3P3SYS}=V_{3P3A}=3.0V, MSN V_{BAT}=3.8V,V_{3P3SYS}=V_{3P3A}=0V, BRN V_{BAT}=2.5V,V_{3P3SYS}=V_{3P3A}=0V, BRN		v*mode*[1:0]=01, *lcd_dac*[4:0]=0x10	 3.02 2.9 3.02 2.4	 3.33 2.95 3.33 2.45	 3.6 3.0 3.65 2.5	V
LCD DAC Zero Scale V_{3P3SYS}=V_{3P3A}=3.6V, MSN V_{3P3SYS}=V_{3P3A}=3.0V, MSN V_{BAT}=3.8V,V_{3P3SYS}=V_{3P3A}=0V, BRN V_{BAT}=2.5V,V_{3P3SYS}=V_{3P3A}=0V, BRN		v*mode*[1:0]=01, *lcd_dac*[4:0]=0x00	 2.32 2.32 2.32 2.4	 2.55 2.55 2.55 2.45	 2.78 2.78 2.678 2.5	V
Flash Memory †††						
Program/Erase Cycles			100,000			Cycles
Data Retention		At +85°C	10			Years
Program Time (32-bit Word)				20		μs
Page Erase Time (1KB Page)				2		ms
Mass Erase Time				10		ms
V_{DD} Standby Current				0.1	5	μA
V_{DD} Active Read Current (32-bit Word)		20MHz read operation frequency			6	mA
V_{DD} Current during Program Operation		T_{PROG}=20us			4	mA
V_{DD} Current during Page Erase Operation		T_{PAGE_ERASE}=2ms			4	mA
V_{DD} Current during Mass Erase Operation		T_{MASS_ERASE}=10ms			4	mA

††† Not tested in production

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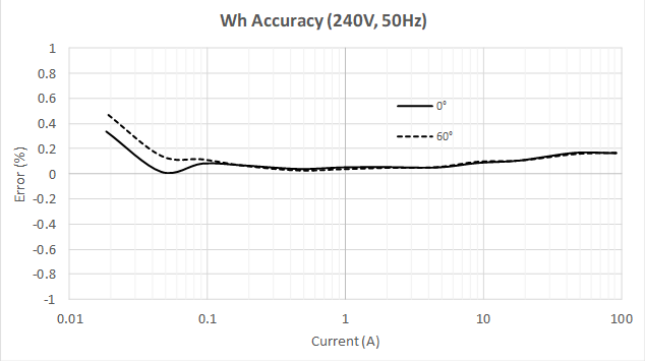
Typical Performance Characteristics

Measured at 240V/50Hz with three CTs.



Measured at 240V/50Hz with 120µΩ shunt.

Detailed Description

On-Chip Resources

Clock Management

For normal operation, an external 32kHz watch crystal is used to drive the internal oscillator. A PLL generates the master clock from the 32kHz signal. If the external crystal fails, an internal R/C backup oscillator trimmed to 32kHz takes over for continued operation.

Power-On Reset (POR)

An on-chip power-on reset (POR) block monitors the supply voltage (VDD) and initializes the internal digital circuitry at power-on. Once VDD is above the minimum operating threshold, the POR circuit triggers and initiates a reset sequence. It also issues a reset to the digital circuitry if the supply voltage falls below the minimum operating level.

No external reset circuitry is necessary.

Watchdog Timer (WDT)

A watchdog timer (WDT) block detects any software processing errors. The embedded code periodically refreshes the free-running watchdog timer to prevent it from timing out. If the WDT times out, it is an indication that software is no longer being executed in the intended sequence; thus, a system reset is initiated. The WDT cannot be disabled by code.

External Reset Pin (RST Pin)

The RST pin can be used in test and evaluation to reset the SY7T213H. For proper reset, the RTS pin must be pulled high for at least 5µs.

Analog Front End (AFE)

The AFE consists of three dedicated (staring) ADCs (ADCS) and one multiplexed ADC (ADCM), followed by FIR filters with programmable length for decimation. The staring ADCs are typically used for the current inputs and have differential inputs. The ADCS for phase A has a selectable gain stage (gain = 1, 8). In the poly-phase SoCs, the gain stage is available, but not tested in production.

32-Bit Compute Engine (CE)

The Compute Engine is 32-bit DSP that performs management and signal processing of the ADC samples. It can perform read and write operation in the dedicated memory space with no wait states. The CE is a programmable device, and Silergy typically provides binary code modules that the CE uses to perform energy computations. The CE calculations and processes may include:

- Multiplication of each current sample with its associated voltage sample to obtain the energy per sample (when multiplied with the constant sample time).
- 90° phase shifter (for VAR calculations).
- Pulse generation.
- Measurement of the input signal frequency (for frequency and phase information).
- Monitoring of the input signal amplitude (for sag and swell detection).
- Scaling of the processed samples based on calibration coefficients.
- Scaling of samples based on MPU temperature compensation information.
- Optional creep processing.
- Extraction, suppression, or filtering of harmonics for special functions.
- Extraction of the fundamental for reactive energy for conformance with IEC 62053-24.
- Variable gain and phase compensation.

The CE Code image resides in flash as part of the Cortex M0 code image.

The CE is a fixed-function core and is not user programmable. Silergy Technology provides many different configurations for the CE as precompiled modules that can be linked into user programs. Please see the relevant *CE Code Reference Manual* for specific functional details.

Debug Interface

The part has an integrated debugger that allows real-time debugging of the code running on the Cortex M0 MPU core. Basic debug functionality includes processor halt, single-step, processor core register access, Reset and Hard Fault Vector Catch,

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four hardware breakpoints, and full system memory access. The debug system uses Serial-Wire Debug (SWD), not JTAG.

RAM

The RAM accessible to the Cortex M0 MPU core is implemented as SRAM. A RAM controller manages simultaneous access requests from multiple SRAM clients. The clients are the CE (data), RTM, FIRs for ADCM and ADCS, LCD DMA, and the Cortex M0 MPU core.

The NV-RAM supported by the V_{BAT_RTC} voltage provides 4KB.

Additional NV-RAM

An additional section of 64 bytes of NV-RAM is not directly accessible and has its own address range. Each cell pointed to by the address pointer has access to 32 bits. The size of this NV-RAM is 16 32-bit words, or 64 bytes.

Flash Programming

The flash memory can be programmed via the debug interface.

Power Modes

The SoC supports five operational (power) modes:

- **Mission (MSN) mode:** The part is in *MSN Mode* when the primary power supply is within specification. Primary power is supplied via the V_{3P3SYS} (digital power) and V_{3P3A} (analog power) pins. Comparators on the V_{3PSYS} pin monitor the voltage level on this bus. If the voltage at the V_{3PSYS} pin falls below a set threshold, the part automatically enters *BRN Mode*.
- **Brownout (BRN) mode:** In *BRN Mode*, the voltages at V_{3P3A} and V_{3P3SYS} are too low to maintain MSN mode operation, and the supply for the I/O and other circuits is automatically switched to the V_{BAT} input. In BRN *Mode* the metrology blocks are functional, and the Cortex M0 MPU core continues to operate at full speed until the firmware selects a lower clock speed, and/or powers down the ADCs to reduce power consumption. BRN mode can be maintained until the voltage at the V_{BAT} pin falls below 2.5V.
- **LCD-ONLY mode:** This mode is commanded by the Cortex M0 MPU core. In this mode, the LCD can take its power from either V_{3P3SYS}, V_{BAT}, or from an external VLCD supply, depending on the LCD configuration. The Cortex M0 MPU core and the analog functions are not available in *LCD-ONLY* mode. It is possible to place up to 15 different images of the LCD in RAM, and step through them automatically without using the Cortex M0 MPU. To support this, RAM remains powered in *LCD-ONLY* mode. Wake pins must be tied low or high in LCD-ONLY mode to prevent excessive current consumption.
- **Sleep (SLP) mode:** The *SLP Mode* is commanded by the Cortex M0 MPU core. In *SLP* mode, hardware shuts down all logic blocks except the RTC and non-volatile memory blocks. In SLP mode all power to the device except the NV domain (and the LCD domain if *LCD-ONLY* is selected) is removed. The only way to exit SLP mode is if a wake event occurs. Various events can be configured to cause a wake up from *SLP* mode, e.g., timer, UART0 RX, pushbutton, two wake pins, or temperature. Wake pins must be tied low or high in SLP mode to prevent excessive current consumption.

Hardware in the SoC and firmware control transitions between the power modes.

There are eight power-related pins in the part:

- **V_{3P3SYS}:** This is the primary digital supply input for the device. It is typically connected to the same supply as V_{3P3A}, but it is separately bypassed.
- **V_{3P3A}:** This is the primary analog supply input for the device. In MSN mode, it provides power to the ADC blocks, to the voltage comparator blocks and to the bandgap voltage reference with its output buffer.
- **V_{BAT}:** The primary battery supply input. This input is selected to provide system power when the V_{3P3SYS} circuit falls below its threshold level.
- **V_{BAT_RTC}:** This pin provides the RTC and non-volatile memory backup power. It is typically connected to a lithium battery to maintain the RTC and NV memory elements.
- **V_{3P3RTC}:** This pin provides a bypass point for the non-volatile power domain.
- **V_{3P3D}:** The output from an internal switch that selects either V_{3P3SYS} (if the primary supply is above threshold) or V_{BAT} (if the primary supply is below threshold). This pin should always be bypassed and never be used to drive external loads.
- **V_{LCD}:** Usually, this is a bypass point for the LCD supply. Frequently the supply will be the LCD DAC, although it can also be the currently selected V_{BAT} or V_{3P3SYS} supply, directly. This pin can also be used as an input to provide an external voltage to the LCD system.
- **V_{DD}:** The bypass point for the power supply to the internal flash memory

Digital I/O Pins

The SoC contains 73 pins that can be configured as digital I/O (DIO0 – DIO72). When assigned for general-purpose I/O (GPIO), the user can select from different configurations. Pins configured for DIO provide the following properties:

- Programmable interrupt generation capability.
- Bit-masking support using address values.
- Registers for alternate function switching with pin multiplexing support.
- Thread-safe operation by providing separate set and clear addresses for control registers.
- Inputs are sampled using a double flip-flop to avoid metastability issues.

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Individual pins can be configured for LCD or DIO functions using registers, and then can be controlled using two separate mechanisms:

- Using the *LCD_DIO* registers
- Using the register set provided by the Cortex M0 core, therefore taking advantage of masked access and advanced interrupt control. DIO0 – DIO63 are managed by the Cortex M0 MPU core registers. To control DIO64 – DIO72, the *LCD_DIO* registers must be used.

External components such as LEDs, relay coils, etc. should be pulled low by a DIO pin, not driven high.

Wake pins, as well as the DIO72 and RMT_DRV_H pins must be pulled high or low in SLP and LCD-ONLY modes to prevent leakage.

LCD System

The SY7T213H supports up to 64 LCD SEG (segment) pins, and a total 8 COM pins (4 dedicated COM pins and 2 shared COM pins). The shared COM pins are:

- COM6/SEG21
- COM7/SEG22

The *LCD.MAPH* register controls the configuration for pins SEG32/DIO32 through SEG63/DIO63, the *LCD.MAPL* register controls SEG0/DIO0 to SEG31/DIO31. Each bit in these registers controls the configuration of its associated pin: When the bit is set, the pin is in LCD mode and acts as an LCD segment or COM pin. When cleared, the pin is in DIO mode and its function is controlled by the corresponding LCD segment register.

Key features of the LCD System are:

- Automated blinking without MPU interference is possible on two pins: SEG2 and SEG3. With 8 COM pins, this allows for a maximum of 16 blinking segments. The blink rate can be programmed to be 0.5Hz or 1.0Hz.
- Multiple LCD display pages. The device can cycle through a maximum of 31 pages of data at a programmable time interval of up to 32 seconds with 0.25 seconds resolution when the page DMA is enabled.
- LCD voltage can be the output of the LCD DAC, a fixed 3.3V voltage, or the voltage applied at the VLCD pin.

Communication Interfaces

UARTs

Six UARTs are available. UART3 is equipped with an optional optical encoder in transmit (TX3) direction and an optional IrDA decoder in the receive (RX3) direction.

SPI/I²C/µWire Masters

Two SPI master ports are available:

- For SPI M0, three pins are configurable for operation as SPI, I²C, or µWire master interfaces that can be used to connect EEPROMs, display controllers, and other peripheral devices.
- SPI M1 is the second master SPI port.

I2C Master Port

A separate I2C master port is available.

SPI Slave

The SPI slave port communicates directly with the internal AHB bus. It can read and write RAM and register locations. The hardware interface of the SPI slave port uses the SSCSB, SSCK, SSDI, and SSDO pins. These pins are multiplexed with LCD segment driver pins SEG17-SEG20 and are 5V-tolerant. To facilitate flash programming, cold start and reset cause the port pins to default to SPI mode. Interrupts to the Cortex M0 MPU core can be generated by the slave SPI port and both single-byte and multi-byte transactions are possible. In SSPI Safe Mode, SSPI write operations are disabled except for a 16-byte transfer region at address 0x2000_0400 to 0x2000_047F.

Real-Time Clock (RTC)

The RTC keeps accurate time based on the direct output of the 32.768KHz crystal oscillator. The resolution of the RTC output is 1/256th of a second. The RTC output is guaranteed to be monotonic, i.e., the RTC only increments, and cannot decrement due to calibration or temperature compensation. To maintain accuracy across temperature the RTC can be configured to periodically make temperature measurements and compensate the rate at which the RTC accumulates time.

The real-time clock (RTC) block includes a time-of-day clock plus a set of ancillary features to keep the clock accurate and to provide additional services to the system. The RTC include the following features:

- Weekday, date, month, year, seconds, minutes, hours registers with corresponding shadow registers for safe read and write operations
- Eight-bit sub-seconds register.
- Alarm register.
- Wake MPU core from SLP mode on a variety of events.
- Temperature measurement for RTC compensation.
- Third-order (cubic) temperature compensation hardware.

Timers and Counters

The SY7T213H comprises two separate timer modules with two timers each:

- Generic timers, Timer0 and Timer1, with inputs accessible through DIO pins
- Dual-input timers, Dtimer0 and Dtimer1

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Remote Driver Pins

The RMT_DRV_H and DIO72/RMT_DRV_L pins can be used to supply multiple capacitively coupled remote ICs, such as the SY7M007, via isolation transformers. Frequency and duty cycle are selectable via control registers.

PWM Output Pins

The DIO-SEG16/PWM0, DIO-SEG26/PWM2, DIO-SEG25/ PWM1, and DIO-SEG54/PWM3 pins can be configured as PWM outputs with selectable frequencies and duty cycles. The maximum frequency per output is 2.5MHz.

Analog Features

- Reference Voltage: The reference voltage is buffered. The buffer amplifier contains a chop circuit that eliminates temperature drift. The temperature coefficient of the reference voltage itself can be compensated. Typical CE Code features VREF compensation based on die temperature and typical VREF temperature coefficients using a quadratic equation.
- Temperature Sensor: An on-chip temperature sensor is provided. The temperature sensor can be used by the Cortex M0 MPU as part of the application code, but it also can support automatic periodic measurements in SLP mode. Temperature limits can be defined to trigger automatic wake ups from SLP mode.
  The temperature sensor reading (*stemp*) of the part is recorded in production and saved in the Info Block area of the Flash memory (*fuse_temp22*). Since temperatures at production may vary, this reference temperature is not accurate. It is recommended to average several *stemp* readings during meter calibration and store this value as $stemp_{CAL}$ in non-volatile memory as the accurate reference for any subsequent temperature measurements. Use the formula on page 18 to calculate the die temperature once $stemp_{CAL}$ has been established.
- Battery Monitor: The part can monitor the voltage on the two battery pins (V_{BAT} and V_{BAT_RTC}). A de-passivation current can be applied.

Functional Description and Operation

Metering Operation and Processes

Metrology tasks are handled by the Compute Engine (CE), which completely frees up the Cortex M0 MPU for communication, security, and general housekeeping tasks. Processing by the CE typically involves the following operations:

- DC offset removal
- Multiplication of each current sample with its associated voltage sample to obtain the energy per sample
- 90° phase shifter for VARh calculations
- Measurement of the input signal frequency and mains voltage zero crossing
- Monitoring of the signal amplitude for sag and swell detection
- Scaling of the processed samples based on calibration coefficients
- Monitoring of the die temperature
- Scaling of the processed samples based on temperature compensation information
- Accumulation of energy from all phases in fixed intervals for reporting to the host microcontroller
- Squaring and summation of voltage samples for V_{RMS} processing
- Squaring and summation of current samples for I_{RMS} processing
- Delay compensation for shunt sensors, phase compensation for CTs
- Pulse generation
- Extraction, suppression, or filtering of harmonics

Communication between CE and MPU is based on shared RAM.

Accumulation Interval

Metrology data are typically collected and integrated for one second and are then available to the Cortex M0 MPU via transfer registers residing in shared RAM. The integration time is configurable.

Calibration

The calibration process will largely depend on available calibration system hardware and implemented MPU code. All widely used calibration methods, e.g., absolute, ratiometric, multi-point, and auto-calibration, etc., are supported.

Temperature Compensation

For temperature compensation of the metrology, the voltage reference can be digitally compensated over changes in measured die temperature using a quadratic equation. The coefficients for the compensation equation can be generated from fuse settings contained in the Info Block area of the Flash memory. See the HRM (Hardware Reference Manual) and the Reference Manual of the used CE Code for details on temperature compensation.

Similarly, the RTC can be compensated for temperature based on crystal characteristics and die temperature. See the HRM for details.

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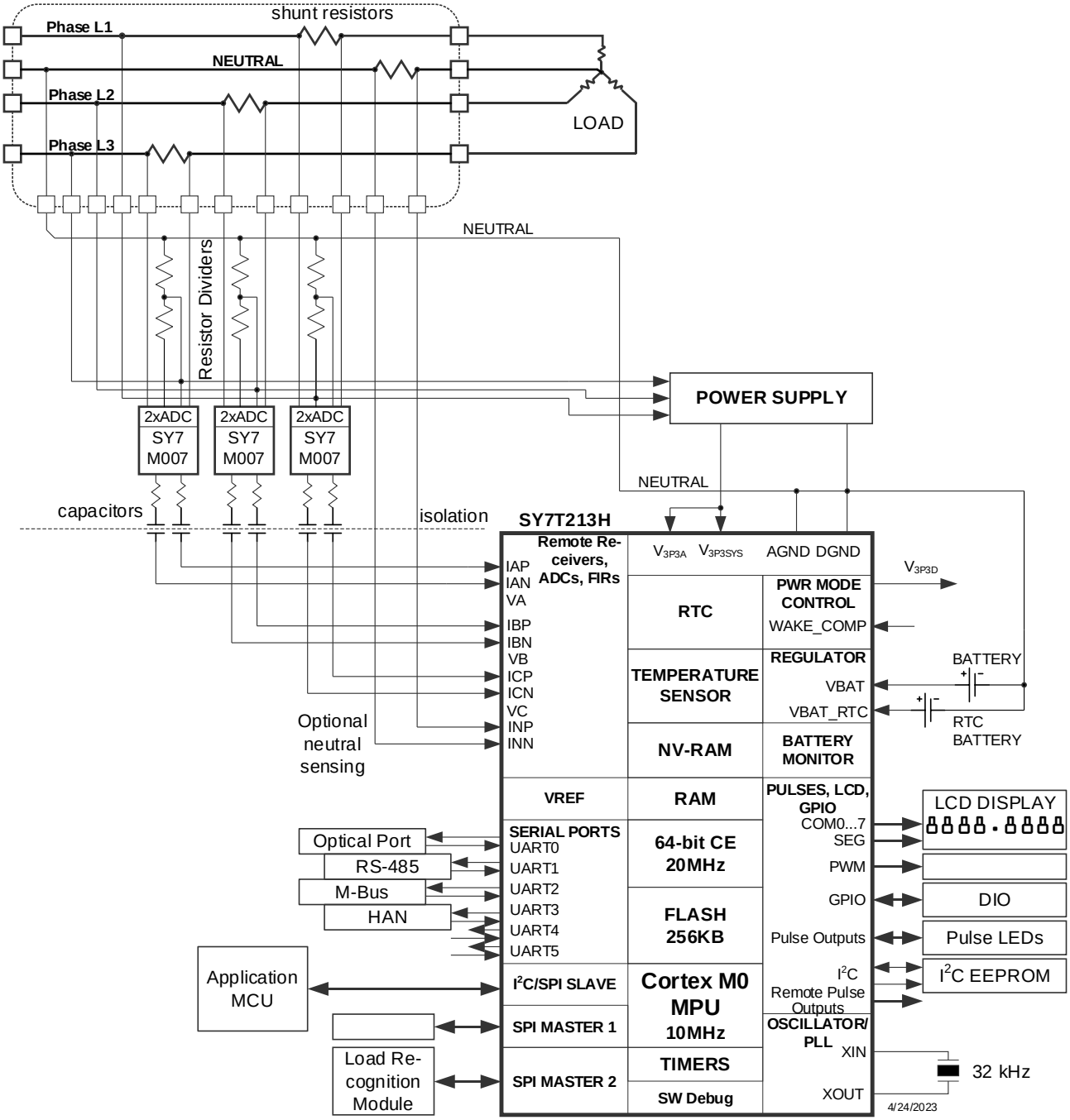
Application Diagrams

Polyphase Shunt Configuration with SY7M007 Remotes



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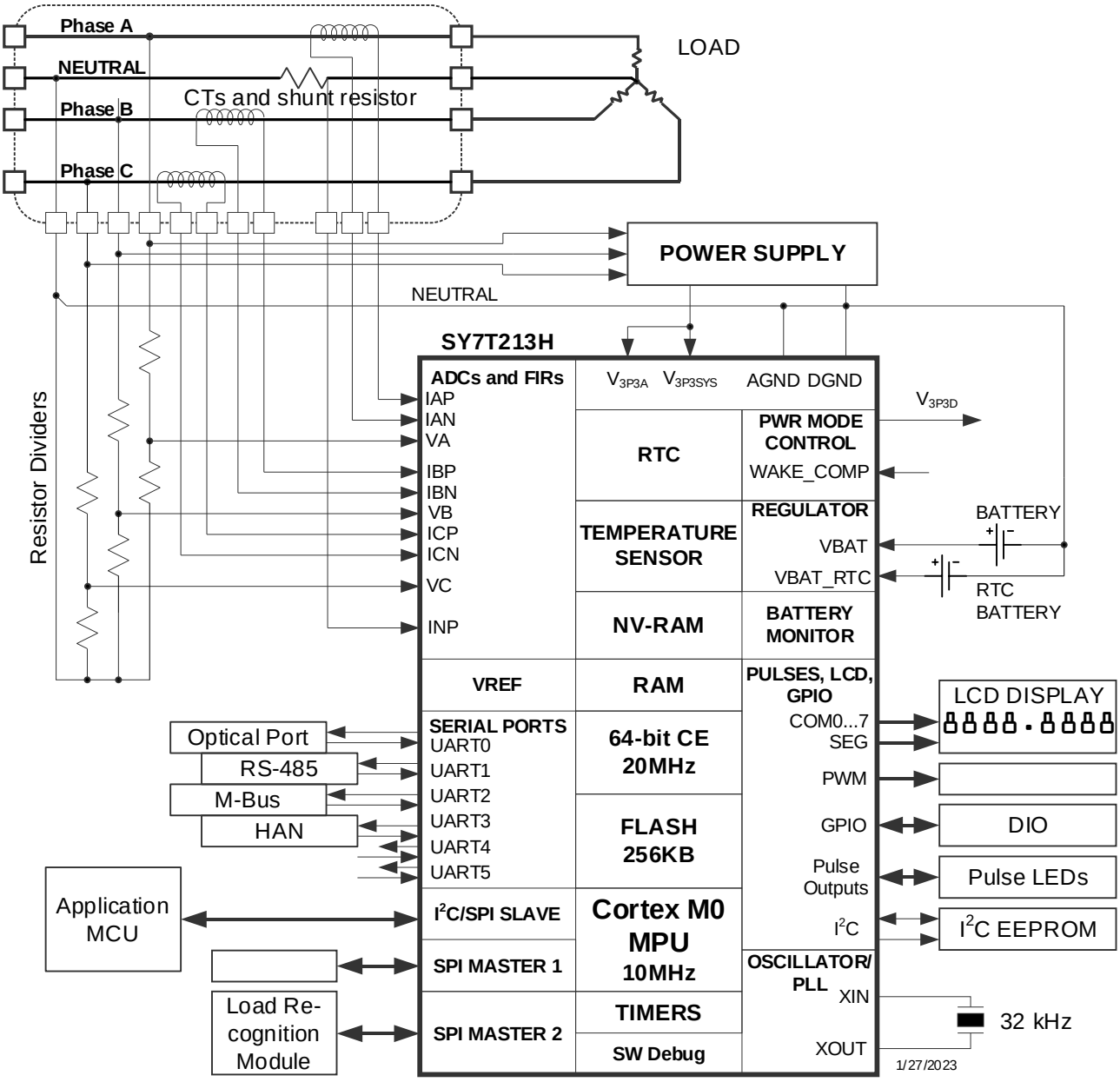
Polyphase CT Configuration



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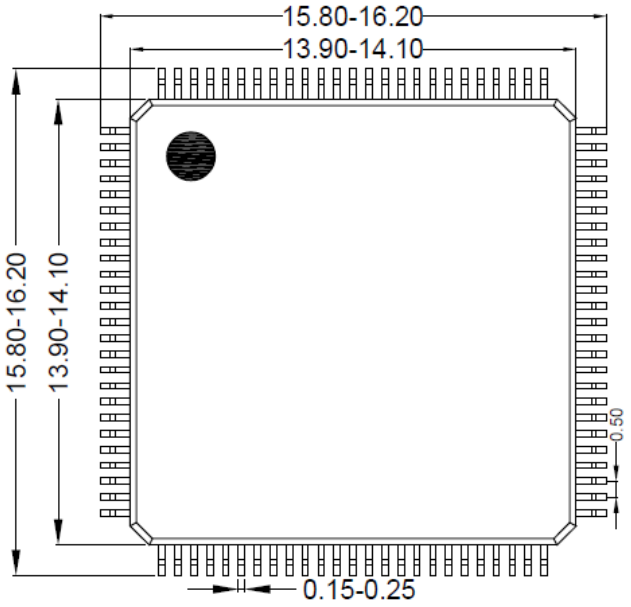
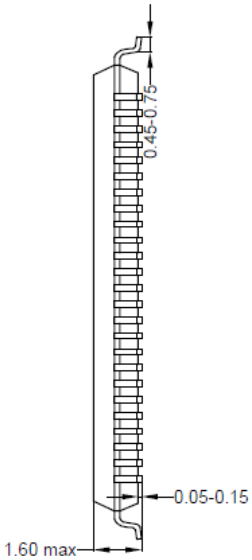
Package Drawings

100-LQFP

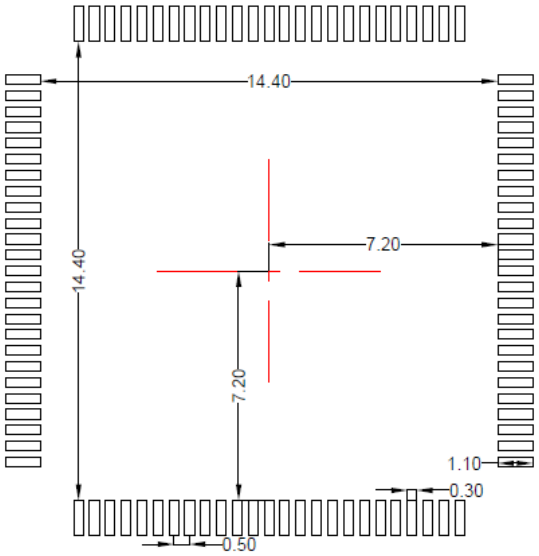


Top View



Side View

Front View



Recommended PCB layout

(only for reference)

Notes: All dimension in millimeter and exclude mold flash & metal burr.

Top View **Bottom View**

Front View **Recommended PCB Layout (reference only)**

Notes: All dimension in millimeter and exclude mold flash & metal burr.

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Package Marking

SY7T213H

TERIDIAN					
SY7T213H					
Rn	**y**	**y**	**w**	**w**	**z**

Rn Silicon revision

y y Last two digits of production year

w w Work week in production year (1 – 52)

z Last digit of assembly lot

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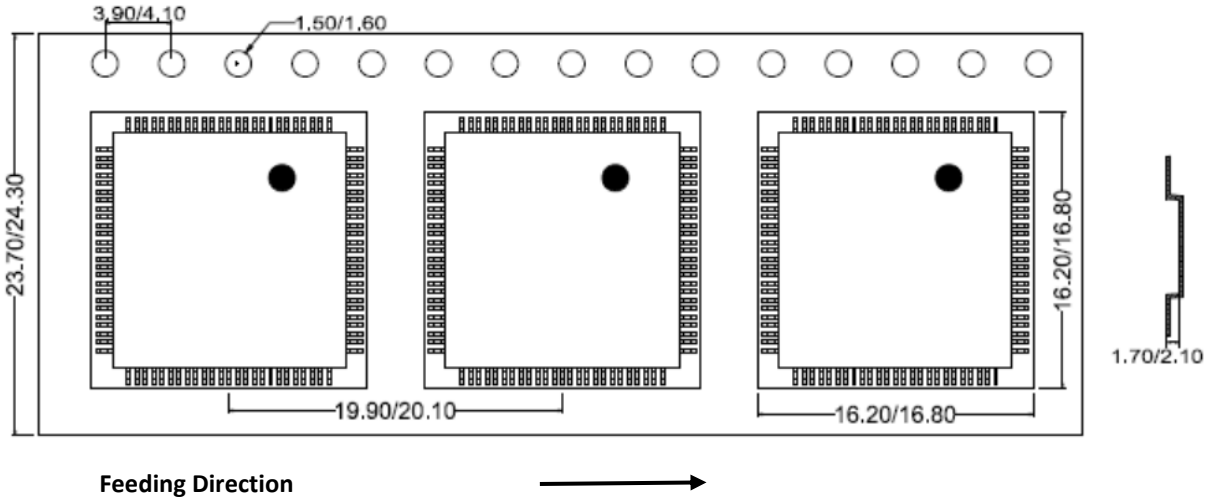
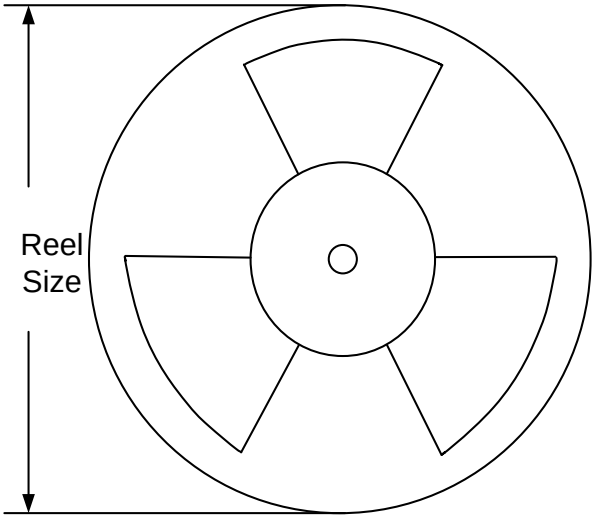
Tape Specifications

Tape Orientation - LQFP14x14-100



Carrier Tape & Reel specification for packages



Package type	Tape width (mm)	Pocket pitch (mm)	Reel size (Inch)	Trailer * length (mm)	Leader * length (mm)	Qty per reel (pcs)
LQFP14x14-100	24	20	13"	1400	1400	1000

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Revision History

Revision Number	Revision Date	Description	Pages changed
1.0	3/9/2023	Initial release	All
1.1	8/3/2023	Corrected package name (LQFP) Clarified definition of RX wake pins (RX0, RX1) Added table “Unused Pins” Corrected Thermal Ratings information Added Application Diagrams for CTs and for shunt/remotes	Many 1 9 11 29
1.2	10/24/2023	Corrected pin description table	6
1.3	9/22/2025	Updated values for capacitors at XIN/XOUT in Recommended External Components Updated TC1S and TC2S vales for bandgap specification Preamp input current is tested in production Removed comment ‘not tested’ from LCD DAC specifications	12 19 21 24

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