UM10508

230 V (AC) 17 W LED driver and dimmer Demo board using the SSL2102

Rev. 1 — 7 April 2016 User manual

Document information

Info	Content
Keywords	SSL2102, AC mains supply, dimmable LED driver, AC/DC conversion
Abstract	This User manual describes a demonstration (demo) board for evaluating an AC mains LED driver with a dimmer for 17 W, PAR38 LEDs using the SSL2102. It also describes key features and connections to aid the design of LED drivers for typical applications.

Revision history

Rev	Date	Description
v.1	20120116	first issue

1. Introduction

WARNING

Lethal voltage and fire ignition hazard

The non-insulated high voltages that are present when operating this product, constitute a risk of electric shock, personal injury, death and/or ignition of fire.

This product is intended for evaluation purposes only. It shall be operated in a designated test area by personnel qualified according to local requirements and labor laws to work with non-insulated mains voltages and high-voltage circuits. This product shall never be operated unattended.

This user manual describes a demo board for evaluating an AC mains LED driver with a dimmer for 17 W, PAR38 LEDs using the SSL2102. It describes key features and connections to aid the design of LED drivers for typical applications.

The demo board operates from an AC mains voltage of 230 V (AC) at 50 Hz. The resulting design is a trade-off between high-power factor, efficiency and dimmer compatibility, combined with high output stability and ElectroMagnetic Compatibility (EMC) compliance.

2. Safety Warning

The demo board is powered by AC mains voltage. Avoid touching the board when power is applied. An isolated housing is obligatory when used in uncontrolled, non-laboratory environments. The secondary circuit with LED connection has galvanic isolation, however this isolation is not in accordance with any standard and has not been thoroughly tested. Always provide galvanic isolation of the mains phase using a variable transformer. The following symbols identify isolated and non-isolated devices.

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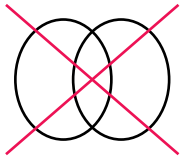

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a. Isolated

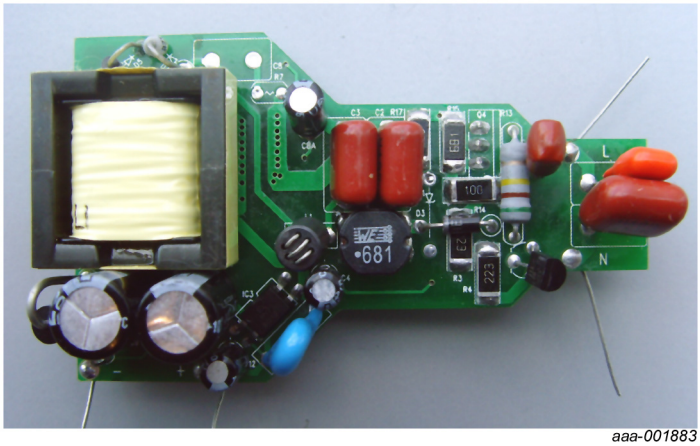
b. Non-isolated

Fig 1. Isolated and non-isolated symbols

3. Specification

Table 1. Demo board specification

Parameter	Value	Comment
AC line input voltage	210 V (AC) to 230 V (AC), ±10 %, 50 Hz	230 V (AC) model
Output voltage (LED voltage)	17 V (DC) to 33 V (DC)	
Output voltage protection	33 V (DC)	
Output current (LED current)	500 mA typical	
Input voltage and load current dependency	−5 % to +5 %, between 210 V (AC) and 250 V (AC)	
Output voltage and load current dependency	−10 % to +10 %, between 19 V (DC) to 30 V (DC)	
Temperature stability	−3 % to +3 % from −20 °C to +100 °C	
Current ripple	±15 % at 500 mA	typical value
Maximum output power (LED power)	19 W	depends on load
Efficiency	78 % to 82 %	
Power factor	>0.93 at 230 V (AC)	
Switching frequency	40 kHz to 60 kHz	at 230 V (AC) input voltage
Dimming range	100 % to 0 %	for triac dimmers
Board dimensions	82 mm × 62 mm × 35 mm	L × B × H
Operating temperature	0 °C to 105 °C	-
EMC Compliance	FCC15 and IEC 61000-3-2 pre-compliant EN 55015 and IEC 61000-3-2 pre-compliant	



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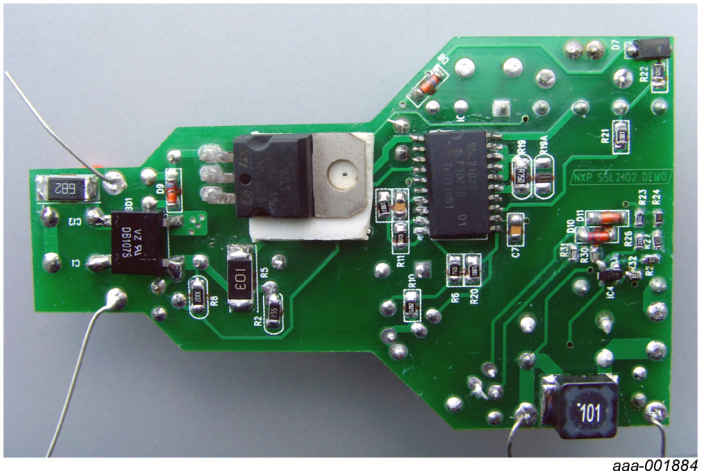
a. Top view.



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b. Bottom view.

Fig 2. 17 W PAR38 LED demo board

4. Demo board connections

The demo board is optimized for an AC mains source of 120 V (60 Hz). It is designed to work with multiple high-power LEDs having a total working voltage of between 18 V and 33 V. The output current is set to 600 mA at typical load. The output voltage is limited to 33 V.

When attaching an LED load to the board (hot plugging), an inrush peak current occurs due to the discharge of output capacitors C9 and C10. Frequent discharges can damage or deteriorate the LEDs.

Remark: Mount the board in a shielded or isolated box for demonstration purposes.

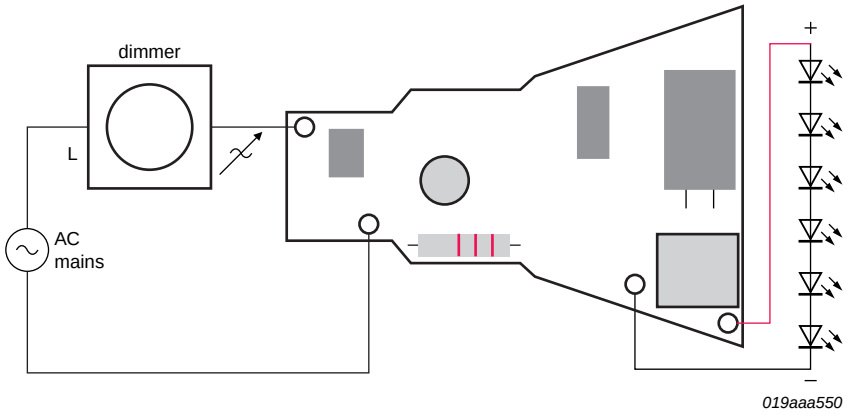


Fig 3. Demo board connections

Place a galvanic isolated transformer between the AC source and the demo board, if one is used. Connect a series of between 5 and 10 LEDs to the output as shown in Figure 3.

5. Dimmer compatibility

Silergy Corp. has tested the performance of several triac-based dimmers having different specifications. The range of dimmers which have been tested with the demo board are given in Table 2.

Table 2. Tested dimmers
An incandescent lamp is used as load.

Manufacturer	Type	Voltage (V)	Power range (W)	Trigger	High dim level (%)	Low dim level (%)
LK	DG07103	230	400	[1]	91.5	6.5
Italy	DG04027	220 to 240	60 to 400	[1]	90	3
BG_British	BG general	200 to 250	60 to 500	[1]	88	13
Legrand	V8051	220	40 to 300	[1]	97	1.5
JingNeng	JN2301	230	50 to 400	[1]	80	0.5
Meierte	PDDT	230	630	[1]	98	0.2
ShiToneSB	DIM	230	300	[1]	96	0
CLIPSAL	32E450UDM	220 to 240	450	[2]	89	7.5
Busch-Jaeger Elektro	6513 U-102	230	40 to 420	[2]	92.5	15
HPM	CAT700T	230 to 240	10 to 700	[2]	90	8.7

[1] Leading edge.

[2] Trailing edge.

6. Functional description

Refer to Figure 4 “Demo board 230 V (AC) schematic” on page 12 for more information.

The AC mains LED driver IC SSL2102 controls and drives a flyback converter circuit and ensures correct dimmer operation. The IC has three integrated high-voltage switches, one of which, located between pins DRAIN and SOURCE, controls flyback input power. When the switch opens, current flows and is stored as energy in transformer TX1. The current is interrupted when either:

- the duty factor exceeds the 75 % maximum level set using the PWMLIMIT pin
- the voltage on the SOURCE pin exceeds 0.5 V

In the next cycle, the energy stored in the transformer discharges via D6 to output capacitors C9 and C10. The load absorbs the energy. The external RC components connected to pins RC and RC2 control the internal oscillator timing. These external components set the flyback converter frequency. The upper and lower frequency values are set using the BRIGHTNESS pin. The ratio between R11 and R12 sets flyback converter frequency range.

The two other switches in the IC are called weak-bleeder (pin WBLEED) and strong-bleeder (pin SBLEED). When the voltage on these pins is below a certain value, typically 52 V, the strong-bleeder switches on. A path is provided for the load current to the dimmer during zero voltage crossing. The dimmer timer is reset. When the voltage on the pins is above 52 V and the voltage on pin ISENSE > −100 mV, transistor Q3 switches the weak-bleeder on. The weak-bleeder supplies a boosted (hold) current to the dimmer to maintain stable latching when the flyback converter draws insufficient current.

Figure 4 shows the bleeder voltage against time in dimmed and undimmed modes.

The demo board is optimized to work at a power factor above 0.9. The flyback converter operates during the MOSFET on-time. Capacitors C9 and C10 buffer the flyback converter output power. This configuration gives the circuit a resistive input current behavior in undimmed mode; see curve I_I in Figure 4.

In dimmed mode, the dimmer latch and hold current must be maintained. In addition, add a damper to reduce the inrush current and dissipate the electric power stored in the dimmer LC filter.

A serial resistor is used as a damper at power ranges of less than 10 W. However, a resistor is inefficient at higher power ranges. This effect is due to the significant voltage drop and dissipation that occurs from the supply current to the flyback converter.

The Darlington transistor Q4 provides the necessary high gain. Q4 is saturated while its base voltage is higher than the emitter voltage plus the base-emitter voltage (V_{BE}). The voltage across emitter resistor R14 increases with the current. When the emitter voltage rises above the threshold, Q4 stops saturation, turns off and R15 limits the current. Choose the values of D9 and R13 with care to ensure consistent operation. A Darlington transistor provides the necessary high current gain. This modification changes the specifications of efficiency and power factor.

A combination of serial resistance and a parallel damper is chosen. The serial resistance comprises R14, R15 and R17. The parallel group damper comprises C1, C13 and R1 in parallel with C8 and R7 for optional fine-tuning. To improve efficiency, the major serial damping is activated only when there is a peak inrush current (active inrush current limiter). In normal operation, the Darlington transistor Q4 conducts, bypassing R15 and lowering ohmic losses. When a high inrush current is detected, Q4 starts to clip at its maximum current of 500 mA.

The flyback converter input circuit must have a filter that is partially capacitive. C2, L2, C3, C13 and L1 form a filter that blocks most of the disturbance caused by the flyback converter input current. The drawback of this filter is a reduced power factor due to the capacitive load. A lower flyback converter power relative to the capacitive value of this filter/buffer reduces the power factor. With the 230 V (AC) design using 330 nF capacitors, a minimum power factor of 0.93 is achieved.

The demo board has a feedback loop to limit the output current. The feedback loop senses the LED current through sense resistor R25, and current mirror circuit with IC4. The current level can be set using R27 and R29. The same feedback loop is also used for overvoltage protection. If the LED voltage exceeds 33 V, a current starts to flow through R23 and D11. The current through the optocoupler IC3 forces pins PWMLIMIT and BRIGHTNESS LOW. At a value below 400 mV, the MOSFET on-time is zero.

The feedback loop has a proportional action only. The gain is critical because of phase shift caused by the flyback converter and C6.

The relationship between pin PWMLIMIT and the output current is quadratic in nature. The resulting output current spread is acceptable for most LED applications. If higher demands are placed on LED current spread, a secondary regulation circuit in combination with an added pure current action control is advisable.

The dimming range is detected by sensing the average rectified voltage. R2 and R10 form a voltage divider, and C4 filters the resulting signal. The flyback converter sets its duty factor and converter frequency accordingly.

7. System optimization

The modifications described in this section can be applied to achieve customer application specifications.

7.1 Changing output voltage and LED current

One of the major advantages of a flyback converter over other topologies is its suitability for driving different output voltages. In essence, changing the winding ratio while maintaining the value of the primary inductance shifts the output working voltage accordingly. Part of the efficiency of the driver is linked to the output voltage. A lower output voltage increases the transformation ratio and cause higher secondary losses. In practice, mains dimmable flyback converters have an efficiency of:

- 85 % for higher output power and voltage such as 60 V
- 60 % for lower output power and voltage such as 1 W and 3 V

At lower voltages, synchronous rectification is advisable to reduce losses after high current is rectified. Silergy Corp. TEA1761 and TEA1791 synchronous rectification controllers are ideal for this purpose. Calculations for transformer properties and peak current are described in detail in application note *AN10754, SSL2101 and SSL2102 dimmable mains LED driver*.

7.2 Changing the output ripple current

The LED voltage, The LED dynamic resistance and the output capacitor determine the output ripple current. While the values of C9 and C10 are chosen to optimize capacitor size with light output. A ripple of ±15 % results in an expected deterioration of LED brightness of less than 1 %[1].

The size of the buffer capacitor is determined using Equation 1.

$$C10 + C9 = \frac{I_{led}}{\Delta I} \times \frac{1}{6 \times f_{net} \times R_{dyn}} \quad (1)$$

Example:

A ±5 % ripple current, a 50 Hz AC mains frequency and a 0.6 Ω dynamic resistance, results in a combined C9 + C10 value of $\frac{20}{300 \times 0.6} = 111\ mF$.

A ripple current of 25 % and a dynamic resistance of 6 Ω, results in a value for C9 + C10 of $\frac{4}{(300 \times 6)} = 2200\ \mu F$.

Using a series of LEDs, the dynamic resistance of each LED can be added to the total dynamic resistance.

1. M. Weiland 28-07-2006

7.3 Adapting to high-power reverse phase transistor dimmers

Reverse phase (transistor) dimmers differ in two ways that can be beneficial:

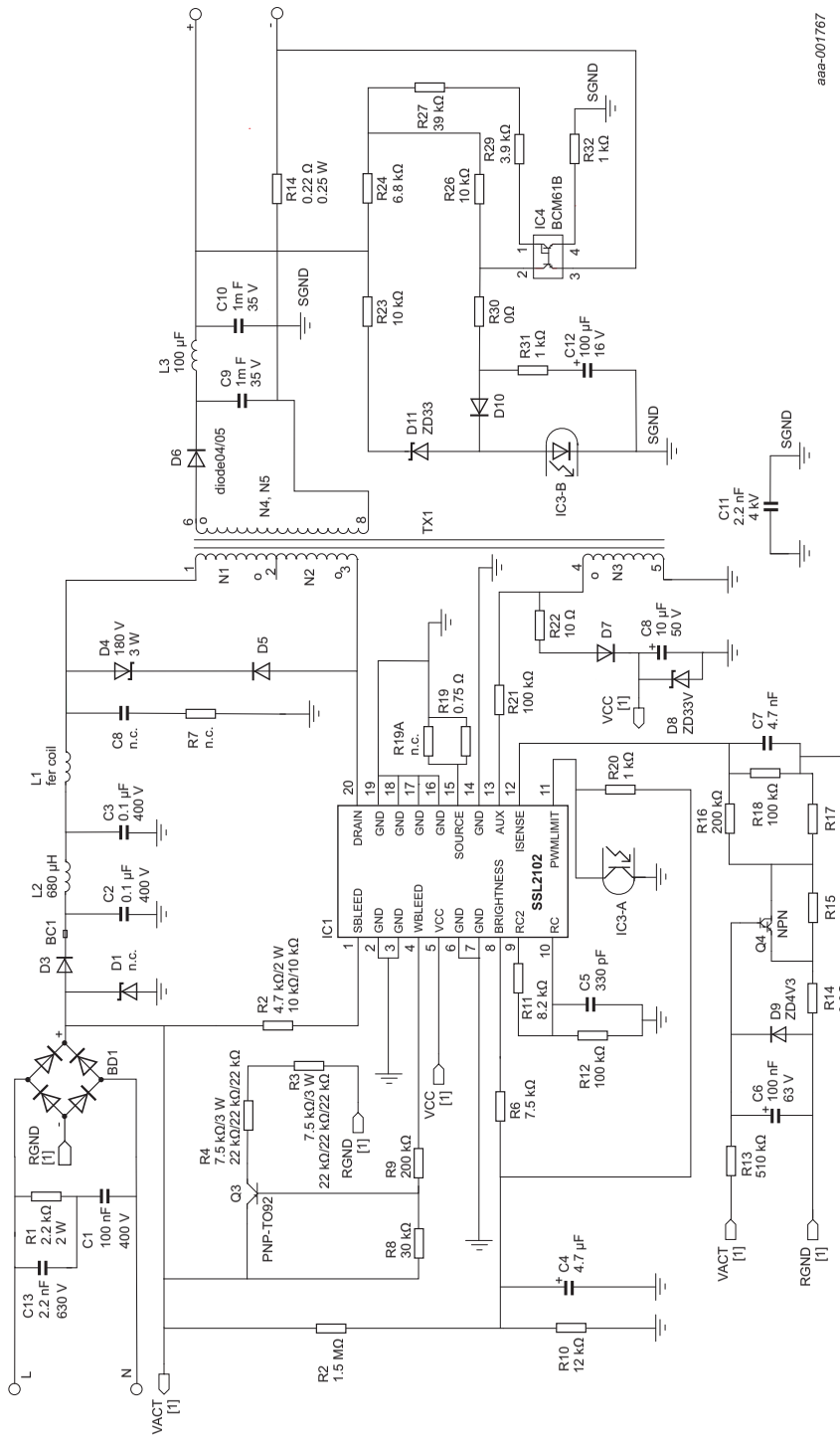
- Due to the negative phase, there is no inrush current when the dimmer triggers. Using triac dimmers, there is a sudden voltage difference over the input, resulting in a steep charge of the input capacitors. The resulting peak current results in higher damper dissipation. Using transistor dimmers, the steep charge is missing. The input capacitors are less stressed and the input circuit is less prone to audible noise.
- Transistor dimmers contain active circuitry that requires a load charge while the dimmer is open. To avoid internal dimmer losses, the dimensioning of the internal supply voltage generation circuit is critical. This means that the remaining voltage drop across the lamp must be low enough to allow this charge to be reached. The minimum load to achieve such a low voltage drop results in inefficient operation at low output power levels. The cause of which is that most of the energy is wasted driving the dimmer instead of used to producing light.

The weak-bleeder resistor values of R3 and R4 are chosen to ensure that any losses are within acceptable limits. These losses only occur in dimmed mode at the end of the phase. The voltage drop in some transistor dimmers is not sufficient for full control of the dimming range. The SSL2102 senses the dimming range by taking the average rectified voltage as input. To compensate for the reduced voltage difference, the voltage detection can be made more sensitive by placing a Zener diode in series with R2. The dimming curve is steeper and shifted when using triac dimmers because of increased sensitivity.

7.4 Changing the output current

The output current can be set initially by varying the values of R29 and R27. The power section and transformer train can withstand output currents up to 500 mA, but losses increase at higher current levels. Resistors R19A/R19B limit the primary peak current and consequently the maximum output power.

8. Demo board schematic



(1) Optional.

Some resistor values are shown with format x/x/x which represent the values required of resistors connected in parallel.

Fig 4. Demo board 230 V (AC) schematic

9. PCB components

Table 3. Demo board 230 V (AC) components

Reference	Quantity	Description	Part	Comment
BD1	1	bridge diode	DB107S	-
C1	1	100 nF; 400 V	CM150-5_6X12	EMI
C2; C3	2	Pi-filter; 0.1 μF; 400 V	CM150-5_6X18	-
C4	1	V_{CTRL} > 105 °C; 4.7 μF; 50 V	CAL04/5	-
C5	1	C_{osc}; 330 pF; 0805C	-	-
C6	1	330 nF; 50 V	CAL04/5	active damper on
C7	1	4.7 nF; 0805C	-	WBLEED on; noise
C8A	1	V_{CC} > 105 °C; 10 μF; 50 V	CAL04/5	-
C9; C10	2	1 mF; 35 V; > 105 °C; ECOUT	-	
C11	1	Y-capacitor; 2.2 nF; 400 V	-	-
C12	1	100 μF; 16 V	CAL04/5	time control CC_OCP on
C13	1	2.2 nF; 630 V	CM150-5_6X12	EMI
D1	0	Zener diode; 250 V	P6KE250	-
D3	1	diode; 02/10	HER107	-
D4	1	Zener diode; 180 V; 3 W; DIP2	BZT030180	-
D5	1	diode; DIP2	HER107	-
D6	1	diode; DIP2	HER303	-
D7	1	diode; SO8	IN4148	-
D8	1	Zener diode	ZD33V	-
D9	1	Zener diode; 4.3 V; SMD; SOD80	-	-
D10	1	diode; SO8	IN4148	-
D11	1	Zener diode	ZD33V	-
IC1	1	IC; SO20	SSL2102	-
IC3	1	optocoupler; IC04-10/PC	LTV-817B	-
IC4	1	current mirror	BCM61B	-
L1	1	EMI MHz level	FERCHOCK	W.E. BEAD
L2	0	WECHOCK; 680 μH; SMD	-	-
L3	1	WECHOCK-2; 100 μH; SMD	-	-
Q3	1	PNP transistor; TO92	KSP92	-
Q4	1	NPN transistor; TO220	ST901T	-
R1	3	6.8 kΩ; R-POWER; 2.2 kΩ; 2 W; SMD	-	three in parallel
R2	1	1.5 MΩ; 5 %; 1206	-	tune for maximum on V_{CTRL}
R3; R4	6	22 kΩ; R-POWER; 15 kΩ; 3 W; SMD	-	three in parallel
R5	2	10 kΩ; R-POWER; 4.7 kΩ; 2 W; SMD	-	two in parallel
R6	1	7.5 kΩ; 0805	-	tune for dimming curve
R8	1	30 kΩ; 1206	-	hold current compensation
R9	1	200 kΩ; 1206	-	hold current compensation
R10	1	12 kΩ; 0805	-	tune for minimum off V_{CTRL}
R11	1	C_{osc}; 0805; 8.2 kΩ	-	-

Table 3. Demo board 230 V (AC) components *…continued*

Reference	Quantity	Description	Part	Comment
R12	1	100 kΩ; 0805	-	R18 WBLEED on
R13	1	390 kΩ; RT3.5MM-1W; DIP	-	DIP
R14	3	10 Ω; RT5MM; 3.3 Ω; 2 W; SMD	-	three in parallel
R15	2	680 Ω; RT5MM; 330 Ω; 2 W; SMD	-	two in parallel
R16	1	200 kΩ; 0805	-	WBLEED on
R17	3	20 Ω; RT5MM; 10 Ω; 2 W; SMD;	-	two in parallel
R18	1	100 kΩ; 0805	-	-
R19	1	0.75 Ω; 1 %; 1206	-	tune for I_{pk};
R20	1	1 kΩ; 0805	-	tune for dimming curve
R21	1	100 kΩ; 0805	-	-
R22	1	10 Ω; 0805	-	VCC noise
R23; R26	2	10 kΩ; 0603	-	tune for CC_OCP
R24	1	6.8 kΩ; 0603	-	current limit
R25	1	0.22 Ω; 0.25 W; 1 %; DIP; RT3.5MM	-	DIP
R27	1	51 kΩ; 0603	-	tune for CC_OCP
R29	1	3.9 kΩ; 0603	-	tune for CC_OCP
R30	1	0 Ω; 0603	-	-
R31; R32	2	1 kΩ; 0603	-	tune for CC_OCP
TX1	1	transformer; 1 mH; EFD25-DIP	Würth Elektronik	-

10. Test results

10.1 Input and output stability

Table 4. Input and output stability test results

No. Board	V_{IN} (V (AC))	P_I (W)	PF	V_o (V)	I_o (A)	P_o (W)	η (%)
1	230	17.87	0.936	29.1	0.503	14.6373	81.9099
2	230	17.56	0.932	29	0.487	14.123	80.42711
3	232	17.79	0.933	29	0.495	14.355	80.6914
4	230	17.25	0.938	29	0.489	14.181	82.2087
5	232	17.79	0.933	29.1	0.499	14.5209	81.62395
6	229	17.48	0.943	29	0.493	14.297	81.79062
7	229	17.45	0.934	29	0.499	14.471	82.92837
8	229	17.48	0.934	29	0.492	14.268	81.62471
9	230	17.48	0.935	29	0.493	14.297	81.79062
10	230	17.48	0.93	29	0.499	14.471	82.78604
11	231	17.56	0.928	29	0.497	14.413	82.07859
12	230	17.51	0.94	29	0.494	14.326	81.81611
13	232	17.25	0.943	29	0.487	14.123	81.87246
14	229	17.58	0.935	29	0.496	14.384	81.82025
15	229	17.21	0.92	29	0.484	14.036	81.55723
16	229	17.39	0.936	29	0.491	14.239	81.88039
17	231	17.68	0.932	29.1	0.501	14.5791	82.46097
18	231	17.67	0.934	29.1	0.498	14.4918	82.01358
19	229	17.56	0.939	29	0.496	14.384	81.91344
20	231	17.48	0.931	29	0.491	14.239	81.45881