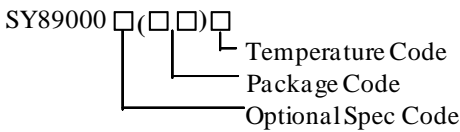


### General Description

The SY89000 develops a high efficiency synchronous step-down DC/DC converter capable of delivering 0.6A current. The SY89000 operates over a wide input voltage range from 7V to 100V and integrates main switch and synchronous switch with very low  $R_{DS(ON)}$  to minimize the conduction loss. The SY89000 always operates under continuous condition mode. The device adopts the instant PWM architecture to achieve fast transient responses for high step down applications.

### Ordering Information



Ordering Number	Package type	Note
SY89000FCC	SO8E	--

### Features

- Low  $R_{DS(ON)}$  for Internal Switches (Top/Bottom): 500mΩ/285mΩ
- 7~100V Input Voltage Range
- 0.6A Output Current Capability
- Constant On-time Control
- Instant PWM Architecture to Achieve Fast Transient Responses
- Programmable Switching Frequency Range: 200kHz~600kHz.
- 2ms Internal Soft-start Limits the Inrush Current
- Precise  $\pm 2\%$  1.225V Reference over  $-40^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$  Temperature Range
- Cycle-by-cycle Peak Current Limit
- Over Temperature Protection with Auto Recovery
- RoHS Compliant and Halogen Free
- Compact Package SO8E

### Applications

- Isolated Telecom Bias Supply
- Secondary High Voltage Post Regulator
- Automotive Systems

### Typical Applications

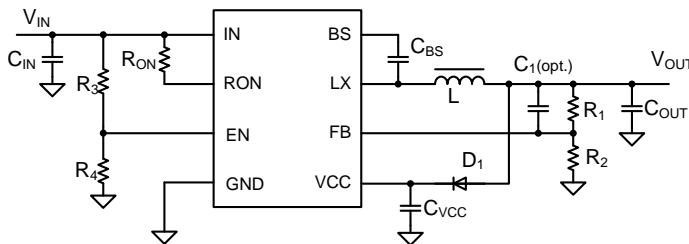


Figure1. Schematic Diagram

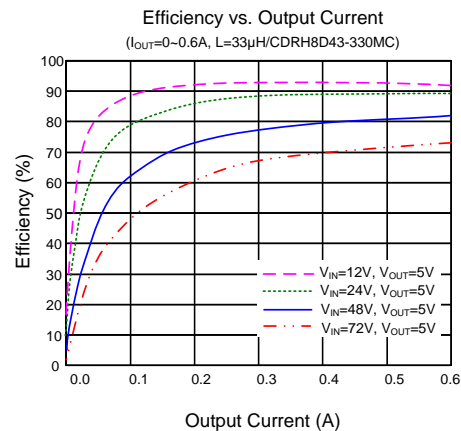
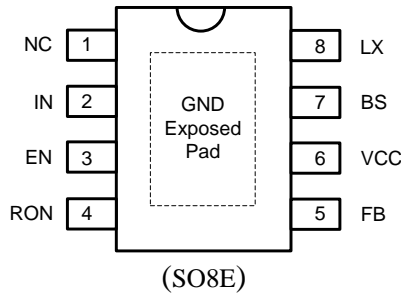


Figure2. Efficiency vs. Output Current

## Pinout (top view)



Top Mark: **CTBxyz** (Device code: CTB; *x=year code, y=week code, z=lot number code*)

Pin Name	Pin Number	Pin Description
NC	1	Not connected.
IN	2	Input pin. Decouple this pin to GND with a low ESR ceramic capacitor.
EN	3	Enable control pin. This pin can also be used for programming $V_{IN}$ turn on voltage with the resistor divider. The device has an accurate 1.225V rising threshold.
RON	4	Connect a resistor from this pin to the IN to set the top switch ON time. The switching frequency can be calculated using the following equation: $f_s \text{ (kHz)} = \frac{11 \times V_{OUT} \text{ (V)} + 500}{R_{ON} \text{ (M}\Omega\text{)}}$
FB	5	Output feedback pin. Connect this pin to the center point of the output resistor divider (as shown in Figure 1) to program the output voltage: $V_{OUT} = 1.225 \times (1 + R_1/R_2)$
VCC	6	Supply input of internal LDO.
BS	7	Boot-Strap Pin. Supply high side gate driver. Connect a 0.1 $\mu\text{F}$ ceramic capacitor between the BS pin and the LX pin.
LX	8	Inductor pin. Connect this pin to the switching node of inductor.
GND	Exposed Pad	Ground pin.

## Block Diagram

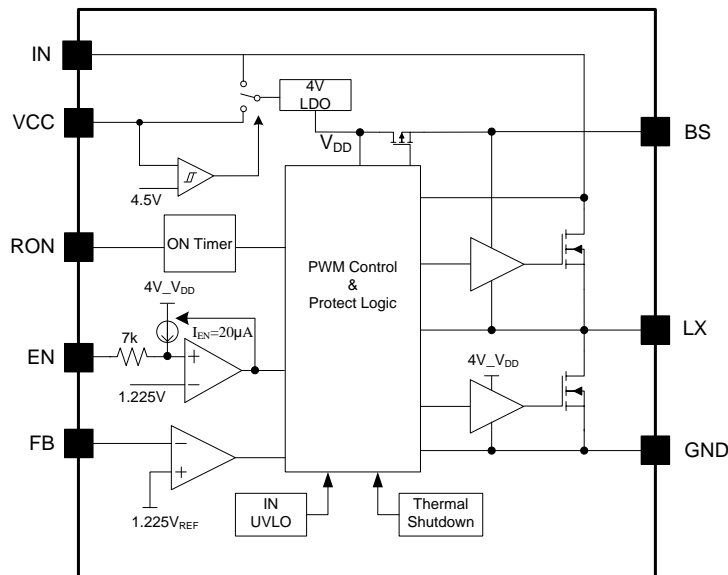


Figure3. Block Diagram



**Absolute Maximum Ratings** (Note 1)

IN -----	-0.3V to 100V
EN, RON -----	-0.3V to $V_{IN} + 0.3V$
LX -----	-0.7V to $V_{IN}+0.3V$
BS-LX -----	-0.3V to 6V
FB Voltage -----	-0.3V to 6V
VCC -----	-0.3V to 30V
Power Dissipation, $P_D$ @ $T_A = 25^\circ C$ SO8E -----	3.3W
Package Thermal Resistance (Note 2)	
$\theta_{JA}$ -----	30°C/W
$\theta_{JC}$ -----	10°C/W
Junction Temperature Range -----	-40°C to 150°C
Lead Temperature (Soldering, 10 sec.) -----	260°C
Storage Temperature Range -----	-65°C to 150°C
Dynamic LX voltage in 50ns Duration -----	$V_{IN}+3V$ to GND-5V

**Recommended Operating Conditions** (Note 3)

Supply Input Voltage -----	7V to 100V
Junction Temperature Range -----	-40°C to 125°C
Ambient Temperature Range -----	-40°C to 85°C

## Electrical Characteristics

( $V_{IN}=48V$ ,  $V_{OUT}=5V$ ,  $L=33\mu H$ ,  $C_{OUT}=10\mu F$ ,  $I_{OUT}=0.6A$  unless otherwise specified. Typical value correspond to  $T_J=25^\circ C$ . Minimum and maximum limits apply over  $-40^\circ C$  to  $125^\circ C$  junction temperature range.)

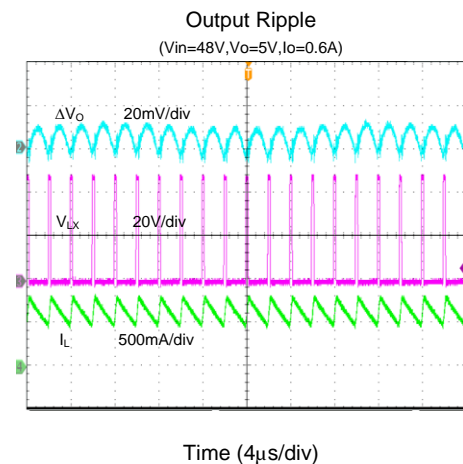
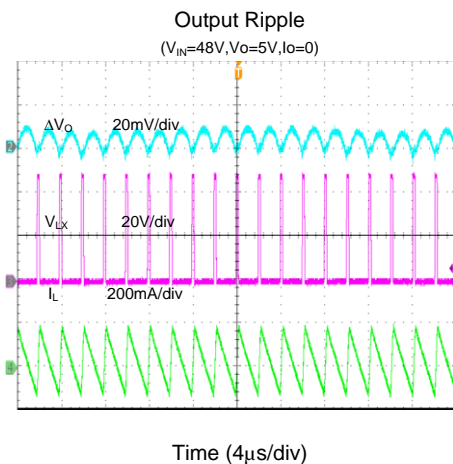
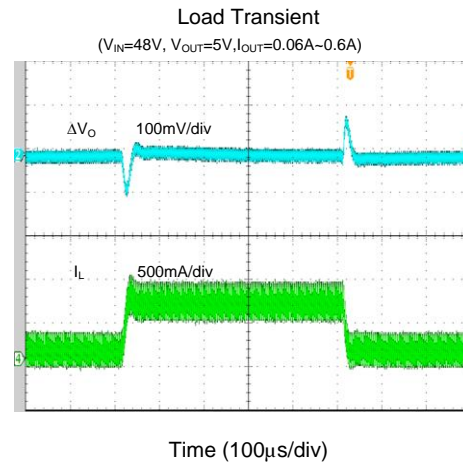
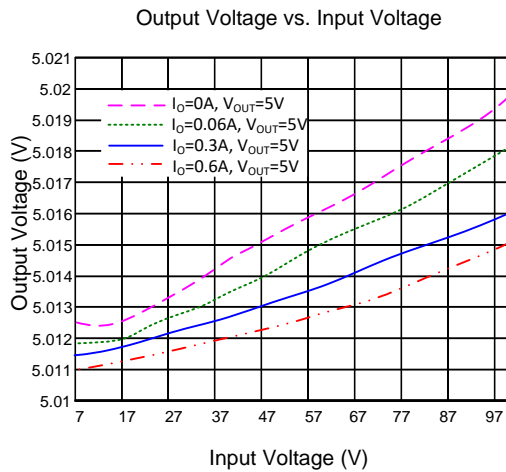
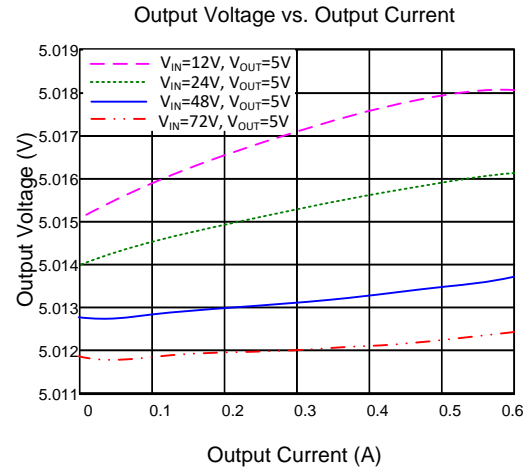
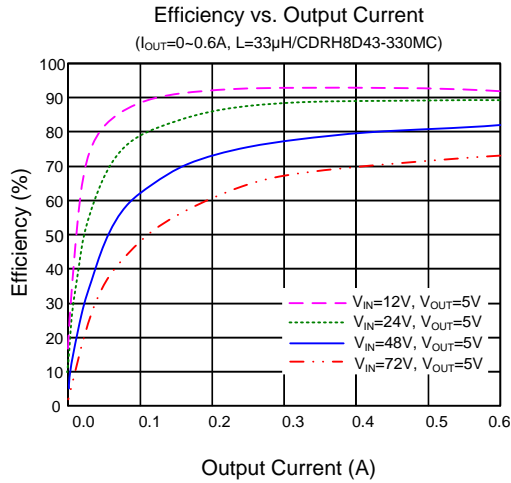
Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Input Voltage Range	$V_{IN}$		7		100	V
Input UVLO Rising Threshold	$V_{IN,UVLO}$		5.8	6.3	6.8	V
Input UVLO Hysteresis	$V_{HYS}$			0.25		V
Shutdown Current	$I_{SHDN}$	EN=0		8	30	$\mu A$
Feedback Reference Voltage	$V_{REF}$		1.2	1.225	1.25	V
FB Input Current	$I_{FB}$	$V_{FB}=3.3V$	-50		50	nA
Top FET RON	$R_{DS(ON)1}$			500		m $\Omega$
Bottom FET RON	$R_{DS(ON)2}$			285		m $\Omega$
Top FET peak Current Limit	$I_{LIM, TOP}$		0.9	1.2	1.5	A
Bottom FET Valley Current Limit	$I_{LIM, BOTTOM}$		0.6	0.8	1	A
Negative Current Limit	$I_{LIM, NEG}$		-480	-650	-820	mA
VCC Input Rising UVLO Threshold	$V_{VCC, UVLO}$			4.5		V
VCC Input UVLO Hysteresis	$V_{VCC, HYS}$			0.3		V
EN Rising Threshold	$V_{EN}$		1.185	1.225	1.265	V
EN Hysteresis Input Current	$I_{EN, HYS}$		-10	-20	-29	$\mu A$
Switching Frequency	$f_{OSC}$	$V_{IN}=48V$ , $R_{ON}=1.1M\Omega$	350	500	650	kHz
Min ON Time	$t_{ON}$			90		ns
Min OFF Time	$t_{OFF}$			200		ns
Thermal Shutdown Temperature	$T_{SD}$			150		$^\circ C$
Thermal Shutdown Hysteresis	$T_{HYS}$			15		$^\circ C$

**Note 1:** Stresses beyond the “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

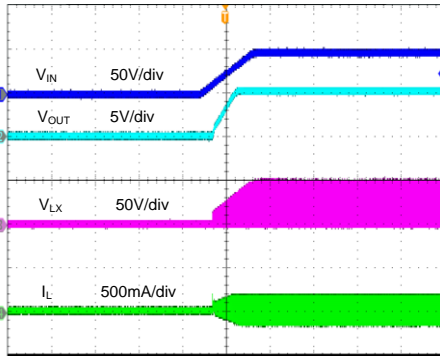
**Note 2:**  $\theta_{JA}$  is measured in the natural convection at  $T_A = 25^\circ C$  on a low effective 4-layer thermal conductivity test board of JEDEC 51-3 thermal measurement standard. Paddle of SO8E packages is the case position for  $\theta_{JC}$  measurement.

**Note 3:** The device is not guaranteed to function outside its operating conditions.

## Typical Performance Characteristics

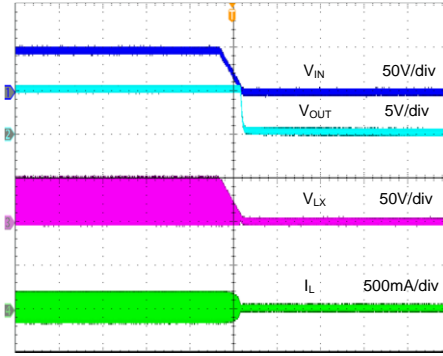


Startup from  $V_{IN}$   
( $V_{IN}=48V$ ,  $V_{OUT}=5V$ ,  $I_{OUT}=0A$ )



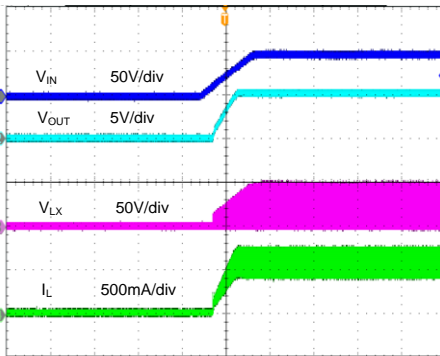
Time (4ms/div)

Shutdown from  $V_{IN}$   
( $V_{IN}=48V$ ,  $V_{OUT}=5V$ ,  $I_{OUT}=0A$ )



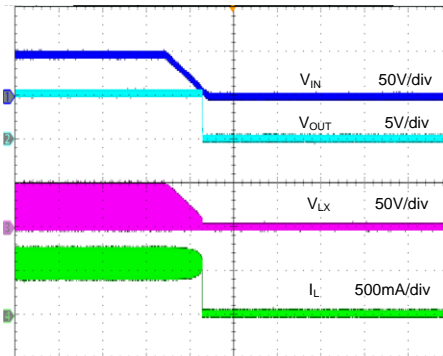
Time (200ms/div)

Startup from  $V_{IN}$   
( $V_{IN}=48V$ ,  $V_{OUT}=5V$ ,  $I_{OUT}=0.6A$ )



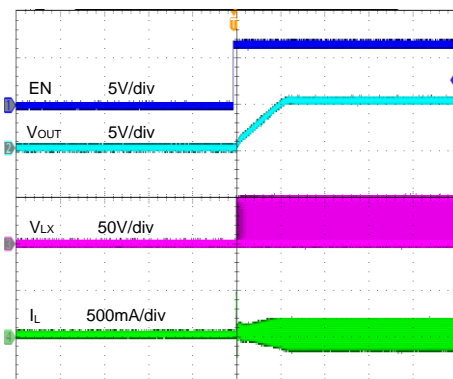
Time (4ms/div)

Shutdown from  $V_{IN}$   
( $V_{IN}=48V$ ,  $V_{OUT}=5V$ ,  $I_{OUT}=0.6A$ )



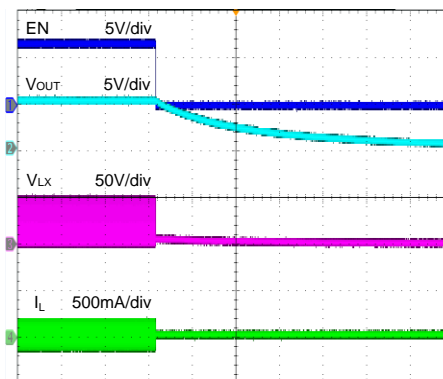
Time (100ms/div)

Startup from EN  
( $V_{IN}=48V$ ,  $V_{OUT}=5V$ ,  $I_{OUT}=0A$ )



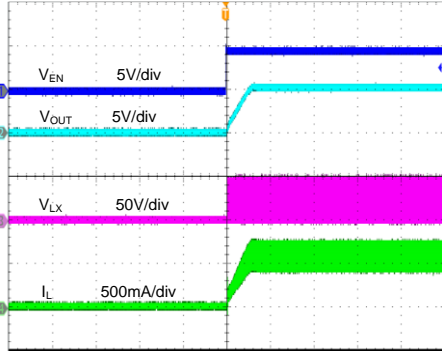
Time (2ms/div)

Shutdown from EN  
( $V_{IN}=48V$ ,  $V_{OUT}=5V$ ,  $I_{OUT}=0A$ )



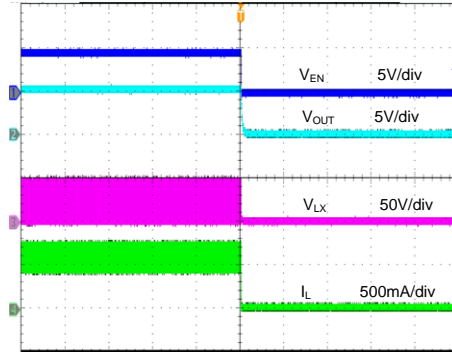
Time (400ms/div)

Startup from EN  
( $V_{IN}=48V$ ,  $V_{OUT}=5V$ ,  $I_{OUT}=0.6A$ )



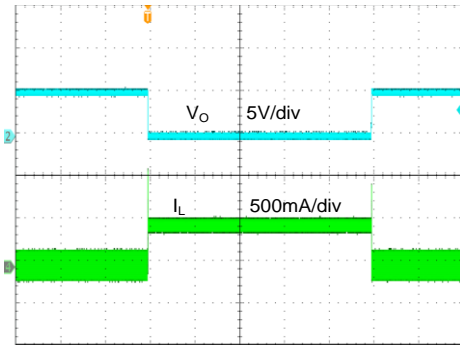
Time (4ms/div)

Shutdown from EN  
( $V_{IN}=48V$ ,  $V_{OUT}=5V$ ,  $I_{OUT}=0.6A$ )



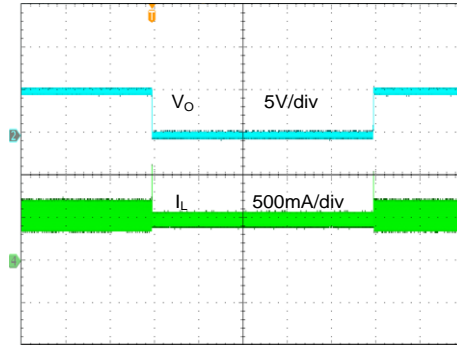
Time (4ms/div)

Short Circuit Protection  
( $V_{IN}=48V$ ,  $V_{OUT}=5V$ ,  $I_O=0A$ ~Short)



Time (10ms/div)

Short Circuit Protection  
( $V_{IN}=48V$ ,  $V_{OUT}=5V$ ,  $I_O=0.6A$ ~Short)



Time (10ms/div)

## Detailed Description

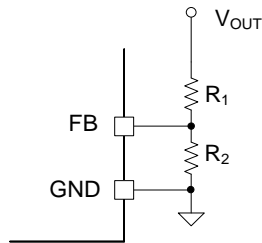
Because of the high integration in the SY89000, the application circuit based on this regulator is rather simple. Only the on-timer resistor  $R_{ON}$ , the feedback resistors ( $R_1$  and  $R_2$ ), the input capacitor  $C_{IN}$ , the output capacitor  $C_{OUT}$  and the output inductor  $L$  need to be selected for the targeted applications specifications.

### Output Voltage Program

Choose  $R_1$  and  $R_2$  to program the proper output voltage. To minimize the power consumption under light loads, it is desirable to choose large resistance values for both  $R_1$  and  $R_2$ .

$$V_{OUT} = \left(1 + \frac{R_1}{R_2}\right) \times V_{FB}$$

$V_{FB}$  is typical 1.225V.



### Output Inductor L

There are several considerations in choosing this inductor.

1) Choose the inductance to provide the desired ripple current. It is suggested to choose the ripple current to be about 40% of the maximum output current. The inductance is calculated as:

$$L_1 = \frac{V_{OUT} \times (1 - V_{OUT} / V_{IN\_MAX})}{f_s \times I_{OUT\_MAX} \times 40\%}$$

Where  $f_s$  is the switching frequency and  $I_{OUT\_MAX}$  is the maximum load current.

The SY89000 regulator is quite tolerant of different ripple current amplitude. Consequently, the final choice of inductance can be slightly off the calculation value without significantly impacting the performance.

2) The saturation current rating of the inductor must be selected greater than the peak inductor current under full load conditions.

$$I_{SAT\_MIN} > I_{OUT\_MAX} + \frac{V_{OUT} \times (1 - V_{OUT} / V_{IN\_MAX})}{2f_s \times L_1}$$

3) The DCR of the inductor and the core loss at the switching frequency must be low enough to achieve the desired efficiency requirement. It is desirable to choose an inductor with smaller DCR to achieve a good overall efficiency.

### Input Capacitor $C_{IN}$

The ripple current through the input capacitor is calculated as:

$$I_{CIN\_RMS} = I_{OUT\_MAX} \times \sqrt{D(1-D)}$$

The capacitance of the input capacitor is calculated as:

$$C_{IN} = \frac{I_{OUT} \times V_{OUT} \times (V_{IN} - V_{OUT})}{\Delta V_{IN} \times f_s \times \text{Eff} \times V_{IN}^2}$$

$\Delta V_{IN}$  is desired input voltage ripple.

To minimize the potential noise problem, place a typical X5R or better grade ceramic capacitor really close to the IN and the GND pins. Care should be taken to minimize the loop area formed by  $C_{IN}$  and the IN/GND pins. In this case, a 1 $\mu$ F low ESR ceramic capacitor is recommended.

### Output Capacitor $C_{OUT}$

The output capacitor is selected to handle the output ripple noise requirements. Both steady state ripple and transient requirements must be taken into consideration when selecting this capacitor. It is recommended to use an X5R or better grade ceramic capacitor greater than 10 $\mu$ F capacitance.

### On-time

The on-time for the SY89000 is determined by the  $R_{ON}$  resistor, and is inversely proportional to the input voltage, resulting in a nearly constant frequency as  $V_{IN}$  is varied over its range.

Frequency vs.  $R_{ON}$  Resistor:

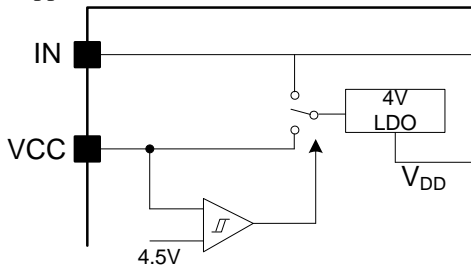
$$f_s \text{ (kHz)} = \frac{11 \times V_o \text{ (V)} + 500}{R_{ON} \text{ (M}\Omega\text{)}}$$

Notice: Final switch frequency is not only affected by component tolerant but also minimum off and on time limit.

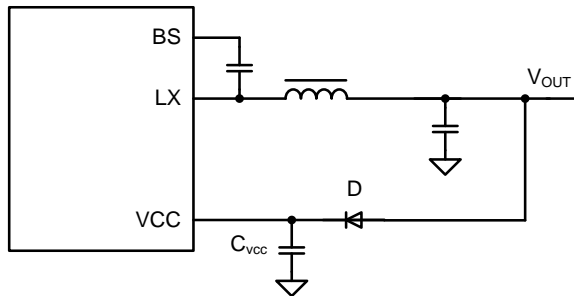
### Internal LDO Regulator

The SY89000 has two power supply ways for 4V LDO. Upon power up, the 4V LDO regulator is power supplied by  $V_{IN}$ . When the voltage on the VDD reaches the under-voltage lockout threshold voltage, the Buck regulator is enabled. After soft start

done, if the VCC pin voltage is larger than 4.5V, the power supply of 4V LDO is switched to VCC. A 0.1μF ceramic capacitor is recommended for C<sub>VCC</sub> at most applications.



In applications, the input pin (IN) can be connected directly to the line voltages up to 100 Volts, where power dissipation in the 4V LDO regulator is a concern; an auxiliary voltage can be connected to the VCC pin via a diode. Setting the auxiliary voltage to 4.8 -28V will shut off the LDO power supply from IN and reduce internal LDO power dissipation.



### Soft-start

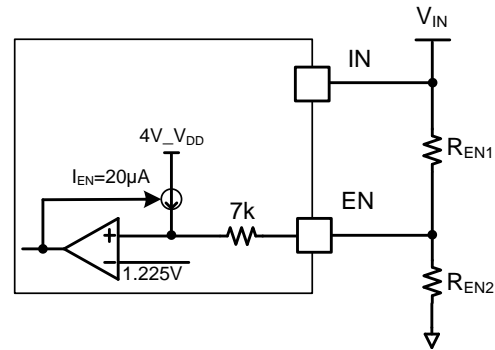
The SY89000 has a built-in soft-start to control the rise rate of the output voltage and limit the input current surge during the IC start-up. The typical soft-start time is 2ms.

### Adjusting Under Voltage Lockout

The EN pin provides electrical on/off control of the device. Once the EN pin voltage exceeds the threshold voltage, the device starts operation. If the EN pin voltage is pulled below the threshold, the regulator stops switching and enters shutdown state. An external set-point voltage divider from V<sub>IN</sub> to GND can be used for setting the minimum operating voltage of the regulator. Minimum V<sub>UVLO</sub> value needs larger than 6.8V.

$$V_{IN,UVLO}(V) = \left(1 + \frac{R_{EN1}}{R_{EN2}}\right) \times V_{EN}$$

V<sub>EN</sub> is typical 1.225V.

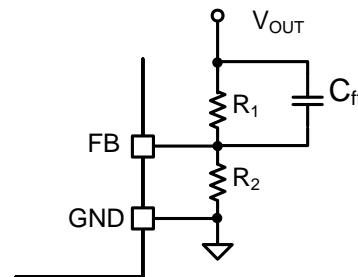


UVLO hysteresis is accomplished with an internal 20μA current source that is switched on or off into the impedance of the set-point divider. When the EN threshold is exceeded, the current source is activated to quickly raise the voltage at the EN pin. The UVLO hysteresis is calculated as

$$V_{HYS}(V) = I_{EN} \times R_{EN1} + I_{EN} \times 7k \times \left(1 + \frac{R_{EN1}}{R_{EN2}}\right)$$

### Load Transient Considerations

The SY89000 regulator adopts the instant PWM architecture to achieve good stability and fast transient responses. Adding a C<sub>ff</sub> ceramic capacitor in parallel with R<sub>1</sub> is recommended.



### External Boot-strap Capacitor

This capacitor provides the gate driver voltage for internal high side MOSFET. A 100nF low ESR ceramic capacitor connected between the BS pin and the LX pin is recommended.

### Over Current Protection

The SY89000 provides cycle-by-cycle over current limit on both high side MOSFET and low-side MOSFET. Under over current condition, if the output voltage drops below 33% of set-point, the device will fold back valley current limit to 0.5×typical value.

### Over-temperature Protection (OTP)

The device includes over-temperature protection (OTP) circuitry to prevent overheating due to excessive power dissipation. This will shut down switching operation when the junction temperature exceeds 150°C. Once the junction temperature cools down by approximately 15°C, the IC will resume normal operation after a complete soft-start cycle. For continuous operation, provide adequate cooling so that the junction temperature does not exceed the OTP threshold.

### Layout Design

The layout design of the SY89000 is very important for proper operation. Following are the tips for good PCB layout.

1) It is desirable to maximize the PCB copper area connecting to the GND pin to achieve the best thermal and noise performance. If the board space allowed, a ground plane is highly desirable.

2)  $C_{IN}$  must be close to the pins IN and GND. The loop area formed by  $C_{IN}$  and GND must be

minimized.

3)  $C_{VCC}$  should be placed close to the VCC pin and the GND pin.

4) The PCB copper area associated with the LX pin must be minimized to avoid the potential noise problem.

5) The feedback components  $R_1$  and  $R_2$  and the trace connecting to the FB pin must NOT be adjacent to the LX net on the PCB layout to avoid the noise problem.

6) If the system chip interfacing with the EN pin has a high impedance state at shutdown mode and the IN pin is connected directly to a power source such as a Li-Ion battery, it is desirable to add a pull-down 1MΩ resistor between the EN and the GND pins to prevent the noise from falsely turning on the regulator at shutdown mode.

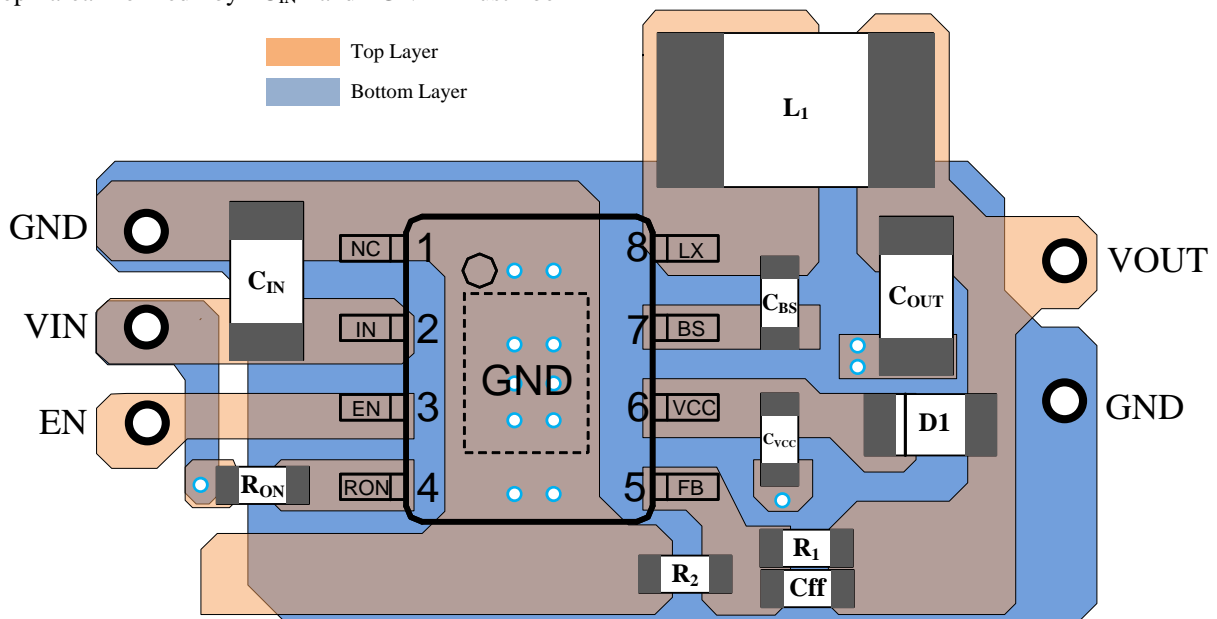
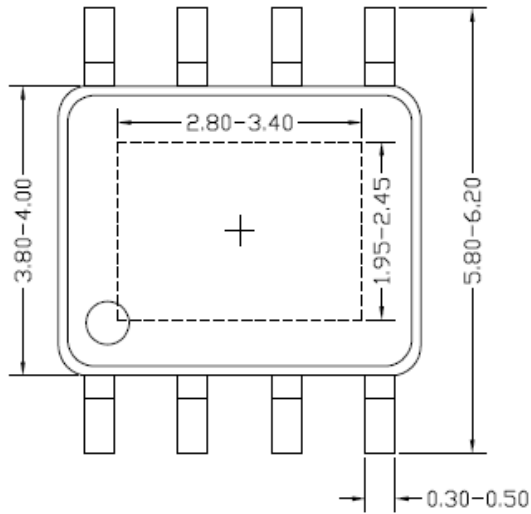
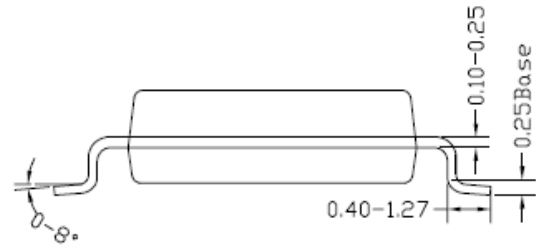


Figure4. PCB Layout Suggestion

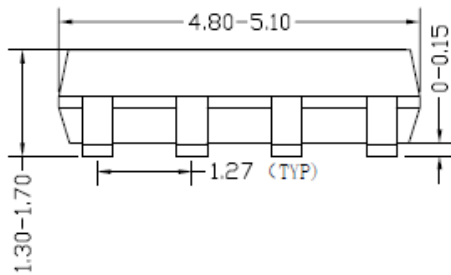
**SO8E Package Outline & PCB Layout**



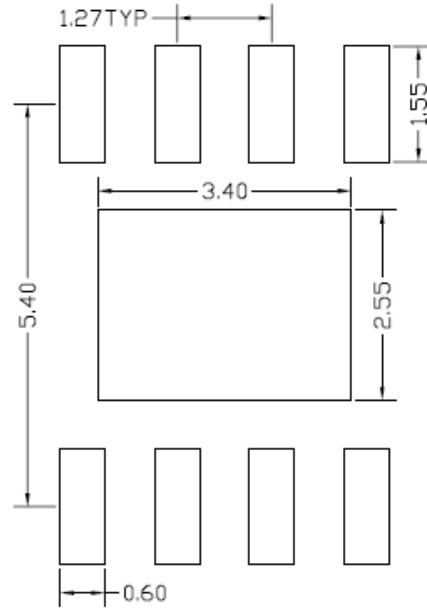
**Top view**



**Side view**



**Front view**



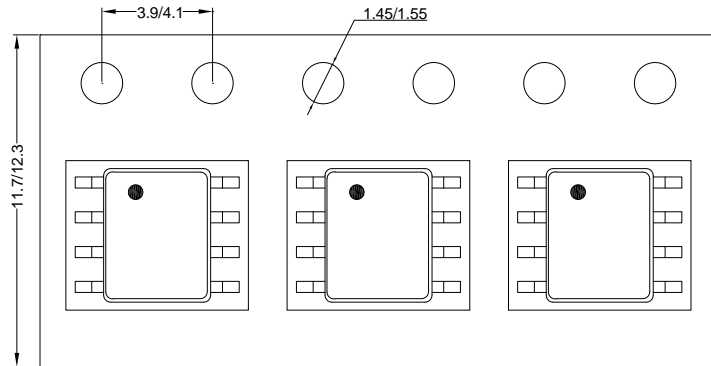
**Recommended PCB layout  
(Reference Only)**

**Notes: All dimension in millimeter and exclude mold flash & metal burr.**

## Taping & Reel Specification

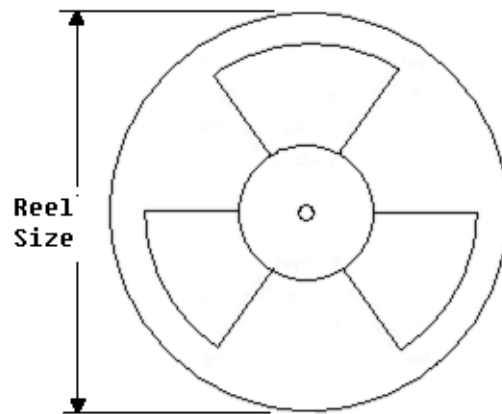
### 1. Taping orientation

SO8E



Feeding direction →

### 2. Carrier Tape & Reel specification for packages



Package type	Tape width (mm)	Pocket pitch(mm)	Reel size (Inch)	Trailer length(mm)	Leader length (mm)	Qty per reel
SO8E	12	8	13"	400	400	2500

### 3. Others: NA



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