SY7065/SY7065A

1.8V Minimum Input and 5. 5V Maximum Output 5A Peak Current Synchronous Boost with Output Disconnect

General Description

The SY7065/SY7065A is a high efficiency synchronous Boost regulator that converts down to 1.8V input and up to 5.5V output voltage. It adopts NMOS for the main switch and PMOS for the synchronous switch. It can disconnect the output from input during the shutdown mode.

Ordering Information

SY7065 □(□□)□

Temperature Code
Package Code
Optional Spec Code

Ordering Number	Package type	Note
SY7065QMC	QFN2×2-10	----
SY7065AQMC	QFN2×2-10	----

Features

- 1.8V Minimum Input Voltage
- Adjustable Output Voltage from 2.5V to 5.5V
- 5A Peak Current Limit
- Input Under Voltage Lockout
- Load Disconnect during Shutdown
- Output Over Voltage Protection
- Input Battery Voltage Monitor
- Automatic Output Discharge at Shutdown:
  - o SY7065: Auto Output Discharge Function
  - o SY7065A: No Output Discharge Function
- Low $R_{DS(ON)}$ (Main Switch/Synchronous Switch) at 5.0V Output: 20/40mΩ
- Compact Package: QFN2×2-10

Applications

- All Single-cell Li or Dual-cell Battery Operated Products as MP-3 Player, PDAs, and Other Portable Equipment

Typical Applications

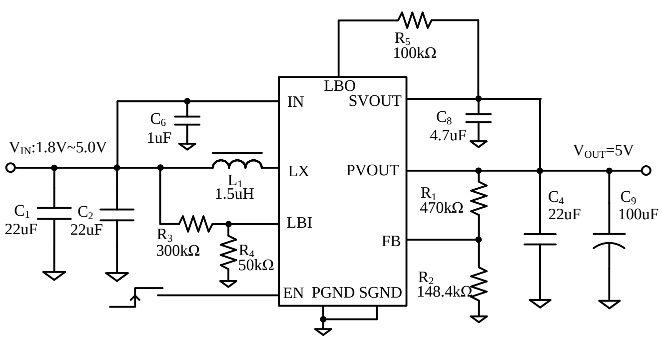


Figure 1. Schematic Diagram

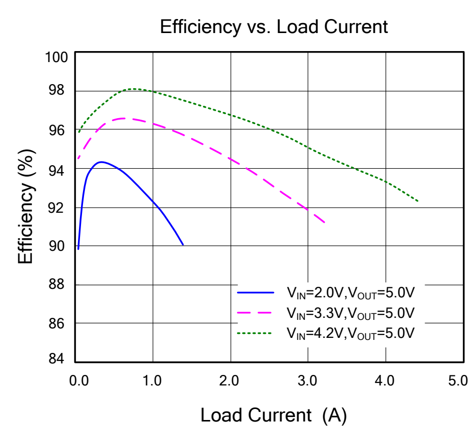
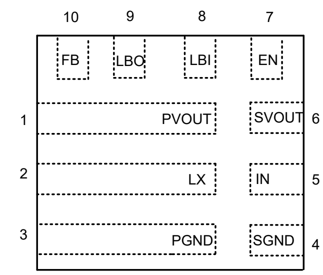


Figure 2. Efficiency Figure

Pinout (top view)



(QFN2×2-10)

Top mark: **RC*xyz* *for SY7065*** (Device code: RC, ***x=year code, y=week code, z= lot number code***)
VL*xyz for SY7065A* (Device code: VL, ***x=year code, y=week code, z=lot number code***)

Pin Name	Pin Number	Description
PVOUT	1	Power output pin. Decouple this pin to the GND pin with at least a 22μF ceramic capacitor.
LX	2	Inductor node. Connect an inductor between the IN pin and the LX pin.
PGND	3	Power ground pin.
SGND	4	Signal ground pin.
IN	5	Signal input pin.
SVOUT	6	Signal output pin. Decouple this pin to the GND pin with at least a 4.7μF ceramic capacitor for noise immunity consideration.
EN	7	Enable pin. Internal integrated with a 1MΩ pull-down resistor.
LBI	8	Low battery comparator input.
LBO	9	Low battery comparator output (open-drain) .
FB	10	Feedback pin. Connect a resistor R_1 between OUT and FB, and a resistor R_2 between FB and GND to program the output voltage. $V_{OUT}=1.2V\times(R_1/R_2+1)$.

Block Diagram

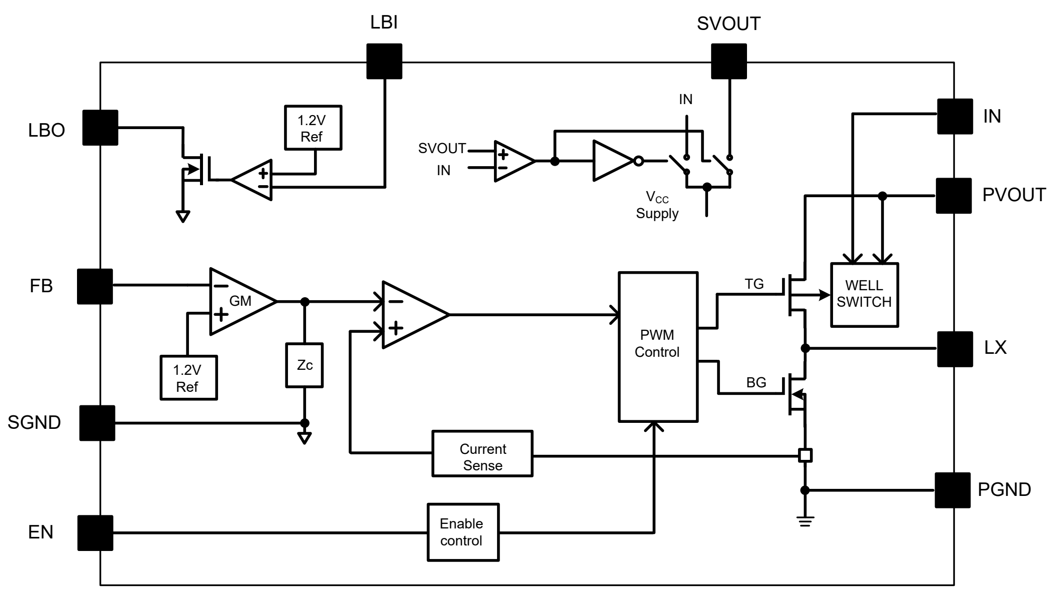


Figure3. Block Diagram

Absolute Maximum Ratings (Note 1)

EN-- V_{OUT}+0.3V
Other Pins-- 6V
Power Dissipation, P_D@ T_A=25°C QFN2×2-10-- 2.5W
Package Thermal Resistance (Note 2)
θ_{JA} -- 50°C/W
θ_{JC} -- 10°C/W
Junction Temperature Range -- 150°C
Lead Temperature (Soldering, 10 sec.) -- 260°C
Storage Temperature Range -- -65°C to 150°C

Recommended Operating Conditions (Note 3)

IN --- 1.8V to 5.25V
PVOUT, SVOUT--- 2.5V to 5.5V
EN -- 0V to V_{OUT}+0.3V
All other pins --- 0-5.5V
Junction Temperature Range -- -40°C to 125°C
Ambient Temperature Range --- -40°C to 85°C

Electrical Characteristics

(V_{IN} =2.4V, V_{OUT}=5V, I_{OUT}=500mA, T_A = 25°C unless otherwise specified)

Parameter		Symbol	Test Conditions	Min	Typ	Max	Unit
Input Voltage		V_{IN}		1.8		5.25	V
Output Voltage Range		V_{OUT}		2.5		5.5	V
Quiescent Current	V_{IN}	I_Q	Io=0A,V_{EN}=V_{IN}=1.8V, V_{OUT}=5.0V		10		µA
	V_{OUT}				27		µA
Shutdown Current		I_{SHDN}	V_{EN}=0V, V_{IN}=2.4V		0.1	1	µA
Linear Charge Current		I_{CHARGE}	V_{OUT}≤1V		1.2		A
			1V<V_{OUT}<90%V_{IN}		1.0		
Soft-start Time		t_{SS}			1		ms
Input V_{IN} UVLO Threshold		V_{UVLO}				1.78	V
V_{IN} UVLO Hysteresis		V_{HYS}			0.1		V
EN Rising Threshold		V_{ENH}		1.2			V
EN Falling Threshold		V_{ENL}				0.4	V
LBI Voltage Threshold		V_{LBI}		1.176	1.2	1.224	V
LBI Input Hysteresis		V_{LBI_HYS}			20		mV
Low Side Main FET R_{ON}		$R_{DS(ON)1}$	V_{OUT}=5.0V		20		mΩ
Synchronous FET R_{ON}		$R_{DS(ON)2}$	V_{OUT}=5.0V		40		mΩ
Main FET Current Limit		I_{LIM1}		5.0			A
Switching Frequency		fsw			500		kHz
Feedback Reference Voltage		V_{REF}		1.182	1.2	1.218	V
Output Over Voltage Protection		V_{OVP}			6		V
Minimum ON Time		t_{ON_MIN}			100		ns
Minimum OFF Time		t_{OFF_MIN}			100		ns
Max ON Time		t_{ON_MAX}			2		µs
Thermal Shutdown Temperature		T_{SD}			150		℃
Thermal Shutdown Hysteresis		T_{HYS}			20		℃
Output Discharge Resistor		R_{DSC}			80		Ω

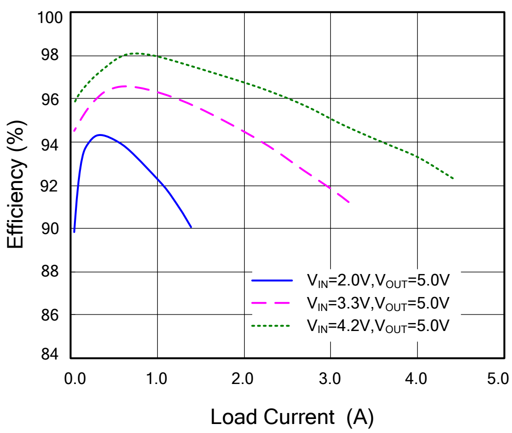
Note 1: Stresses beyond the “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Note 2: θ_{JA} is measured in the natural convection at T_A = 25°C on a four-layer Silergy evaluation board.

Note 3: The device is not guaranteed to function outside its operating conditions.

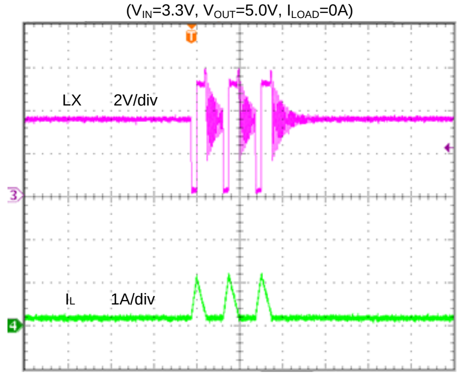
Typical Performance Characteristics (for SY7065)

Efficiency vs. Load Current



Steady State

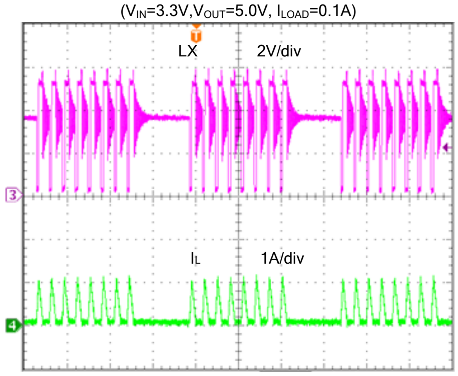
(V_{IN}=3.3V, V_{OUT}=5.0V, I_{LOAD}=0A)



Time (4µs/div)

Steady State

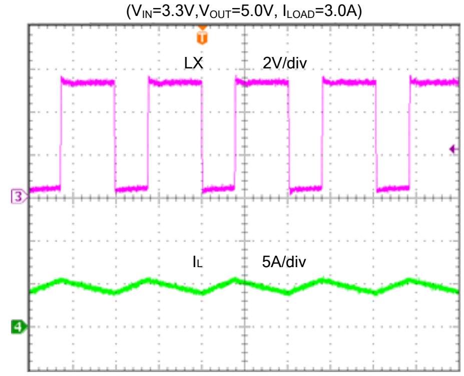
(V_{IN}=3.3V,V_{OUT}=5.0V, I_{LOAD}=0.1A)



Time (10µs/div)

Steady State

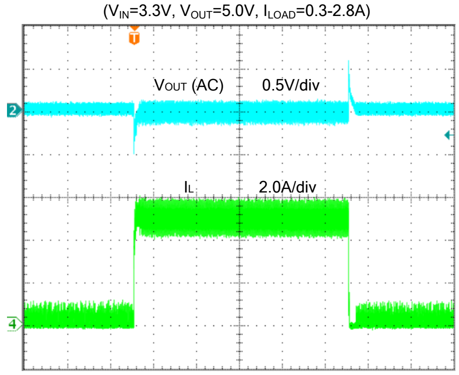
(V_{IN}=3.3V,V_{OUT}=5.0V, I_{LOAD}=3.0A)



Time (1µs/div)

Load Transient

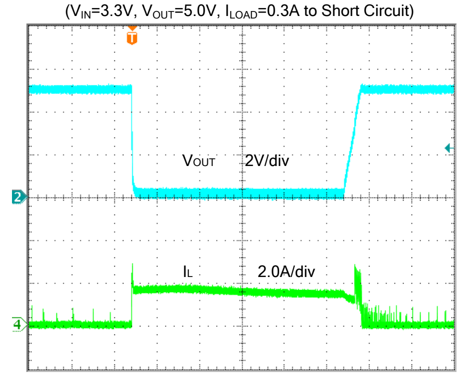
(V_{IN}=3.3V, V_{OUT}=5.0V, I_{LOAD}=0.3-2.8A)



Time (1ms/div)

Short Circuit

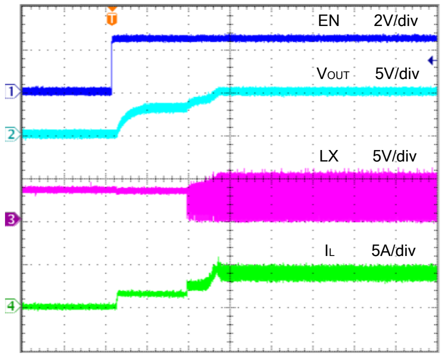
(V_{IN}=3.3V, V_{OUT}=5.0V, I_{LOAD}=0.3A to Short Circuit)



Time (1ms/div)

Startup from Enable

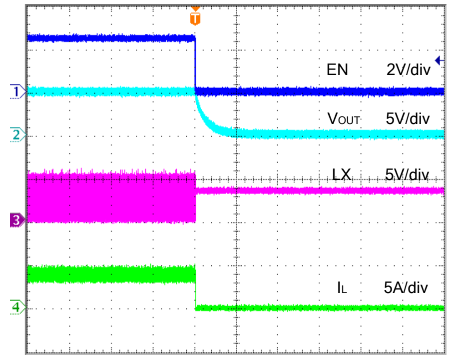
(V_{IN}=3.3V, V_{OUT}=5.0V, I_{LOAD}=2.4A)



Time (1ms/div)

Shutdown from Enable

(V_{IN}=3.3V, V_{OUT}=5.0V, I_{LOAD}=2.4A)



Time (1ms/div)

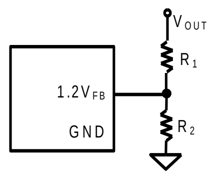
Applications Information

Because of the high integration for the SY7065/A, only the input capacitor C_{IN}, the output capacitor C_{OUT}, the inductor L and the feedback resistors (R_1 and R_2) need to be selected for the targeted applications specifications.

Feedback Resistor Dividers R_1 and R_2:

Choose R_1 and R_2 to program the proper output voltage. To minimize the power consumption under light loads, it is desirable to choose large resistance values for both R_1 and R_2. A value of between 10kΩ and 1MΩ is recommended for both resistors. If V_{OUT} is 5.0V, R_1=470kΩ is chosen, using the following equation, then R_2 can be calculated to be 148.4kΩ:

$$R_2 = \frac{1.2V}{V_{OUT} - 1.2V} R_1 \qquad (1)$$



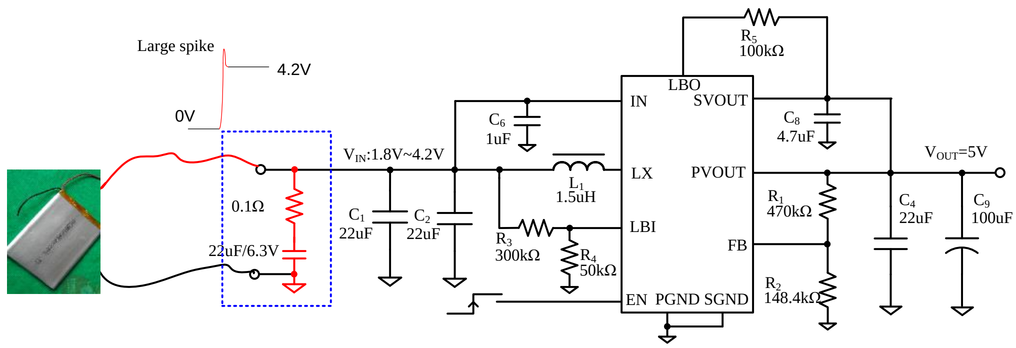
Input Capacitor C_{IN}:

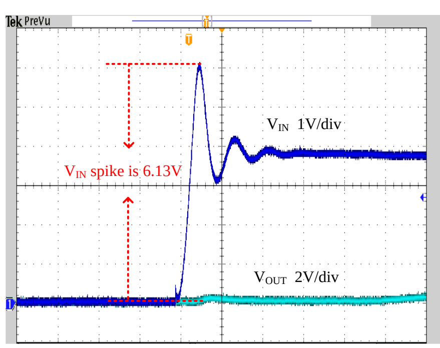
The input capacitor is selected to handle the input ripple current requirements. For the best performance, it is recommended to use an X5R or better grade ceramic capacitor with 6.3V rating and greater than 22µF capacitance.

Li-Ion Battery Hot Plug Consideration:

In the mass production stage, the Li-ion battery will always hot plug in between the IN and the GND pin. The hot plug may lead to large voltage spike and even lead to the IC EOS fail. To avoid this potential risk, a 22µF ceramic capacitor serial with a 0.1Ω resister is recommended to absorb the input voltage spike.

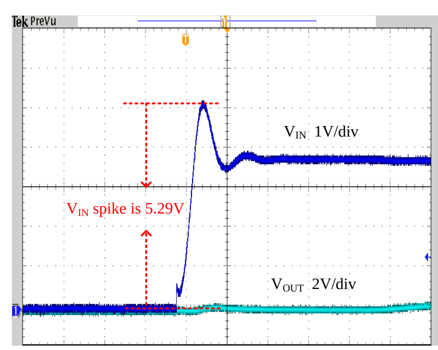
With the recommended input absorb solution, the voltage spike can be reduced from 6.13V to 5.29V.





Time (10us/div)

C_{IN}=22uF/6.3V*2



Time (10us/div)

C_{IN}=22uF/6.3V*2 // (22uF+0.1Ω)

Inductor L Selection:

There are several considerations in choosing this inductor.

1) Choose the inductance to provide the desired ripple current. It is suggested to choose the ripple current to be about 40% of the maximum output current. The inductance is calculated as:

$$L=\left(\frac{V_{IN}}{V_{OUT}}\right)^2\frac{(V_{OUT}-V_{IN})}{f_{SW}\times I_{OUT,MAX}\times 40\%} \qquad (2)$$

Where f_{SW} is the switching frequency and $I_{OUT,MAX}$ is the maximum load current.

The SY7065/A is quite tolerant of different ripple current amplitude. Consequently, the final choice of inductance can be slightly off the calculation value without significantly impacting the performance.

2) The saturation current rating of the inductor must be selected to be greater than the peak inductor current under full load conditions.

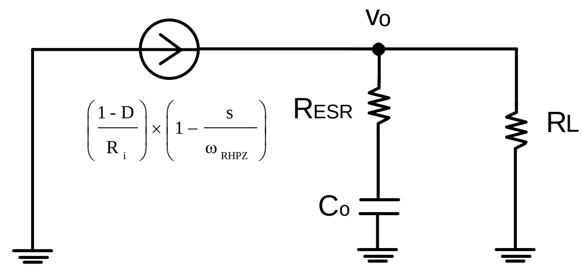
$$I_{SAT,MIN}>\left(\frac{V_{OUT}}{V_{IN}}\right)\times I_{OUT,MAX}+\frac{V_{IN}}{V_{OUT}}\frac{(V_{OUT}-V_{IN})}{2\times f_{SW}\times L} \qquad (3)$$

3) The DCR of the inductor and the core loss at the switching frequency must be low enough to achieve the desired efficiency requirement. It is desirable to choose an inductor with DCR<50mΩ to achieve a good overall efficiency.

Inductor vs. Output Capacitor:

The output capacitor is selected to handle the output ripple noise requirements. Both steady state ripple and transient requirements must be taken into consideration when selecting this capacitor. Care should be taken to minimize the loop area formed by C_{OUT}, and the OUT/GND pins. It's recommended to use an X5R or better grade ceramic capacitor with 10V rating and great than 22μF capacitance to decouple the high frequency current. And also a tantalum capacitor with 16V rating and great than 100μF capacitance is recommended for the stability consideration.

All continuous mode Boost converters have a right half plane zero (RHPZ) due to the inductor being removed from the output during charging. In a converter with current mode control, inner current feedback loop allows the switch, inductor and modulator to be lumped together into a small signal variable current source, shown as follows.



the power stage approximate transfer function is:

$$G_c(s)=\frac{(1-D)\times R_L}{R_i}\times\frac{\left(1+\frac{s}{\omega_{ESR}}\right)\left(1-\frac{s}{\omega_{RHPZ}}\right)}{1+\frac{s}{\omega_p}} \qquad (4)$$

Where

$$\omega_{ESR}=\frac{1}{R_{ESR}C_O} \qquad (5)$$

$$\omega_P=\frac{1}{(R_{ESR}+R_L)\times C_O} \qquad (6)$$

$$\omega_{RHPZ}=\frac{R_L}{L}\times\left(\frac{V_{IN}}{V_{OUT}}\right)^2 \qquad (7)$$

As the equation 4 shows, Boost convert with current mode control transfer function is consist of one ESR zero, one right half plane zero and one pole. Right half plane zero brings 20dB/decade gain increase, 90 degrees phase drop. So the bandwidth of the Boost converter MUST be lower than f_{RHPZ}.

As shown in equation 7, right half plane zero is depending on R_L, L and duty cycle. Larger inductor lead to lower f_{RHPZ}, so bandwidth should be designed lower than f_{RHPZ}.

Some low profile application may prefer to use the ceramic capacitor solution and some low cost application may use the Electrolytic capacitor to reduce the BOM cost.

Below is selection table based on the different inductance and the output capacitor

Inductance vs. Output Capacitor Selection Table

Inductance		Low profile capacitor application		Low cost capacitor application
Part Number	L(μH)	Part Number	C_{OUT} (μF)	C_{OUT} (μF)
SPM6530T-1R0M	1.0	C3216X5R1A226M	22μF/10V×3pcs	22μF/10V+100uF(E-cap)
SPM6530T-1R5M	1.5	C3216X5R1A226M	22μF/10V×4pcs	22μF/10V+100uF(E-cap)
SPM6530T-2R2M	2.2	C3216X5R1A226M	22μF/10V×5pcs	22μF/10V+200uF(E-cap)

Enable Operation

Pulling the EN pin low (<0.4V) will shut down the device. During shutdown mode, the SY7065/A shutdown current drops to lower than 1μA, driving the EN pin high (> 1.2V) will turn on the IC again.

Low Battery Detector Function-LBI/LBO

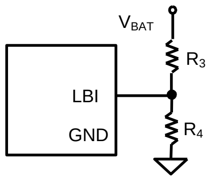
The low-battery detector function is used for monitoring the battery voltage and generating an error flag when the battery voltage drops below a user-set threshold voltage.

The function is active only when the device is enabled. When the device is disabled, LBO stays at high impedance. The detection threshold is 1.2V at LBI. During the normal operation, LBO stays at high impedance when the voltage applied at LBI is above the threshold. It is active low when the voltage at LBI goes below 1.2V.

The battery voltage, at which the detection circuit switches, can be programmed with a resistive divider connected to the LBI pin. The resistive divider scales down the battery voltage to a voltage level of 1.2V, which is then compared to LBI threshold voltage. The LBI pin has a built-in hysteresis of 20mV. If the low-battery detection circuit is not used, the LBI pin should be connected to GND (or to VBAT) and the LBO pin can be left unconnected. Do not leave the LBI pin floating.

R_3 and R_4 are designed to program the proper low battery threshold voltage. The voltage across R_4 is equal to the LBI voltage threshold that is generated on-chip, which has a value of 1.2V. The value of resistor R_3, depending on the desired minimum battery voltage V_{BAT}, can be calculated as:

$$R_3 = \frac{V_{BAT} - 1.2V}{1.2V} R_4 \quad (9)$$



The output of the low battery monitor is a simple open-drain output that goes active low if the dedicated battery voltage drops below the programmed threshold voltage on LBI. The output requires a pull up resistor with a recommended value of 100kΩ. The maximum voltage which is used for pulling up the LBO outputs should not exceed the output voltage of the DC/DC converter. If not used, the LBO pin can be left floating or tied to GND.

Layout Design Consideration:

For the best efficiency and minimum noise problems, the following components should be placed close to the IC: C_{IN}, C_{OUT}, L, R_1 and R_2.

1) It is desirable to maximize the PCB copper area connecting to the PGND pin to achieve the best thermal and noise performance. If the board space allowed, a ground plane is highly recommended.

2) C_{OUT} must be close with the pins PVOUT and PGND. The loop area formed by C_{OUT} and GND must be minimized.

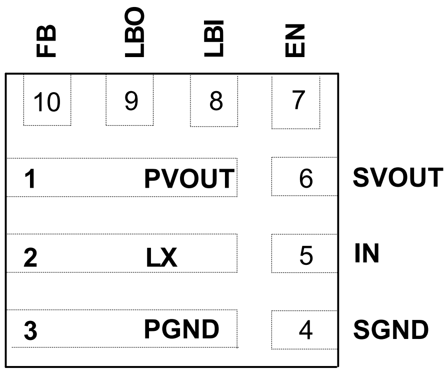
3) To minimize the output decouple loop area, the LX trace is recommended to be routed on bottom or middle layer through via.

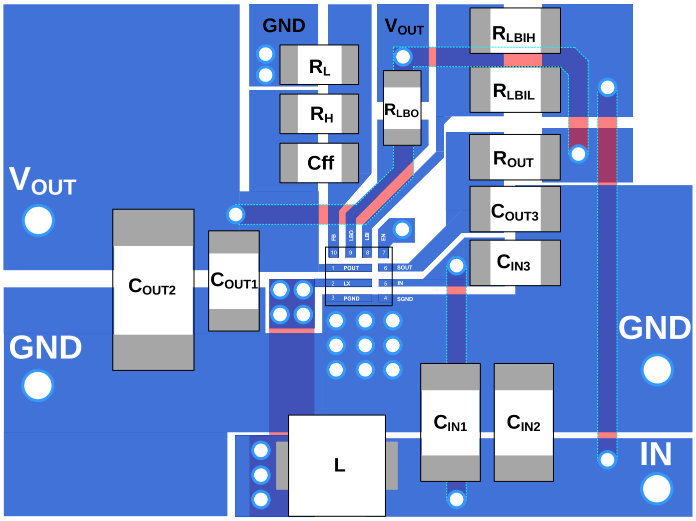
4) The SVOUT is the power supply pin for the internal control circuit. Don't connect to PVOUT pin directly. A 4.7μF ceramic capacitor is strongly recommended to decouple the SVOUT pin to the SGND pin. Please use a jump wire to connect the SVOUT pin to output capacitor side.

5) The PCB copper area associated with the LX pin must be minimized to avoid the potential noise problem.

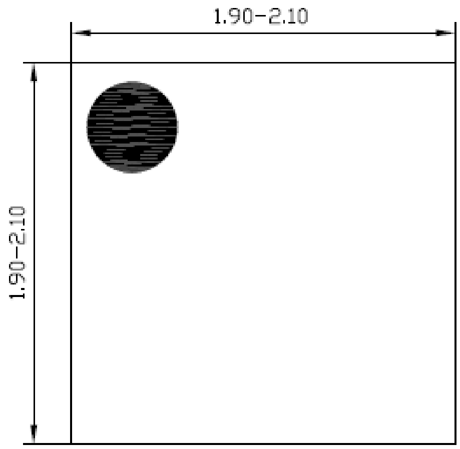
6) The components R_1 and R_2 and the trace connecting to the FB pin must not be adjacent to the LX net on the PCB layout to avoid the noise problem.

PCB Layout Suggestion

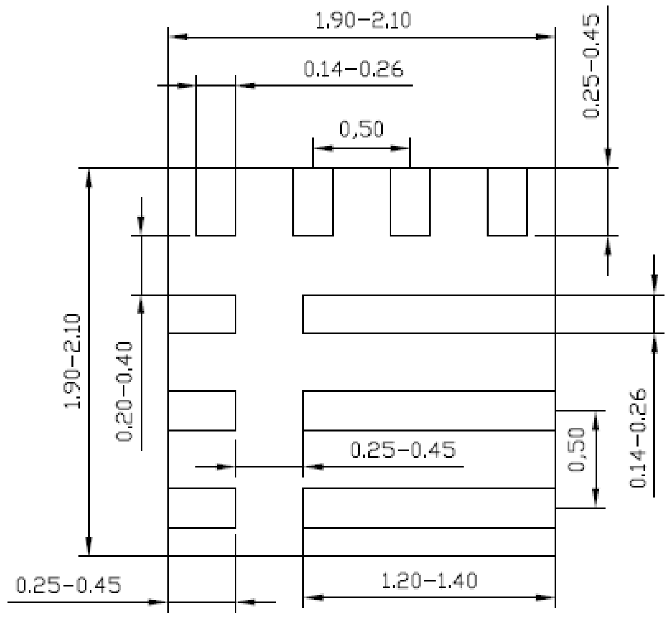




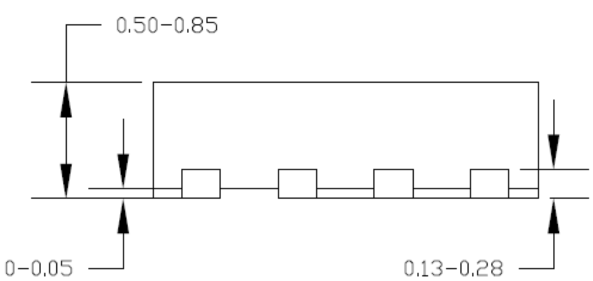
QFN2×2-10 Package Outline



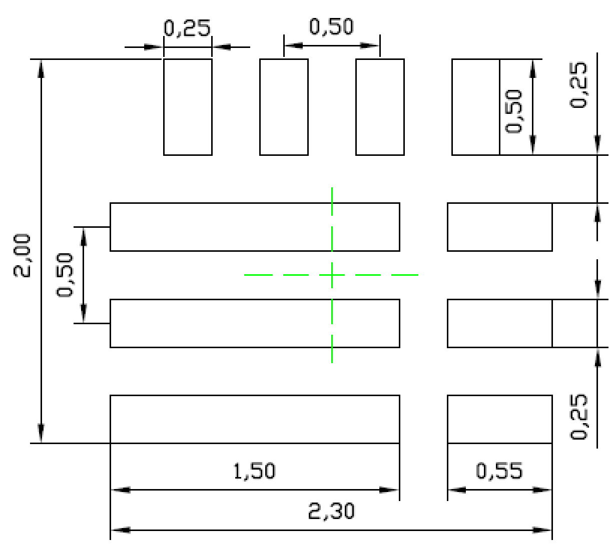
Top View



Bottom View



Side View



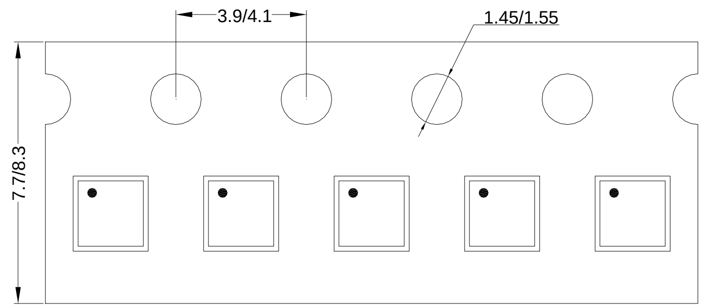
Recommended PCB Layout
(Reference only)

Notes: All dimension in millimeter and exclude mold flash & metal burr

Taping & Reel Specification

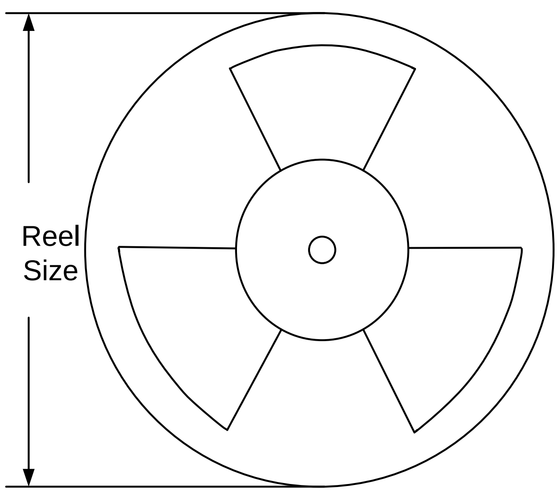
1. Taping orientation

QFN2×2



Feeding direction

2. Carrier Tape & Reel specification for packages



Package types	Tape width (mm)	Pocket pitch(mm)	Reel size (Inch)	Trailer length(mm)	Leader length (mm)	Qty per reel
QFN2×2	8	4	7"	400	160	3000

3. Others: NA

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