SY6307B

500mA Low Dropout Bias Rail LDO Regulator

General Description

SY6307B is a 500mA low dropout bias rail LDO regulator with built-in NMOS. Compact DFN1.2×1.2-6 package is optimized for use in space constrained applications.

Ordering Information

SY6307 □(□□)□
- Temperature Code
- Package Code
- Optional Spec Code

Ordering Number	Package Type	Note
SY6307BSCC	DFN1.2x1.2-6	--

Features

- Input Voltage Range: 0.8V-5.5V
- Bias Voltage Range: 2.4V-5.5V
- Output Voltage Accuracy: +/-1%
- Bias Input Quiescent Current: 110μA
- Up to 500mA Output Current
- Current Limit Protection
- Over Temperature Shutdown
- Output Auto-discharge Resistor: 130Ω
- RoHS Compliant and Halogen Free
- Compact Package: DFN1.2×1.2-6

Applications

- Battery−powered Equipment
- Smart Phones, Tablets
- Cameras, DVRs, STB and Camcorders

Typical Applications

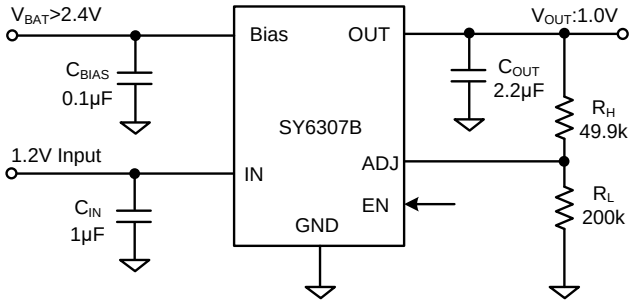


Figure1. Schematic Diagram

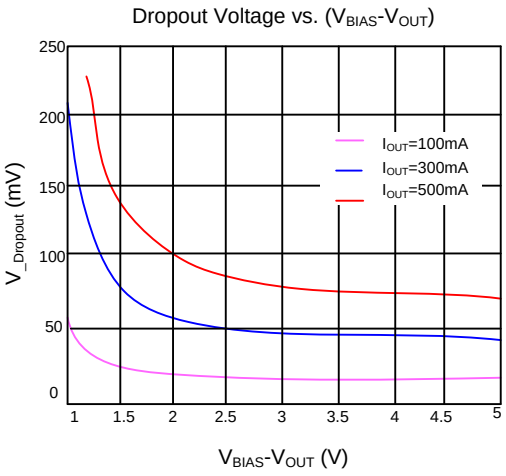
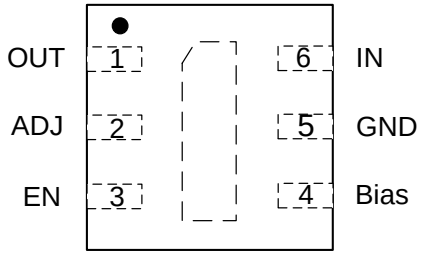


Figure2. Dropout Curve

Pinout (top view)



(DFN1.2x1.2-6)

Top mark: H*xyz* for SY6307BSCC (Device code: H, ***x=year code, y=week code, z= lot number code***)

Pin Number	Symbol	Pin Description
1	OUT	Output pin. Decouple this pin to GND with at least a 2.2μF ceramic capacitor.
2	ADJ	Output voltage programming pin. Connect this pin to the center point of the output resistor divider (as shown in Figure 1) to program the output voltage: V_{OUT}=0.8V× (1+R_H/R_L).
3	EN	Enable control pin. Pull high to enable the regulator. Pull low to shut down the regulator. Do not leave it floating.
4	Bias	Bias voltage supply for internal control circuits. Decouple this pin to GND with at least a 0.1μF ceramic capacitor.
5	GND	Ground pin.
6	IN	Input voltage supply pin. Decouple this pin to GND with at least a 1μF ceramic capacitor.

Block Diagram

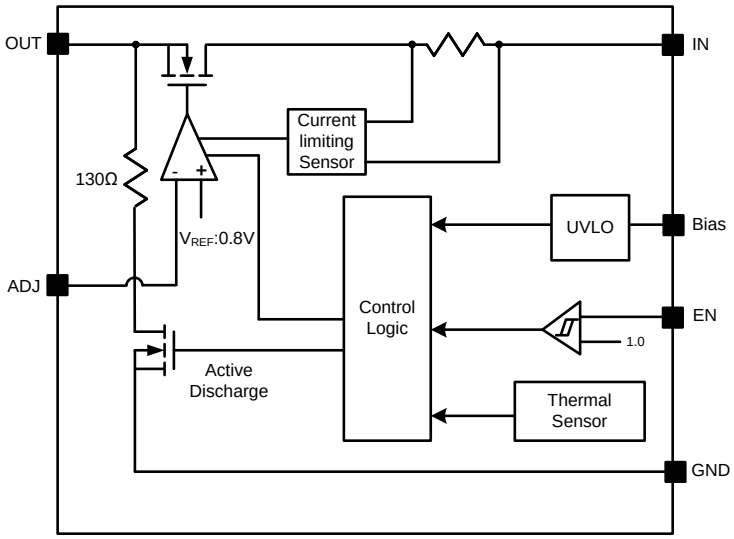


Figure3. Block Diagram

Absolute Maximum Ratings (Note 1)

IN, OUT, Bias, EN, ADJ ---------- -0.3V to 6.0V
Power Dissipation, P_D @ T_A = 25°C, DFN1.2x1.2-6---------- 1.4W
Package Thermal Resistance (Note 2)
θ_{JA} ---------- 70°C/W
θ_{JC} ---------- 12°C/W
Junction Temperature Range ---------- -40°C to 150°C
Lead Temperature (Soldering, 10 sec.) ---------- 260°C
Storage Temperature Range ---------- -65°C to 150°C

Recommended Operating Conditions (Note 3)

Bias Input Voltage ---------- 2.4V to 5.5V
IN ---------- 0.8V to 5.5V
OUT ---------- 0.8V to V_{Bias}-1.4V
Junction Temperature Range ---------- -40°C to 125°C
Ambient Temperature Range ---------- -40°C to 85°C

Electrical Characteristics

(V_{IN} =1.2V, V_{OUT}=1.0V, V_{Bias}=3.3V, I_{OUT}=1mA, C_{IN}=1.0uF, C_{OUT}=2.2μF, T_A = 25°C unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ.	Max	Unit
Input Voltage Range	V_{IN}		$V_{OUT}+V_{DO}$		5.5	V
Bias Input Voltage	V_{Bias}		2.4		5.5	V
Bias Supply Current	I_{Bias}			110		μA
Bias Shutdown Current	I_{SD}	V_{EN}=0		0.1	1	μA
Feedback Reference Voltage	V_{REF}		0.792	0.8	0.808	V
Current Limit	I_{LIM}		500			mA
Load Regulation	V_{LOAD}	I_{OUT}: 1mA~500mA		2		mV
V_{Bias} Line Regulation	$\triangle V_{OUT}/\triangle V_{Bias}$	2.7 V or ($V_{OUT(NOM)}$ + 1.6 V), whichever is greater < V_{Bias} < 5.5 V		0.01		%/V
Dropout Voltage	V_{DO}	I_{OUT}=500mA		90		mV
Ripple Rejection	$PSRR_{(VIN)}$	V_{IN} to V_{OUT}, f = 1 kHz, I_{OUT} = 150mA, $V_{IN} \geq V_{OUT}$ +0.5 V		70		dB
	$PSRR_{(VBias)}$	V_{Bias} to V_{OUT}, f = 1 kHz, I_{OUT} = 150mA, $V_{IN} \geq V_{OUT}$ +0.5 V		70		dB
Output Voltage Temperature Coefficient	$\triangle V_{OUT}/\triangle T$	I_{OUT}=100mA -40°C≤T≤85°C		±100		ppm/°C
Output Noise Voltage	V_N	$V_{IN}=V_{OUT}$+0.5V, V_{OUT}=1V, f=10Hz to 100kHz		40		μV_{RMS}
Discharge resistor	$R_{Discharge}$			130		Ω
EN Rising Threshold	V_{ENH}		1.0			V
EN Falling Threshold	V_{ENL}				0.4	V
Thermal Shutdown Temperature	T_{SD}			150		°C
Thermal Shutdown Hysteresis	T_{HYS}			20		°C

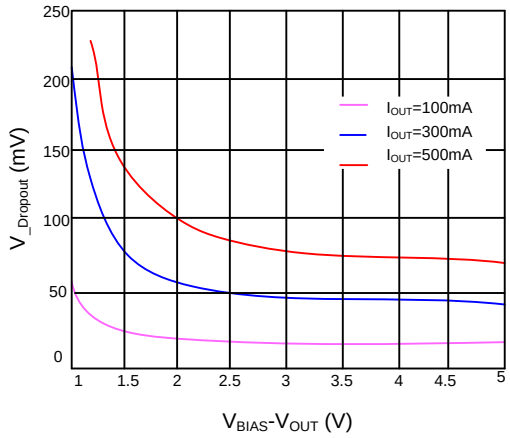
Note 1: Stresses beyond the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: θ_{JA} of SY6307BSCC is measured in the natural convection at T_A = 25°C on a two-layer Silergy evaluation board. θ_{JC} measurement. Paddle of DFN 1.2x1.2-6 package is the case position for SY6307BSCC.

Note 3: The device is not guaranteed to function outside its operating conditions.

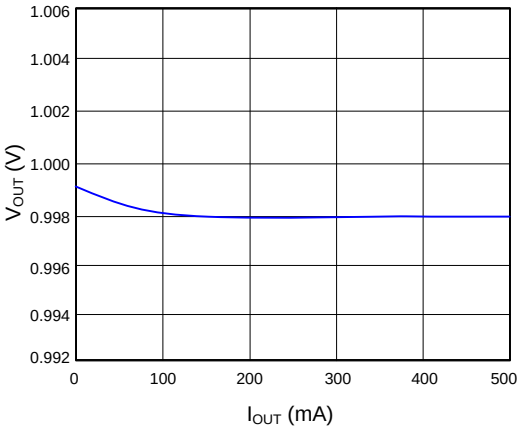
Typical Performance Characteristics

Dropout Voltage vs. (V_{BIAS}-V_{OUT})



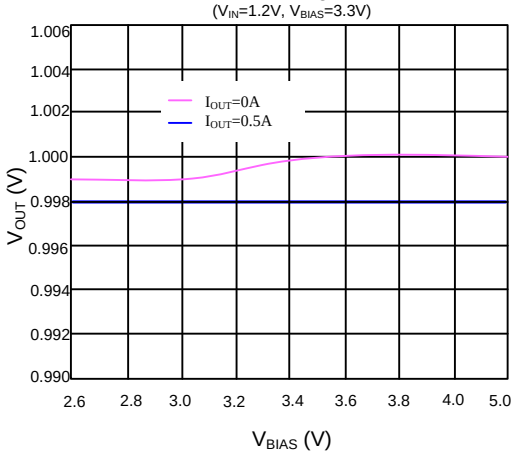
Load Regulation

(V_{IN}=1.2V, V_{BIAS}=3.3V)



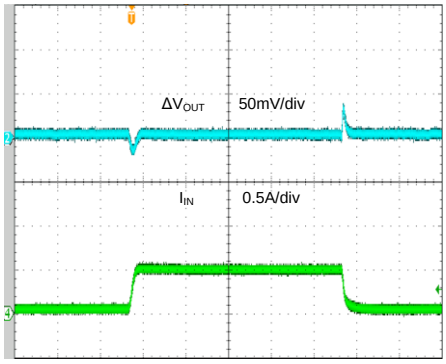
V_{BIAS} Line Regulation

(V_{IN}=1.2V, V_{BIAS}=3.3V)



Load Transient

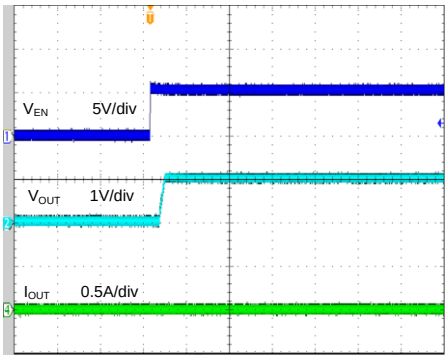
(V_{BIAS}=3.3V, V_{IN}=1.2V, V_{OUT}=1.0V, I_{OUT}= 50mA~ 500mA)



Time (100μs/div)

Startup from Enable

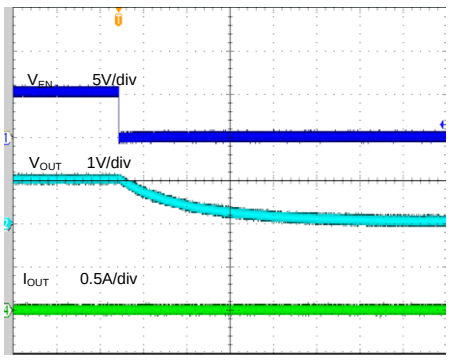
(V_{BIAS}=3.3V, V_{IN}=1.2V, V_{OUT}=1.0V I_{OUT}=0A)



Time (200μs/div)

Shutdown from Enable

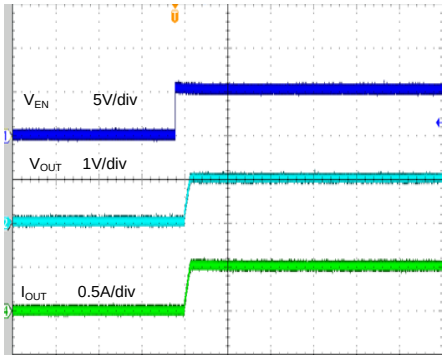
(V_{BIAS}=3.3V, V_{IN}=1.2V, V_{OUT}=1.0V I_{OUT}=0A)



Time (200μs/div)

Startup from Enable

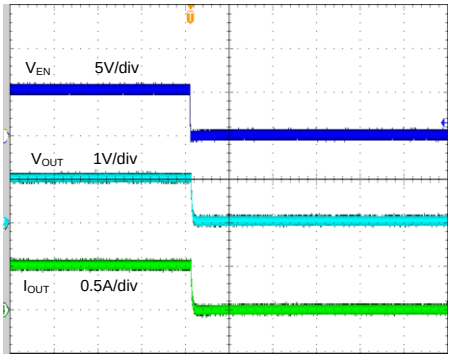
(V_{BIAS}=3.3V, V_{IN}=1.2V, V_{OUT}=1.0V I_{OUT}=500mA)



Time (200μs/div)

Shutdown from Enable

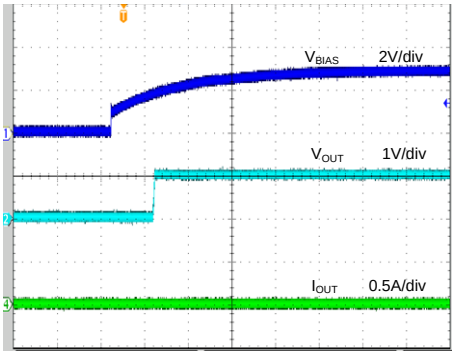
(V_{BIAS}=3.3V, V_{IN}=1.2V, V_{OUT}=1.0V I_{OUT}=500mA)



Time (200μs/div)

Startup from V_{BIAS}

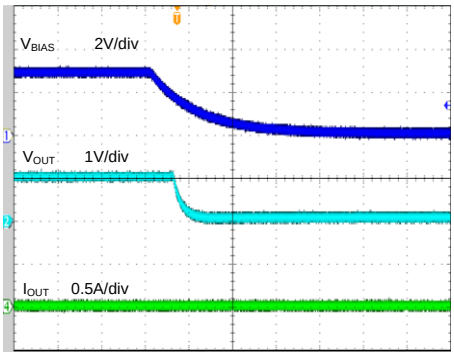
(V_{BIAS}=3.3V, V_{IN}=1.2V, V_{OUT}=1.0V I_{OUT}=0A)



Time (2ms/div)

Shutdown from V_{BIAS}

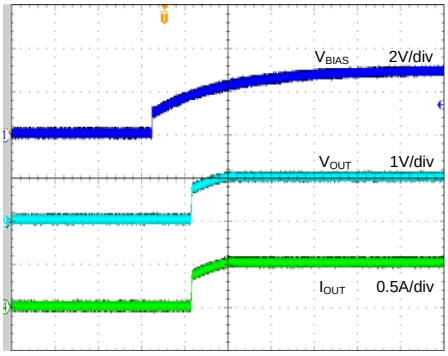
(V_{BIAS}=3.3V, V_{IN}=1.2V, V_{OUT}=1.0V I_{OUT}=0A)



Time (2ms/div)

Startup from V_{BIAS}

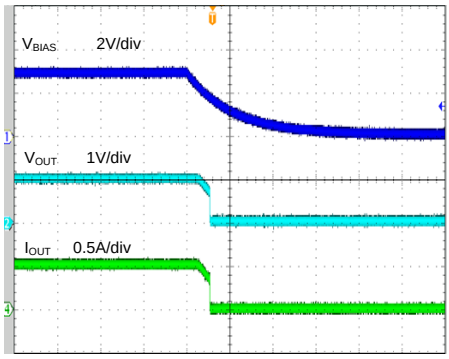
(V_{BIAS}=3.3V, V_{IN}=1.2V, V_{OUT}=1.0V I_{OUT}=500mA)



Time (2ms/div)

Shutdown from V_{BIAS}

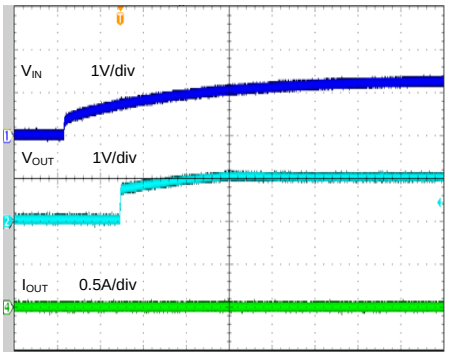
(V_{BIAS}=3.3V, V_{IN}=1.2V, V_{OUT}=1.0V I_{OUT}=500mA)



Time (2ms/div)

Startup from V_{IN}

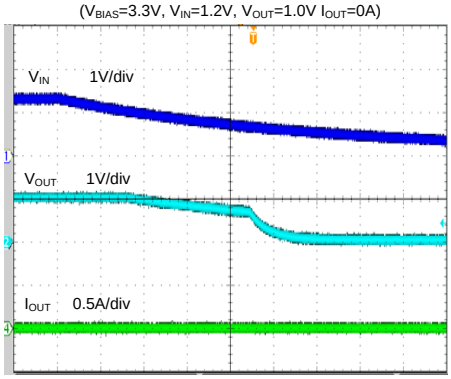
(V_{BIAS}=3.3V, V_{IN}=1.2V, V_{OUT}=1.0V I_{OUT}=0A)



Time (800us/div)

Shutdown from V_{IN}

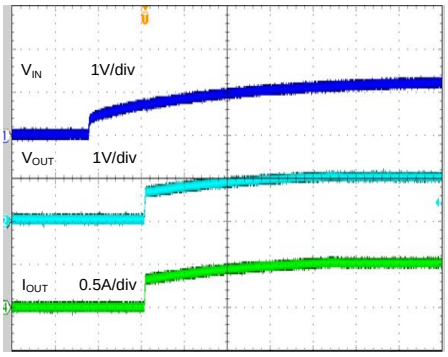
(V_{BIAS}=3.3V, V_{IN}=1.2V, V_{OUT}=1.0V I_{OUT}=0A)



Time (800us/div)

Startup from V_{IN}

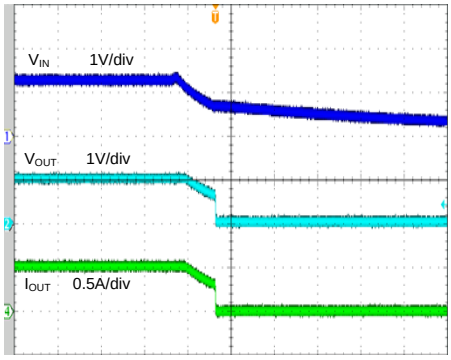
(V_{BIAS}=3.3V, V_{IN}=1.2V, V_{OUT}=1.0V I_{OUT}=500mA)



Time (800us/div)

Shutdown from V_{IN}

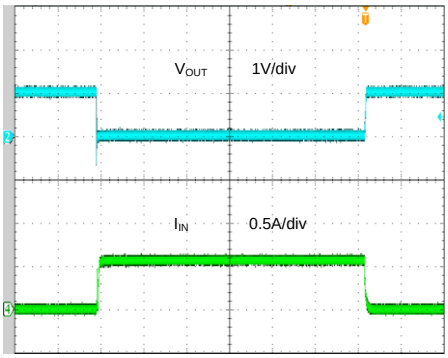
(V_{BIAS}=3.3V, V_{IN}=1.2V, V_{OUT}=1.0V I_{OUT}=500mA)



Time (800us/div)

Hard Short Protection

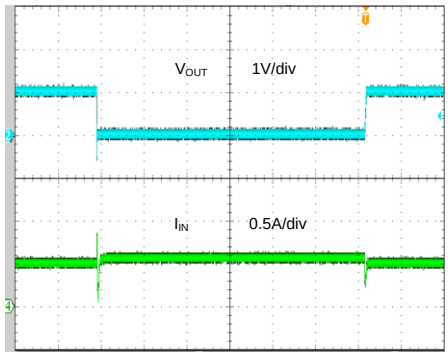
(V_{BIAS}=3.3V, V_{IN}=1.2V, V_{OUT}=1.0V I_{OUT}=0A to short)



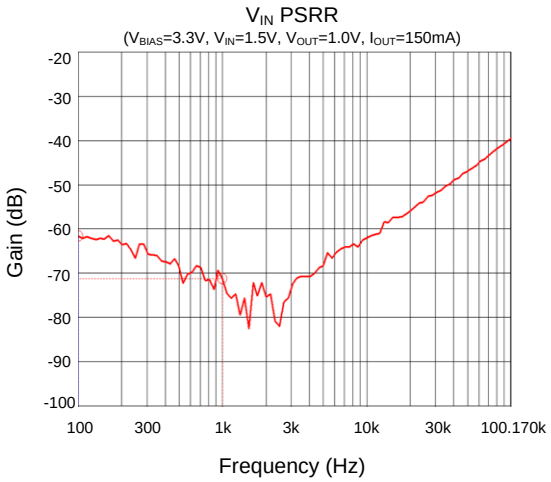
Time (800us/div)

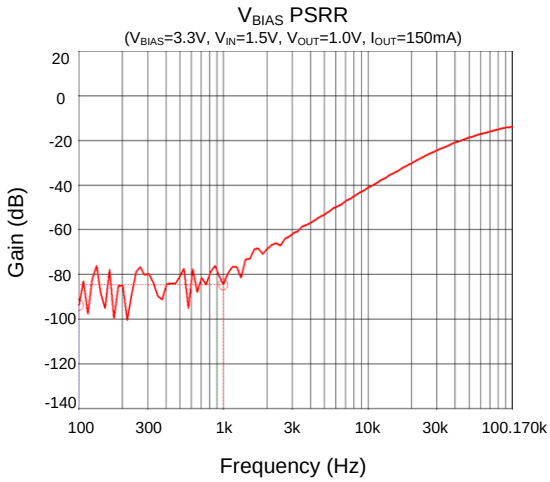
Hard Short Protection

(V_{BIAS}=3.3V, V_{IN}=1.2V, V_{OUT}=1.0V I_{OUT}=0.5A to short)



Time (800us/div)





Operation Information

The SY6307B is a low dropout LDO regulator with a compact DFN1.2×1.2-6 package, capable of delivering up to 500mA output current.

Input Capacitor C_{IN}

A 1μF input capacitor is required between the device input pin and the ground pin. A typical X5R or better grade ceramic capacitor with 6V rating is recommended in this application. This input capacitor must be placed close to the device to assure input stability. A lower ESR capacitor allows the use of smaller capacitance, while higher ESR type requires larger capacitance.

Output Capacitor C_{OUT}

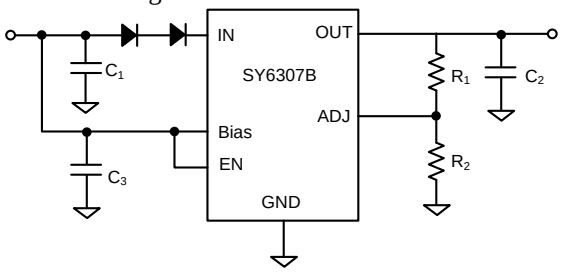
For transient stability, SY6307B is designed specifically to work with very small ceramic output capacitor. 2.2μF output capacitor with 10mΩ to 50mΩ ESR range (like X7R or X5R) can be used in this application. Larger capacitance values help to improve transient. The output capacitor's ESR is critical because it forms a zero to provide phase lead which is required for loop stability.

Bias Capacitor C_{BIAS}

A 0.1μF decouple capacitor at least is strongly recommended to place between the Bias pin and the ground pin. It shall be placed close to the device to achieve the best decouple performance.

Bias Voltage Requirement

The BIAS pin is the power supply pin for internal circuit. This pin should be higher than IN and OUT 1.35V to ensure the internal circuit is proper biased. If there is no higher power rail for VBIAS, it is recommended to add 2 diodes or a resister to reduce the VIN voltage.



No Load Stability

The device will remain stable and in regulation with no external load. This is especially important in CMOS RAM keep-alive applications.

Dropout Voltage

Keep V_{Bias} is higher than V_{OUT} +1.4V, decrease V_{IN} until V_{OUT} starts to decrease, the value V_{IN}-V_{OUT} is defined as V_{IN} dropout voltage. The V_{IN} dropout voltage is the regulator's minimum V_{IN}-V_{OUT}:

$$V_{DROPOUT} = V_{IN} - V_{OUT} = R_{DS(ON)} \times I_{OUT}$$

Current Limit

The minimum current limit of SY6307B is 500mA.

Short-circuit Protection

The SY6307B is short circuit protected and when the event of short circuit comes, the short-circuit control loop will rapidly limit the output current to the current limit value.

Thermal Considerations

The SY6307B can deliver a current of up to 500mA over the full operating junction temperature range. However, the maximum output current must be derated at higher ambient temperature to ensure the junction temperature does not exceed 125°C. With all possible conditions, the junction temperature must be within the range specified under operating conditions. Power dissipation can be calculated based on the output current and the voltage drop across regulator.

$$P_D = (V_{IN} - V_{OUT})I_{OUT}$$

The final operating junction temperature for any set of conditions can be estimated by the following thermal equation:

$$P_{DMAX} = (T_{J(MAX)} - T_A) / \theta_{JA}$$

Where $T_{J(MAX)}$ is the maximum junction temperature of the die and T_A is the maximum ambient temperature.

Layout Design

Good board layout practices must be used or instability can be induced because of ground loops and voltage drops, and large PCB copper area can improve the thermal performance. The input and output capacitors MUST be directly connected to the input, output and ground pins of the device using traces which have no other currents flowing through them. The best way to do this is to layout C_{IN} and C_{OUT} near the device with short traces to the IN, OUT and ground pins.

Below is the recommended PCB Layout diagram:

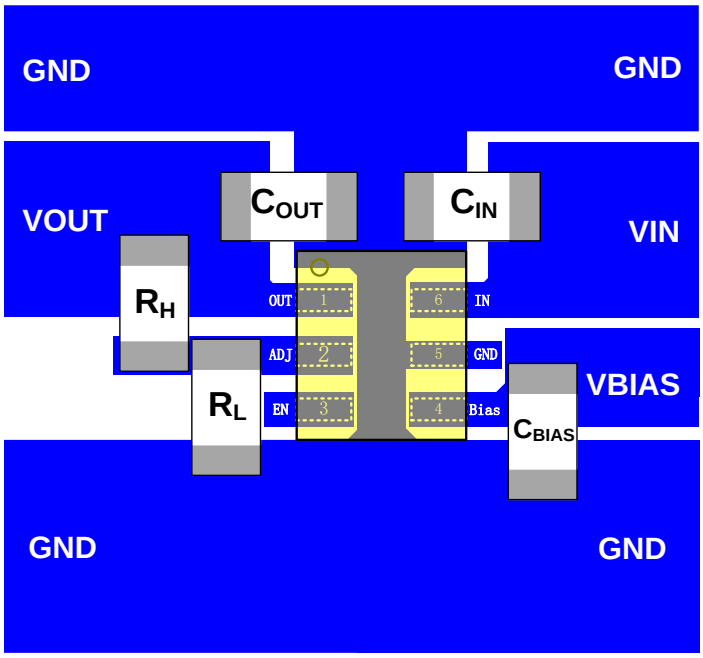
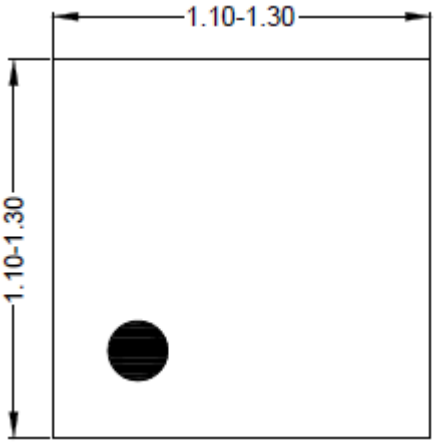
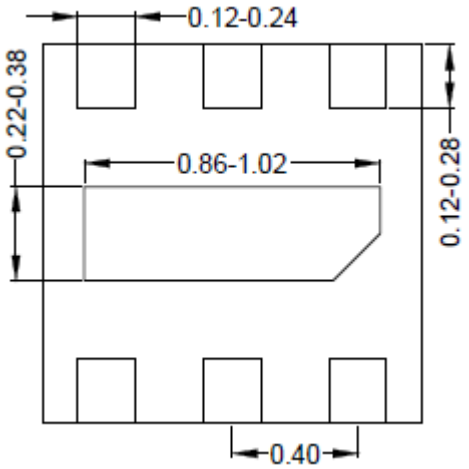


Figure4. PCB Layout Suggestion

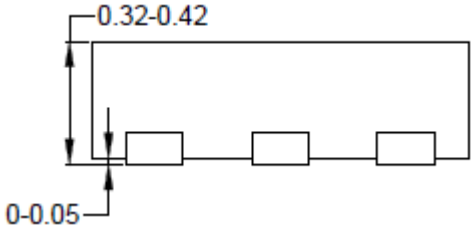
DFN1.2×1.2-6 Package Outline Drawing



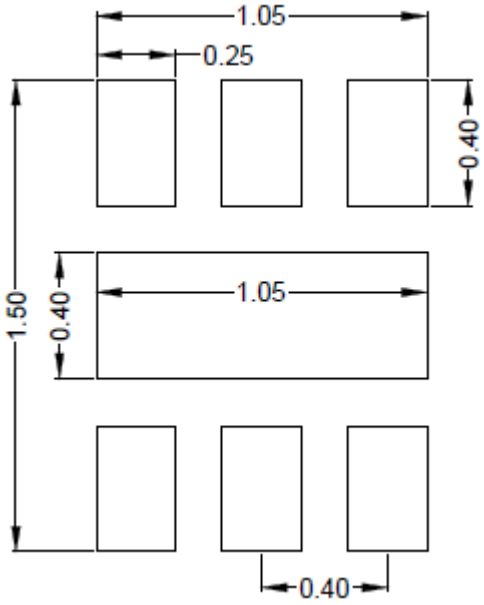
Top view



Bottom view



Side view



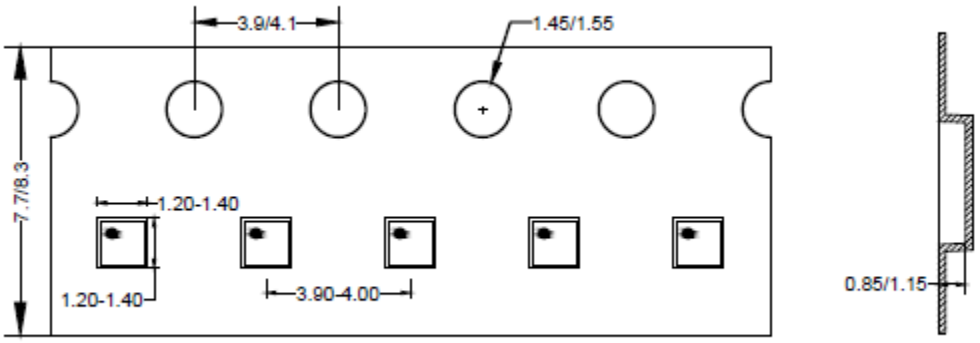
Recommended PCB layout
(Reference only)

Notes: **All dimension in millimeter and exclude mold flash & metal burr.**

Taping & Reel Specification

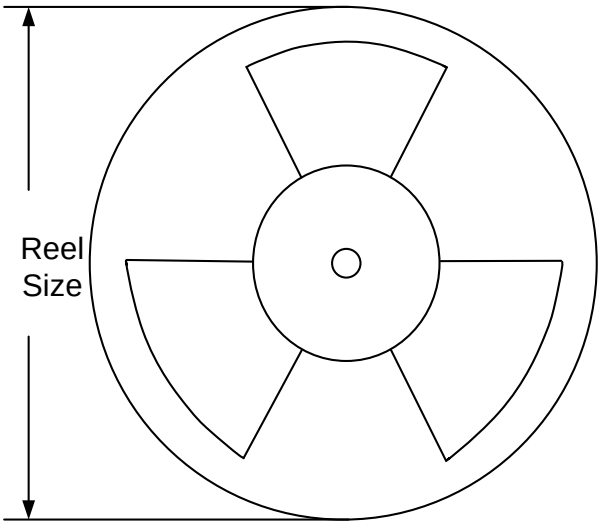
1. Taping orientation

DFN1.2×1.2



Feeding direction ⟶

2. Carrier Tape & Reel specification for packages



Package type	Tape width (mm)	Pocket pitch(mm)	Reel size (Inch)	Trailer length(mm)	Leader length (mm)	Qty per reel
DFN1.2×1.2	8	2	7"	400	160	5000

3. Others: NA

Revision History

The revision history provided is for informational purpose only and is believed to be accurate, however, not warranted. Please make sure that you have the latest revision.

Date	Revision	Change
May 28, 2020	Revision 0.9C	Add Bias Voltage Requirement in Operation Information
Mar 21, 2019	Revision 0.9B	Qty per reel change from 10000 to 5000
Mar 20, 2018	Revision 0.9A	1. Update in "Absolute Maximum Ratings" a. Change from "All pins ---------- 6.0V" to "IN, OUT, Bias, EN, ADJ ---------- -0.3V to 6.0V". b. Change from "Junction Temperature Range ---------- 150°C" to "Junction Temperature Range --------- -40°C to 150°C". 2. Update in "Recommended Operating Conditions" Add "IN ---------- 0.8V to 5.5V OUT ---------- 0.8V to VBias-1.4V". 3. Update in "Dropout Voltage" in Page9 Change from "When V_{Bias} is high enough" to "Keep V_{Bias} is higher than V_{OUT} +1.4V".
Apr 25, 2017	Revision 0.9	Initial Release

IMPORTANT NOTICE

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