SY6018

Analog Class-D Audio IC

General Description

The SY6018 is a Class-D audio power amplifier with analog input and high-power efficiency for driving bridge-tied stereo speakers with up to 2×30W/8Ω or a bridge-tied mono speaker with up to 60W/4Ω. The efficiency of the SY6018 eliminates the need for an external heat sink when playing music.

The SY6018 advanced oscillator/PLL circuit employs a multiple switching frequency option to avoid AM/AF interferences; this is achieved together with an option of Master and Slave synchronization, making it possible to synchronize multiple devices.

The SY6018 is fully protected against faults including short circuit, over temperature, DC error, under voltage and over voltage. The short circuit, over temperature and DC error protection includes an auto-recovery feature. The under voltage and over voltage protection with hysteresis can be self-cleared.

Ordering Information

SY6018 □(□□)□

- Temperature Code
- Package Code
- Optional Spec Code

Ordering Number	Package type	Note
SY6018QEC	QFN5×5-32	

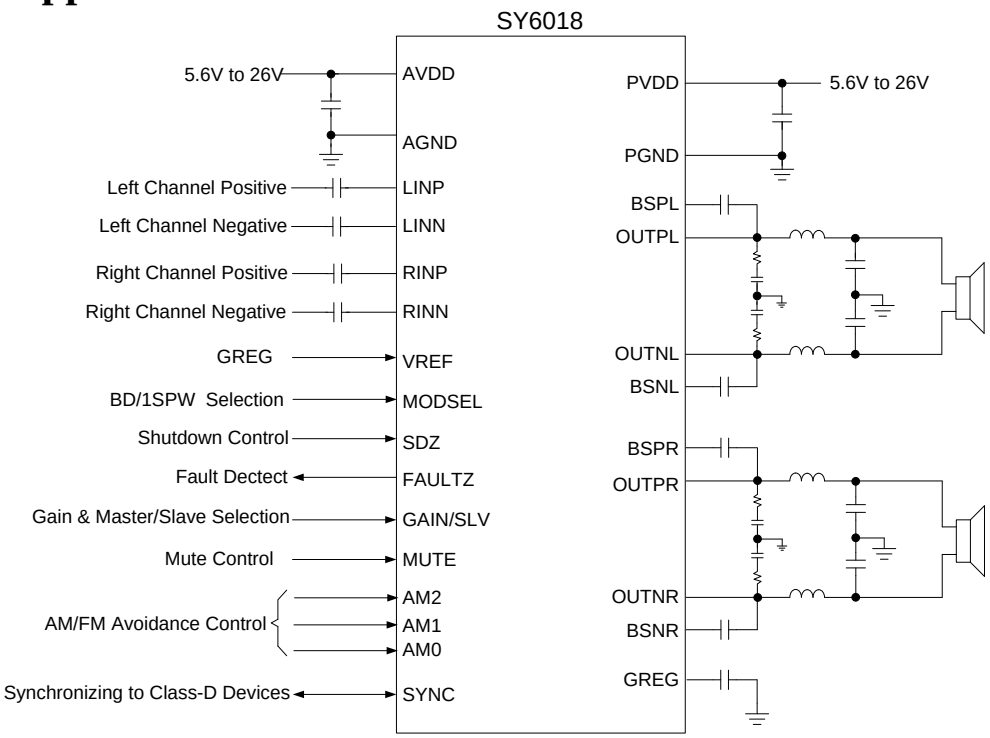
Features

- 2×30W into 8Ω BTL Loads @ 10% THD+N from a 24V Supply
- 60W into a 4Ω PBTL Load @ 10% THD+N from a 24V Supply
- Wide Voltage Range: 5.6V to 26V
- Filter-free Operation
- Differential and Single-ended Inputs
- Internal Feedback Control with High PSRR
- High Efficiency Class-D Operation Eliminates Need for Heat Sinks
- AM/AF Avoidance
- Master and Slave Synchronization
- Four Fixed-gain Controlled: 20dB, 26dB, 32dB and 36dB
- Selectable BD Mode and 1SPW Mode Modulation
- Integrated Protection Circuits Including Over Voltage, Under Voltage, Over Temperature, DC Error, and Short Circuit
- Comprehensive Click and Pop Suppression
- Space-saving Surface Mount 32Pin QFN 5mm×5mm Package

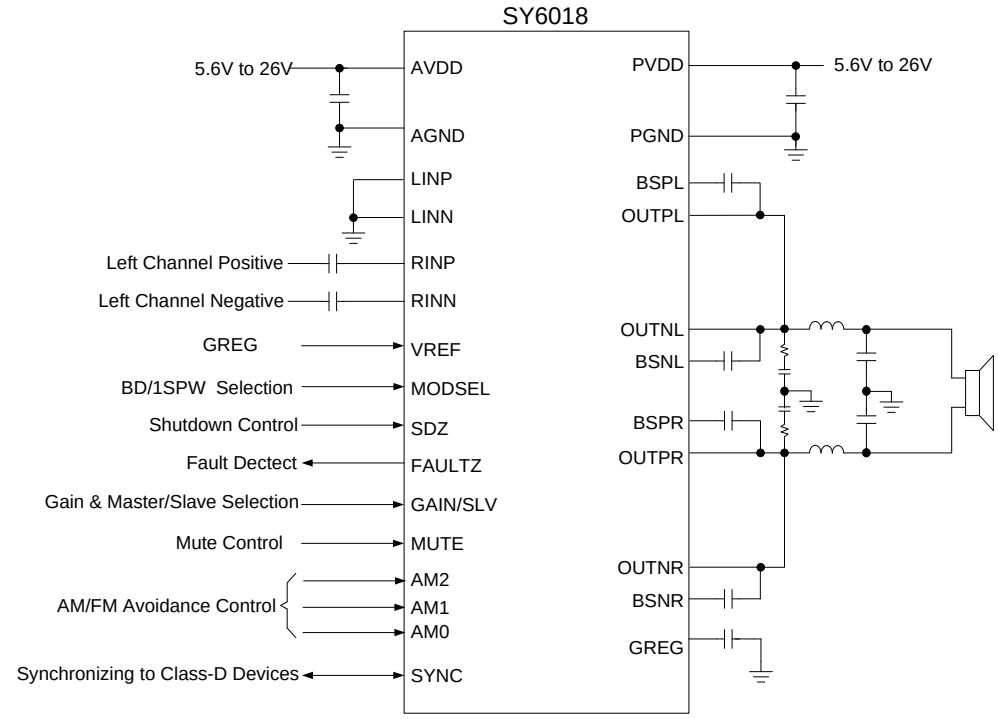
Applications

- Flat Panel Display TVs
- DLP® TVs
- CRT TVs
- Powered Speakers
- Music Instruments
- Boom Box
- Consumer Audio Applications

Typical Applications



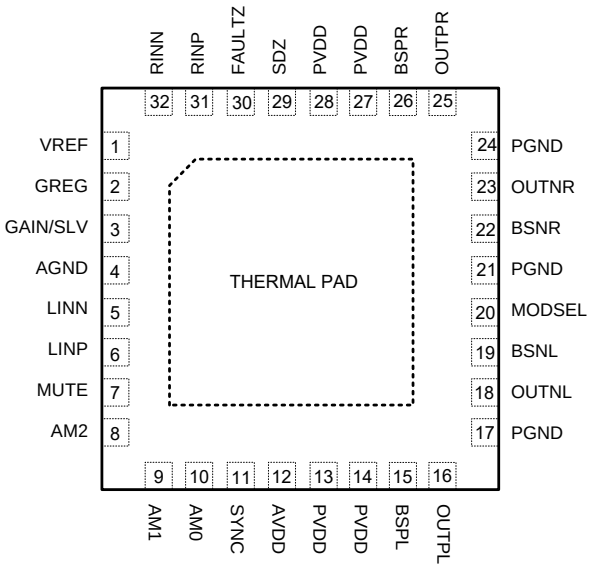
(a) Stereo Class-D Amplifier with BTL Output



(b) Mono Class-D Amplifier with PBTL Output

Fig.1 Typical Application Circuit

Pinout (top view)



(QFN5×5-32)

Top Mark: BHL*xyz* (device code: BHL, ***x=year code, y=week code, z= lot number code)***

Pin Name	Pin Number	Description
VREF	1	Internal reference pin. Connect to GREG directly.
GREG	2	Gate drive supply. Nominal voltage is 3.4V.
GAIN/SLV	3	Gain & Master/Slave mode selection depending on voltage divider from GREG to GND.
AGND	4	Analog Ground.
LINN	5	Negative audio input for left channel. Biased at 1.7V.
LINP	6	Positive audio input for left channel. Biased at 1.7V.
MUTE	7	Mute pin (high=mute, low=unmute), TTL logic levels with compliance to AVDD.
AM2	8	AM/AF avoidance frequency selection.
AM1	9	AM/AF avoidance frequency selection.
AM0	10	AM/AF avoidance frequency selection.
SYNC	11	Clock input/output for synchronizing other Class-D devices. Determined by GAIN/SLV pin.
AVDD	12	Analog power supply. Not internally connected to PVDD.
PVDD	13	Power supply.
PVDD	14	Power supply.
BSPL	15	Bootstrap for left positive channel output.
OUTPL	16	Positive left channel output.
PGND	17	Power Ground.
OUTNL	18	Negative left channel output.
BSNL	19	Bootstrap for left negative channel output.
MODSEL	20	Mode selection (low=BD, high=1SPW), TTL logic levels with compliance to AVDD.
PGND	21	Power Ground.
BSNR	22	Bootstrap for right negative channel output.
OUTNR	23	Negative right channel output.
PGND	24	Power Ground.
OUTPR	25	Positive left channel output.

BSPR	26	Bootstrap for right positive channel output.
PVDD	27	Power supply.
PVDD	28	Power supply.
SDZ	29	Shutdown pin (low = enter shutdown, high = exit shutdown). TTL logic levels with compliance to AVDD.
FAULTZ	30	Open drain output used to display general fault, including SCP, OTP, DCP fault status (low=fault, high=normal).
RINP	31	Positive audio input for right channel. Biased at 1.7V.
RINN	32	Negative audio input for right channel. Biased at 1.7V.
Thermal Pad	33	Connect to GND for best system performance.

Block Diagram

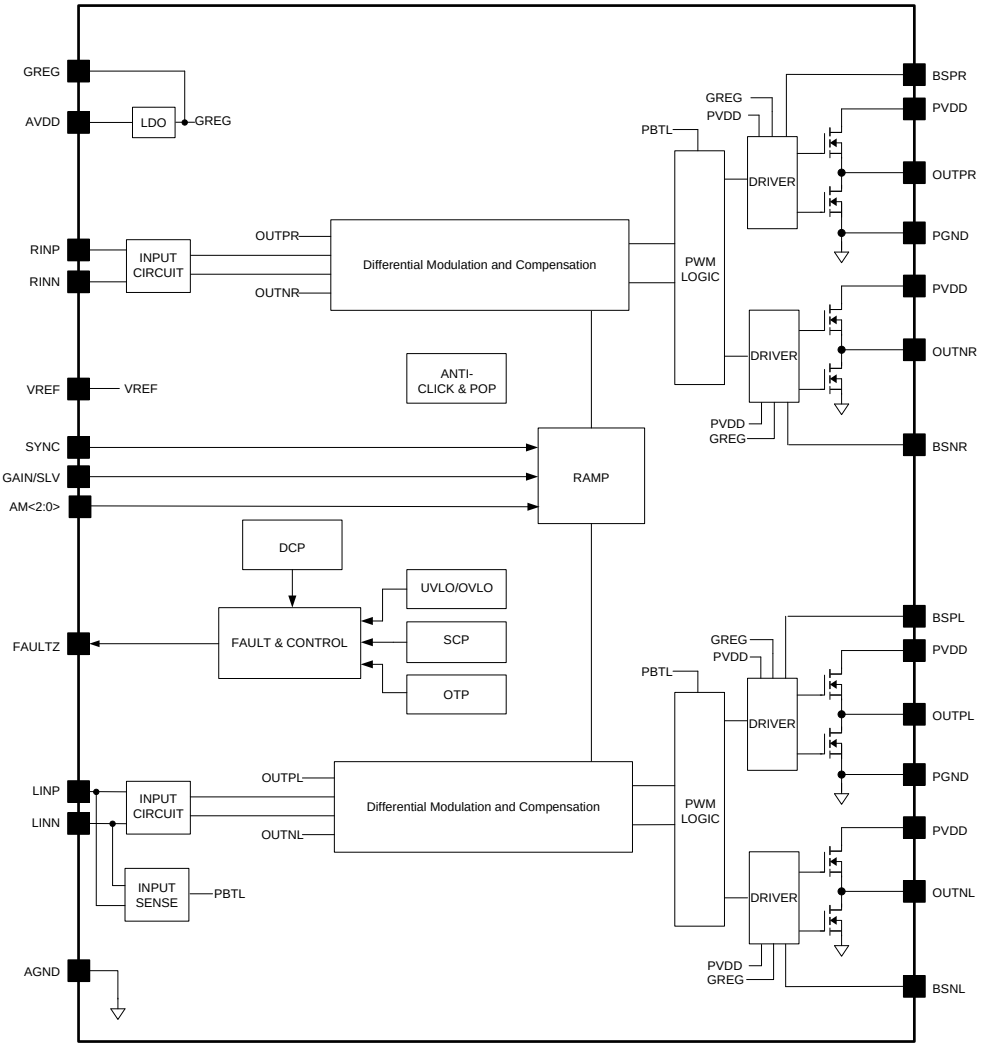


Fig.2 Block Diagram

Absolute Maximum Ratings (Note 1)

AVDD, PVDD (Note 2) ---------- -0.3V to 30V
RIN, LIN ---------- -0.3V to 3.6V
MODSEL, SDZ, MUTE, AM2, AM1, AM0 ---------- -0.3V to (AVDD +0.3)V
VREF, GAIN/SLV, SYNC ---------- -0.3V to (GREG+0.3)V
Minimum Load Resistance Output Configuration ---------- 3.2Ω
Junction Temperature Range ---------- -40°C to 150°C
Storage Temperature Range ---------- -40°C to 125°C
Package Thermal Resistance
θ_{JA} (Note 3) ---------- 22°C/W
θ_{JC} ---------- 8°C/W

Recommended Operating Conditions

Supply Voltage Range ---------- 5.6V to 26V
Junction Temperature Range ---------- -40°C to 125°C
Ambient Temperature Range ---------- -40°C to 85°C

Electrical Characteristics

(T_A =25°C, V_{DD}=19V, R_L=8Ω, Gain=26dB, unless otherwise specified.)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
DC Characteristics						
AVDD, PVDD	V_{DD}		5.6		26	V
Quiescent Supply Current	I_Q	SDZ=1, no load or filter (Note 4)		18.5		mA
		SDZ=0, no load or filter		100	122	μA
High-level Input Voltage	V_{IH}	SDZ, SYNC, MUTE, AM2, AM1, AM0	2.05			V
		MODSEL (Note 4)		1.75		V
Low-level Input Voltage	V_{IL}	SDZ, SYNC, MUTE, AM2, AM1, AM0			0.75	V
		MODSEL (Note 4)		1		V
Low-level Output Voltage (Note 4)	V_{OL}	FAULTZ, $R_{PULL-UP}$=100kΩ, PVDD=26V		0.22		V
High-level Input Current	I_{IH}	MODESEL, MUTE, AM2, AM1, AM0, V_I= 2V	-0.1		0.1	μA
		SDZ, V_I= 2V	4	6	8	μA
Drain-Source On-State Resistance	$R_{DS(ON)}$			105	130	mΩ
Gain (Master)	G	R1=Open, R2=5.6kΩ, no load (Note 4)		20		dB
		R1=100kΩ, R2=20kΩ, no load	25.5	26	26.5	
		R1=100kΩ, R2=39kΩ, no load (Note 4)		32		
		R1=75kΩ, R2=47kΩ, no load (Note 4)		36		

Gain (Slave)	G	R1=51kΩ, R2=51kΩ, no load (Note 4)		20		dB
		R1=47kΩ, R2=75kΩ, no load (Note 4)		26		
		R1=39kΩ, R2=100kΩ, no load (Note 4)		32		
		R1=16kΩ, R2=100kΩ, no load	35.5	36	36.5	
Turn-on Time (Note 4)	t_{ON}	SDZ=1		45		ms
Turn-off Time (Note 4)	t_{OFF}	SDZ=0		1		μs
Output Offset Voltage	$\|V_{OS}\|$	V_I=0V, Measured Differentially at V_{DD} =6V		1.5	15	mV
Gate Drive Supply	GREG	SDZ=1, V_I=0V	3.2	3.4	3.6	V
Oscillator Frequency	f_{OSC}	AM2=0,AM1=0,AM0=0	350	400	428	kHz
		AM2=0,AM1=0,AM0=1	437.5	500	535	
		AM2=0,AM1=1,AM0=0	525	600	642	
		AM2=0,AM1=1,AM0=1	875	1000	1070	
		AM2=1,AM1=0,AM0=0	1050	1200	1284	
		AM2=1,AM1=0,AM0=1	Reserved			
		AM2=1,AM1=1,AM0=0	Reserved			
		AM2=1,AM1=1,AM0=1	Reserved			
AC Characteristics (Note 4)						
Output Integrated Noise	V_n	20Hz to 22kHz, A-weighted filter, Gain=20dB		65		μV
Signal to Noise Ratio	SNR	Max output at THD+N<1%, V_{DD}=6V, f=1kHz, Gain=20dB, A-weighted		95.7		dB
		Max output at THD+N<1%, V_{DD}=12V, f=1kHz, Gain=20dB, A-weighted		102		
		Max output at THD+N<1%, V_{DD}=19V, f=1kHz, Gain=20dB, A-weighted		105.5		
		Max output at THD+N<1%, V_{DD}=21V, f=1kHz, Gain=20dB, A-weighted		106.5		
		Max output at THD+N<1%, V_{DD}=24V, f=1kHz, Gain=20dB, A-weighted		107.5		
Total Harmonic Distortion +Noise	THD+N	V_{DD}=6V, f=1kHz, Po=0.5W		0.035		%
		V_{DD}=6V, f=1kHz, Po=1W		0.035		
		V_{DD}=12V, f=1kHz, Po=1W		0.03		
		V_{DD}=12V, f=1kHz, Po=4W		0.035		
		V_{DD}=19V, f=1kHz, Po=1W		0.03		
		V_{DD}=19V, f=1kHz, Po=10W		0.04		
		V_{DD}=21V, f=1kHz, Po=1W		0.03		
		V_{DD}=21V, f=1kHz, Po=12W		0.04		
		V_{DD}=24V, f=1kHz, Po=1W		0.03		
		V_{DD}=24V, f=1kHz, Po=15.5W		0.045		
Output Power	P_O	V_{DD}=6V, f=1kHz, 1% THD+N		2		W

		V_{DD}=6V, f=1kHz, 10% THD+N		2.5		
		V_{DD}=12V, f=1kHz, 1% THD+N		8		
		V_{DD}=12V, f=1kHz, 10% THD+N		10		
		V_{DD}=19V, f=1kHz, 1% THD+N		19.8		
		V_{DD}=19V, f=1kHz, 10% THD+N		24.7		
		V_{DD}=21V, f=1kHz, 1% THD+N		24.2		
		V_{DD}=21V, f=1kHz, 10% THD+N		30		
		V_{DD}=24V, f=1kHz, 1% THD+N		31.4		
		V_{DD}=24V, f=1kHz, 10% THD+N		38.7		
Crosstalk		Vo=1Vrms, f=1kHz, Gain=20dB		-96		dB
Power Supply Rejection Ratio	PSRR	200mV_{PP} ripple, f=1kHz , Gain=20dB		-73		dB
Protection						
V_{DD} Under Voltage Lockout Voltage	V_{UVLO_RISE}	V_{DD} rising		5.5	5.6	V
	V_{UVLO_FALL}	V_{DD} falling	4.9	5.2	5.3	V
V_{DD} Over Voltage Lockout Voltage	V_{OVLO_RISE}	V_{DD} rising		31	32.5	V
	V_{OVLO_FALL}	V_{DD} falling	26.5	28		V
Short Circuit Protection Current Limit (Note 4)	I_{SC}			15		A
Thermal Shutdown Temperature (Note 4)	T_{SD}			150		°C

Note 1: Stresses beyond the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: DC voltage rating could be derated a little according to the possible switching spike on switching node if the snubber is not appropriate enough.

Note 3: θ_{JA} is measured in the natural convection at T_A=25°C on a low effective single layer thermal conductivity test board of JEDEC 51-3 thermal measurement standard.

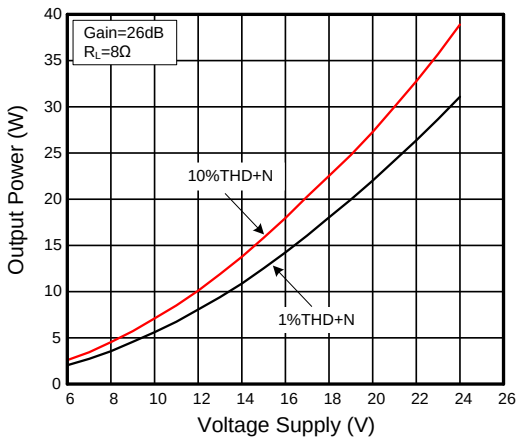
Note 4: Typical test value on demonstration board, guarantee by design.

Typical Performance Characteristics

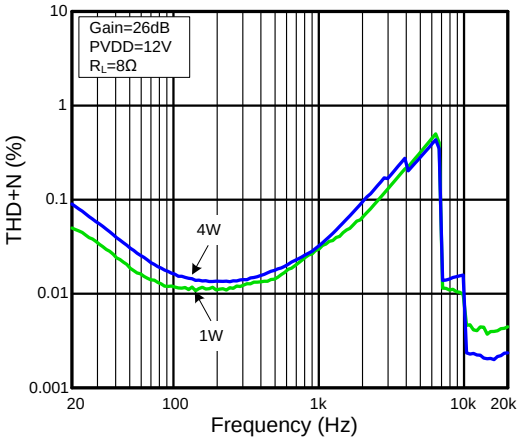
(All Measurements taken at 1 kHz, f_{OSC}= 400 kHz, unless otherwise noted.)

BTL (8Ω)

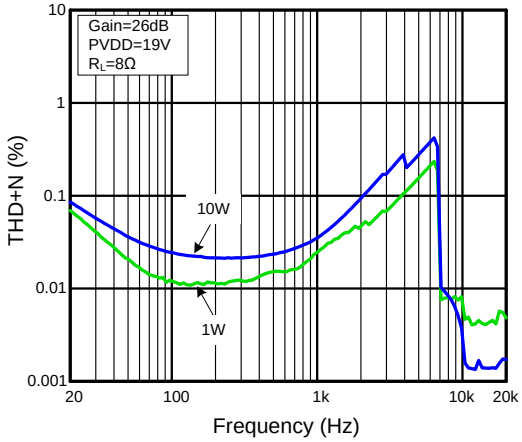
Maximum Output Power vs. Supply Voltage



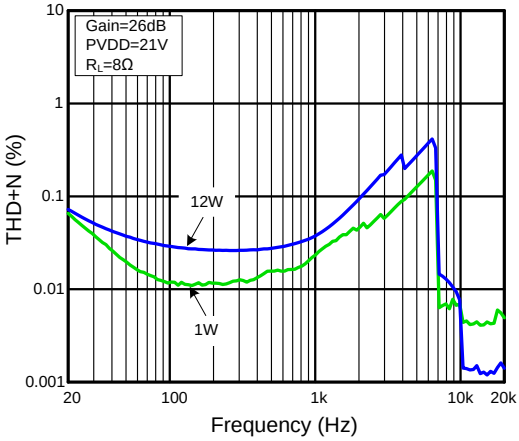
THD+N vs. Frequency



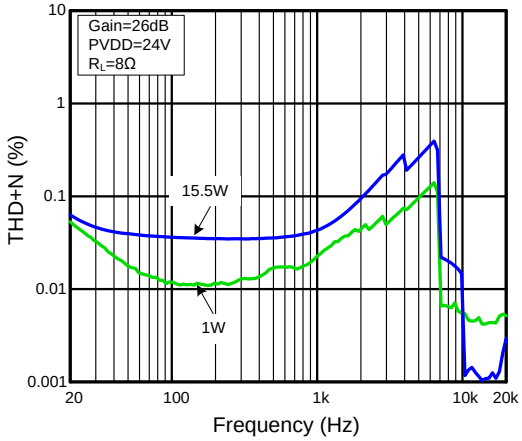
THD+N vs. Frequency



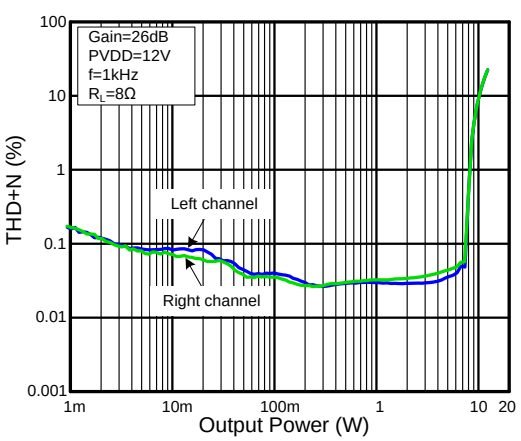
THD+N vs. Frequency



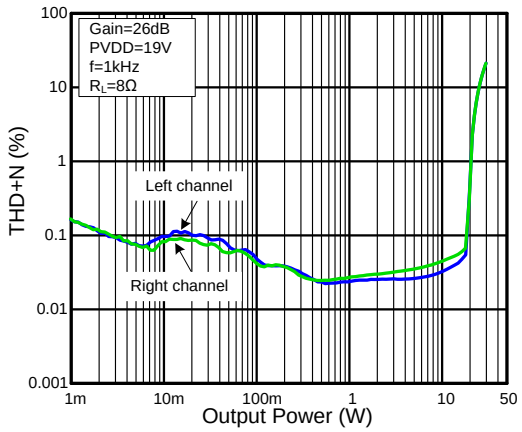
THD+N vs. Frequency



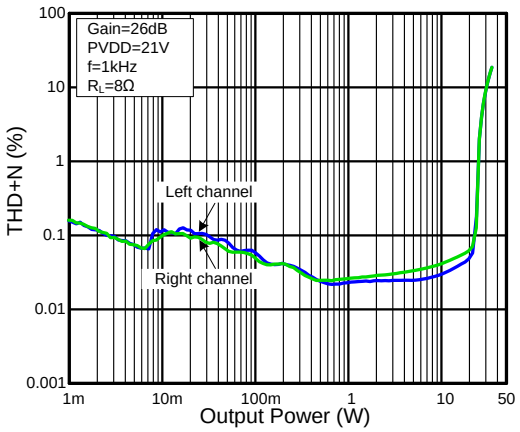
THD+N vs. Output Power



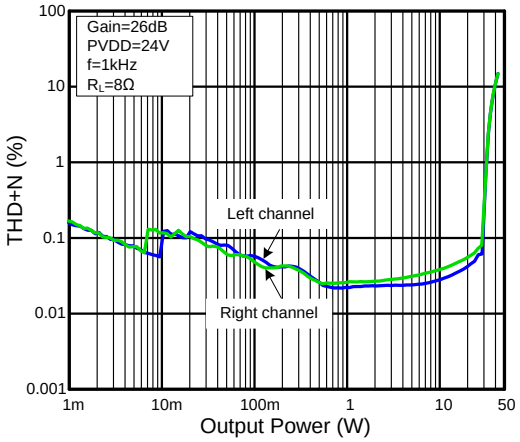
THD+N vs. Output Power



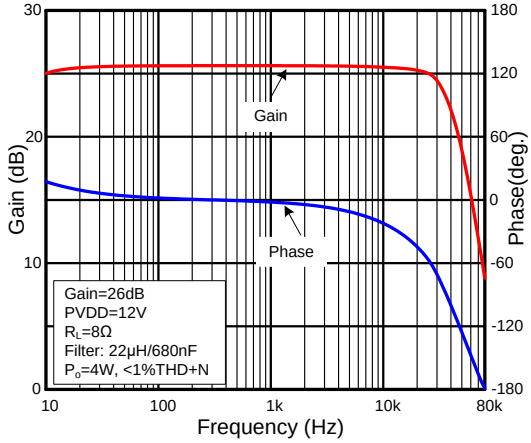
THD+N vs. Output Power



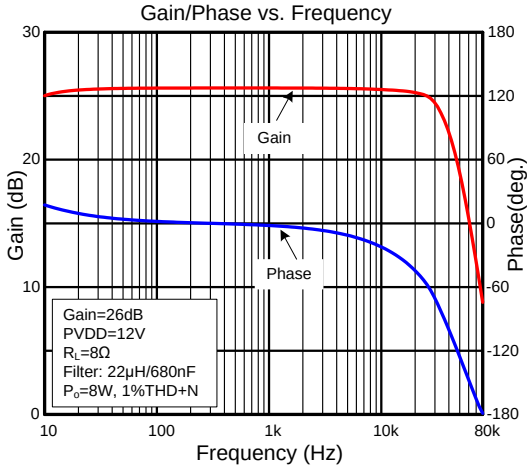
THD+N vs. Output Power



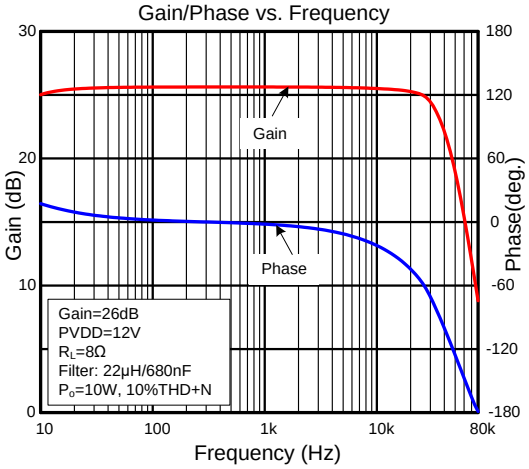
Gain/Phase vs. Frequency



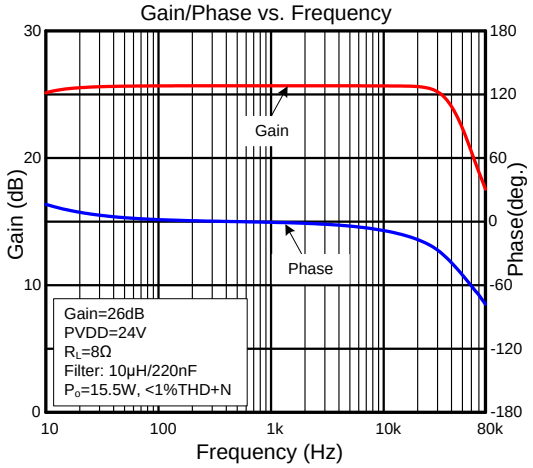
Gain/Phase vs. Frequency



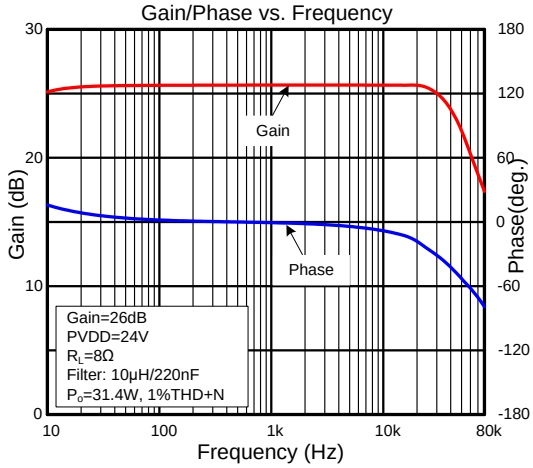
Gain/Phase vs. Frequency



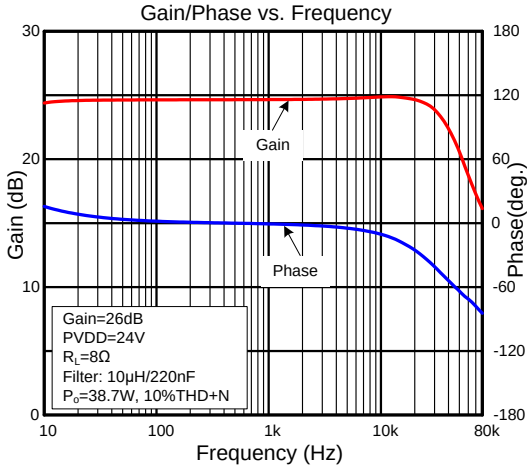
Gain/Phase vs. Frequency



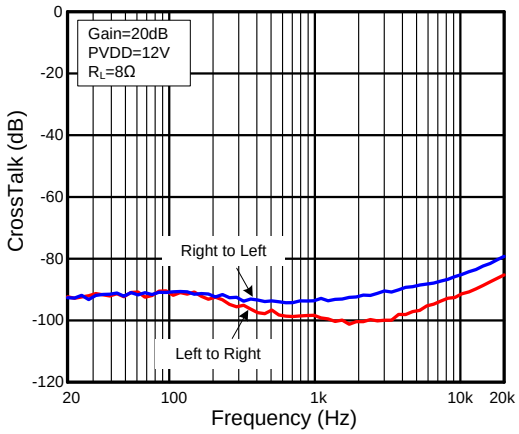
Gain/Phase vs. Frequency



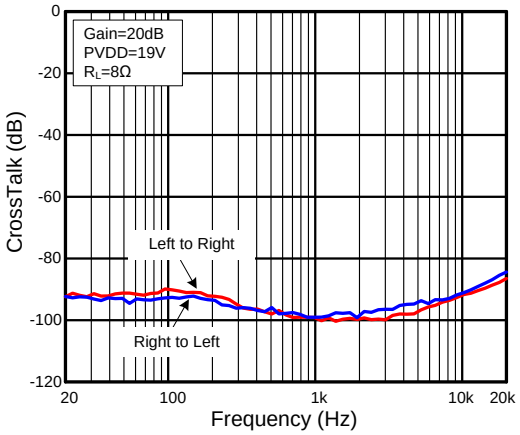
Gain/Phase vs. Frequency



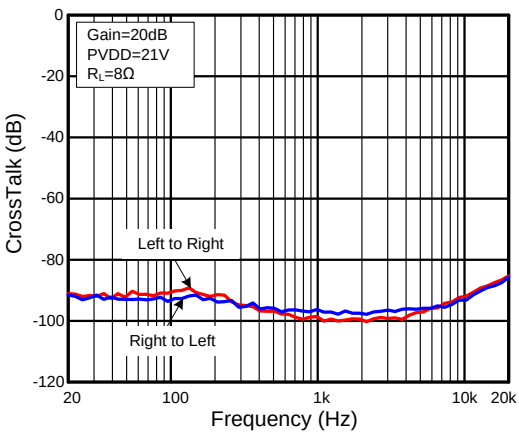
Crosstalk vs. Frequency



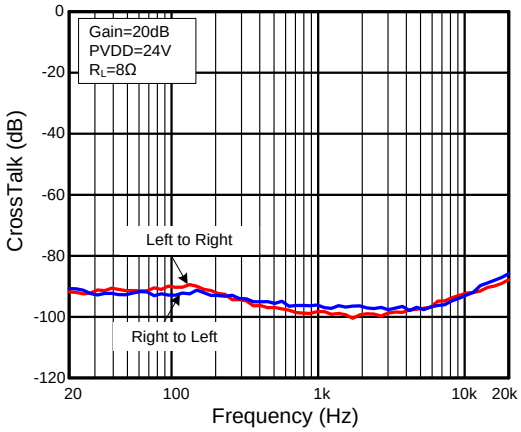
Crosstalk vs. Frequency



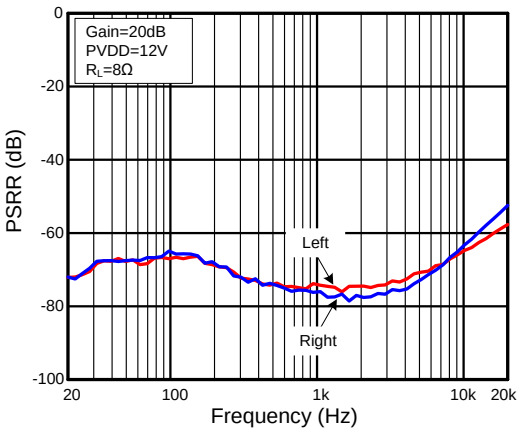
Crosstalk vs. Frequency



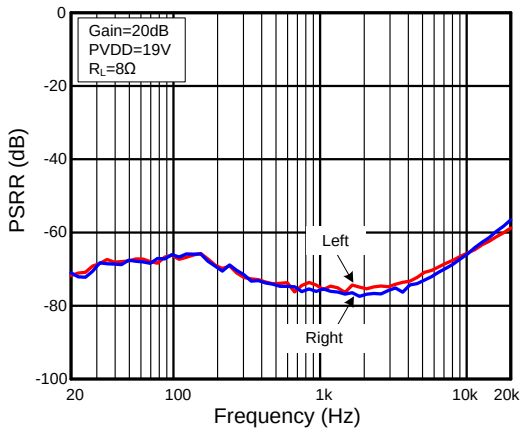
Crosstalk vs. Frequency



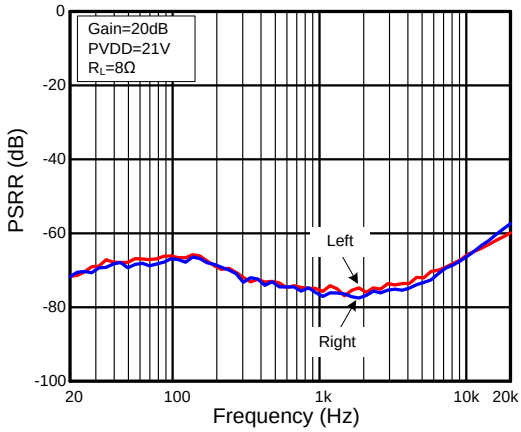
PSRR vs. Frequency



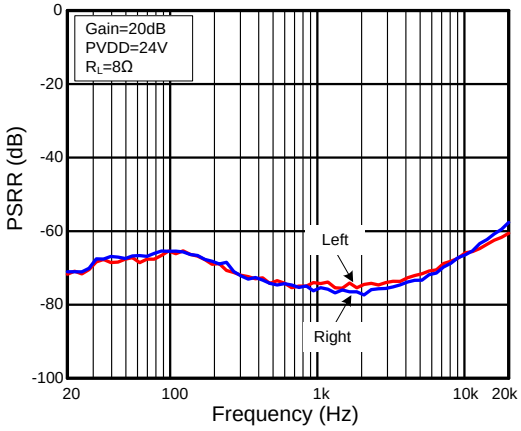
PSRR vs. Frequency



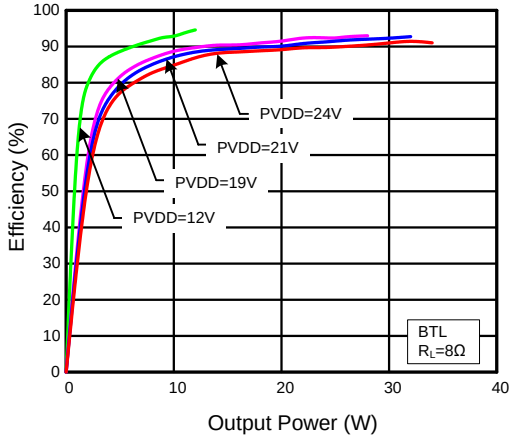
PSRR vs. Frequency



PSRR vs. Frequency

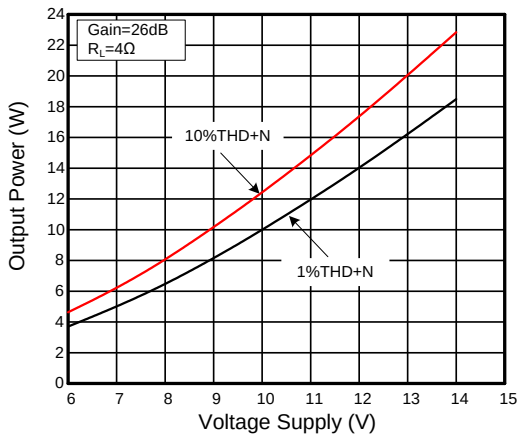


Efficiency vs. Power

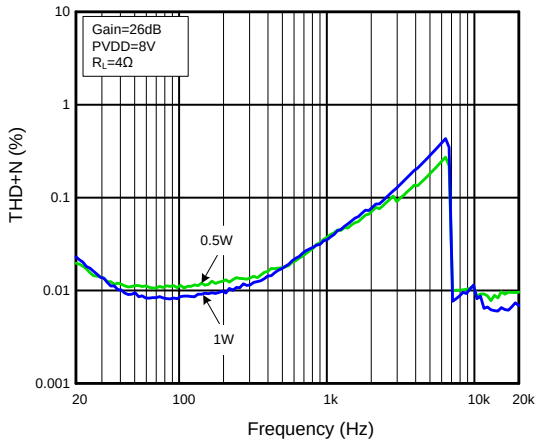


BTL (4Ω)

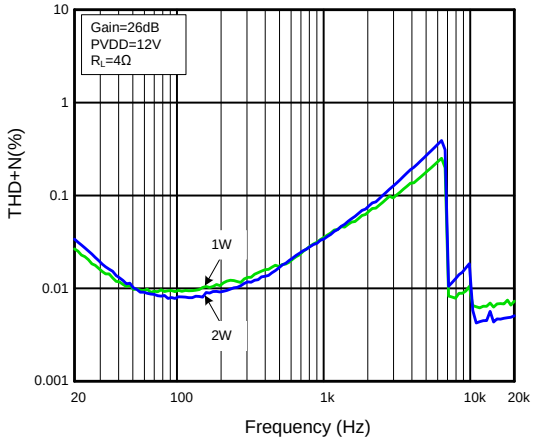
Maximum Output Power vs. Supply Voltage



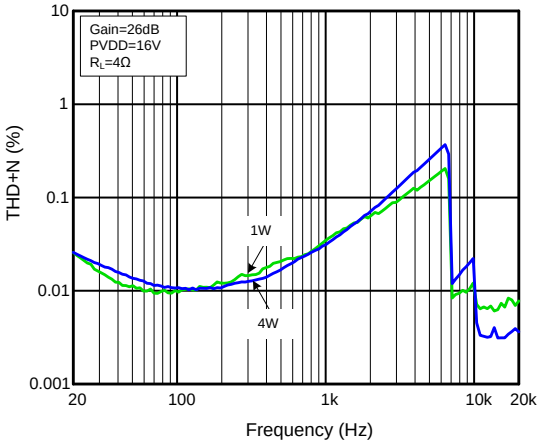
THD+N vs. Frequency



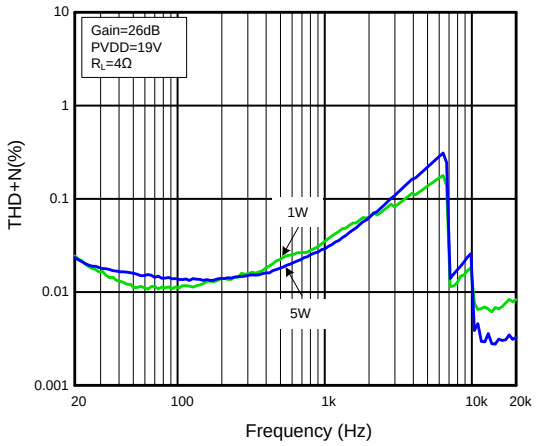
THD+N vs. Frequency



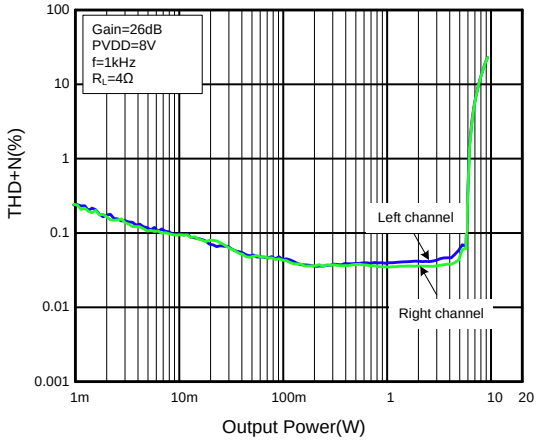
THD+N vs. Frequency



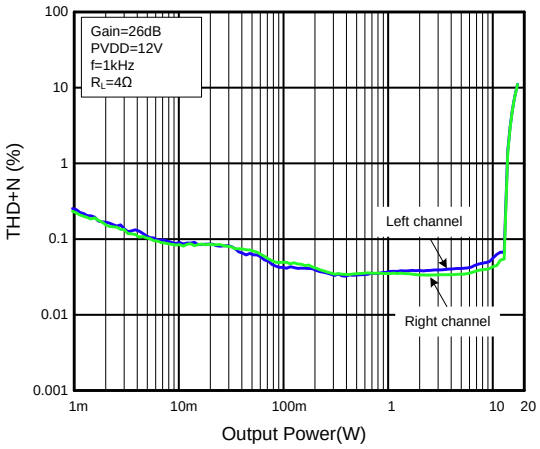
THD+N vs. Frequency



THD+N vs. Output Power



THD+N vs. Output Power



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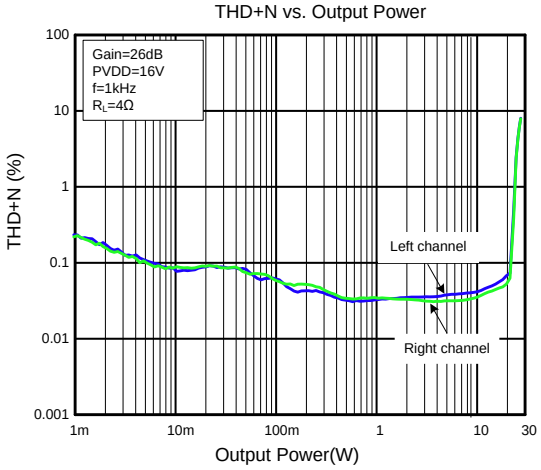
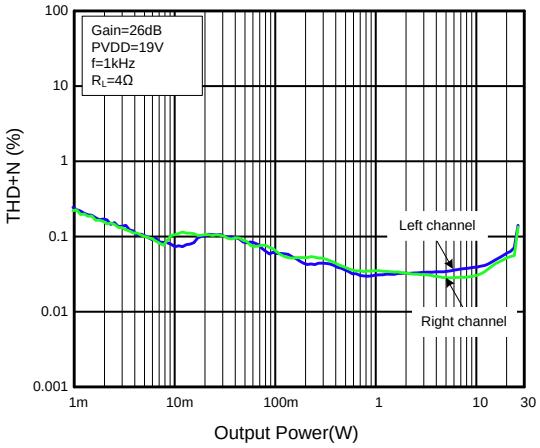
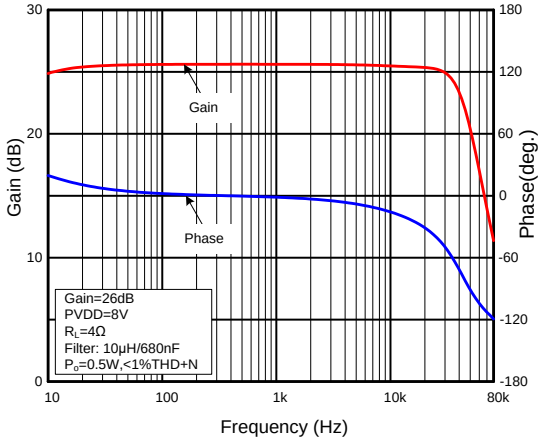


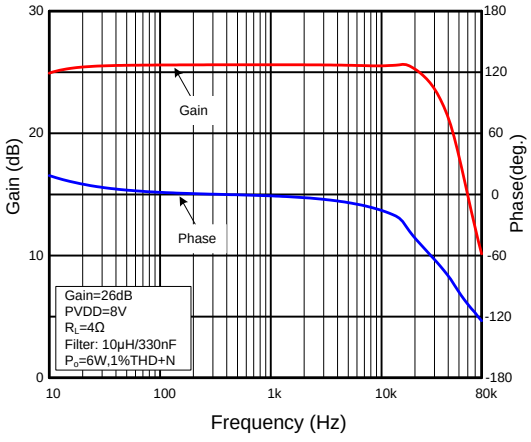
THD+N vs. Output Power



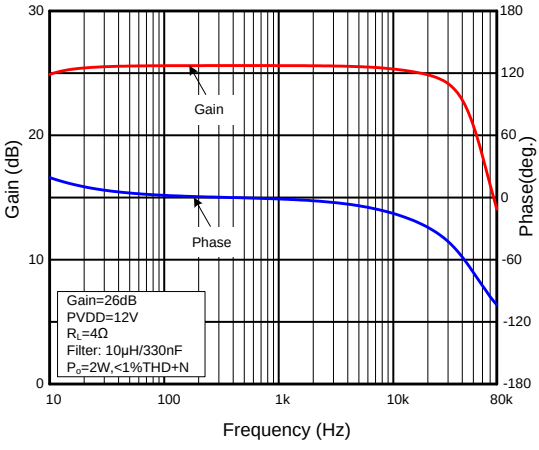
Gain/Phase vs. Frequency



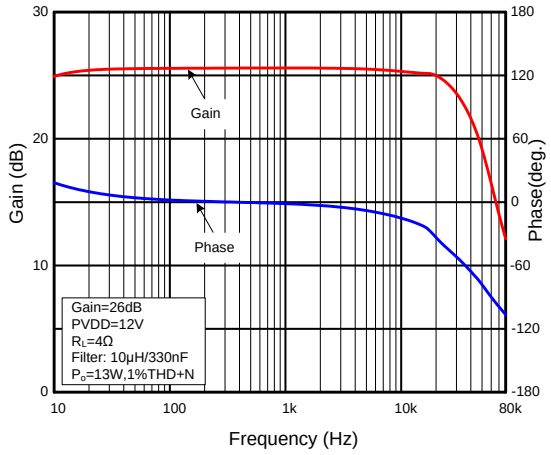
Gain/Phase vs. Frequency



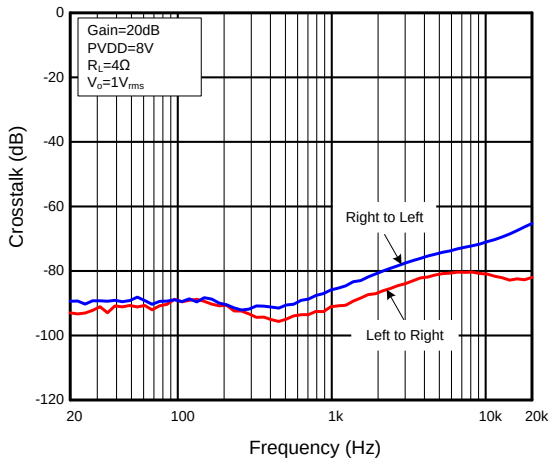
Gain/Phase vs. Frequency



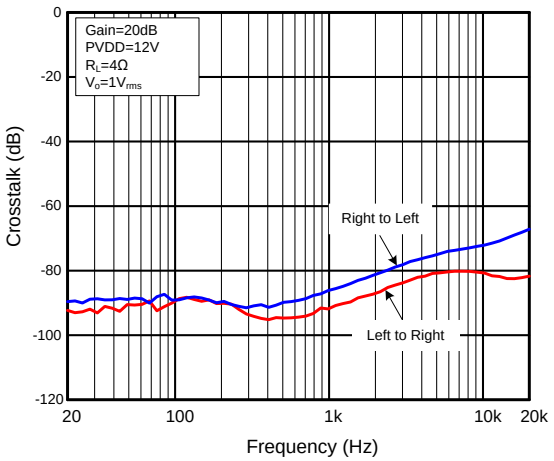
Gain/Phase vs. Frequency



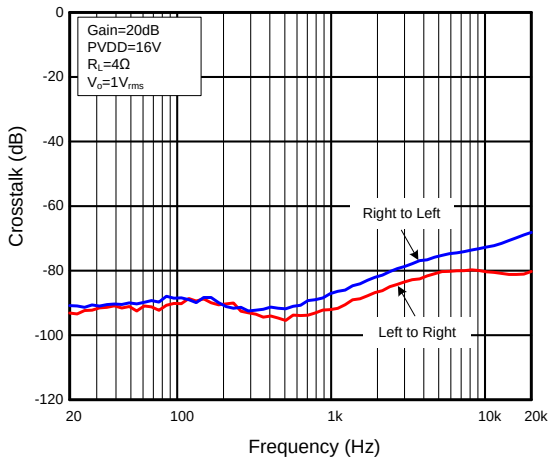
Crosstalk vs. Frequency



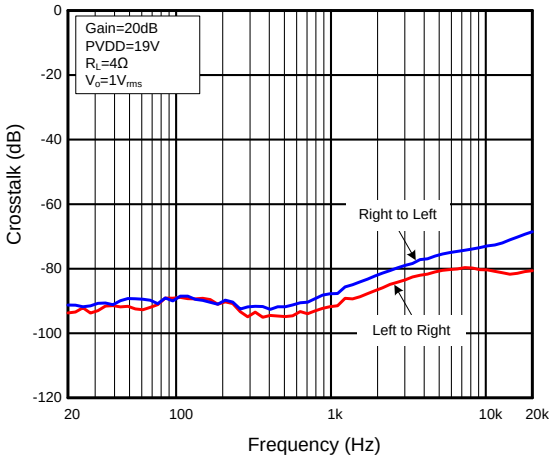
Crosstalk vs. Frequency



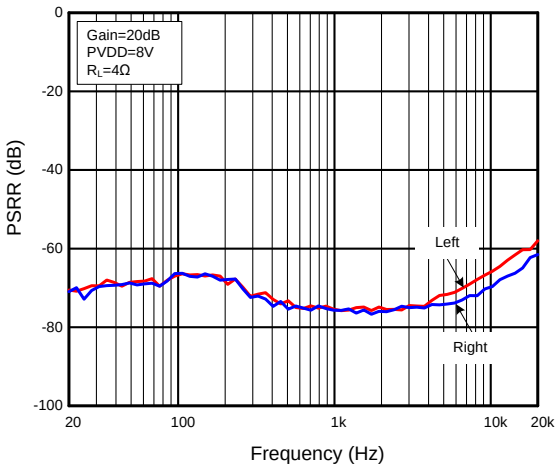
Crosstalk vs. Frequency



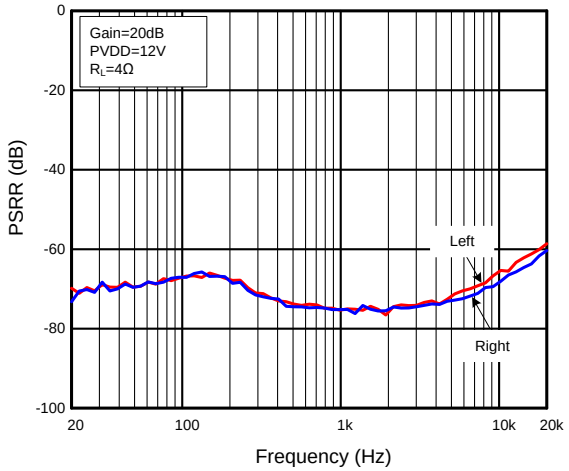
Crosstalk vs. Frequency



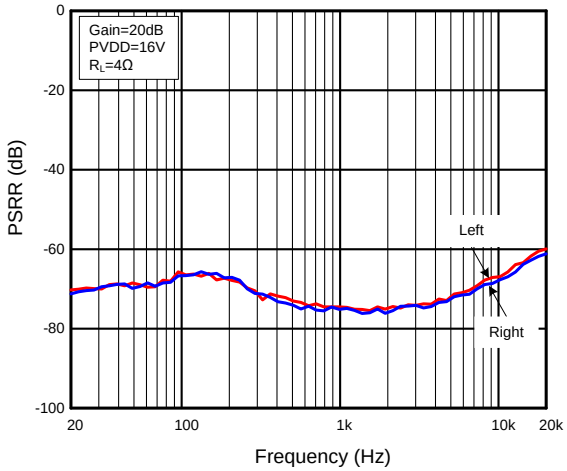
PSRR vs. Frequency



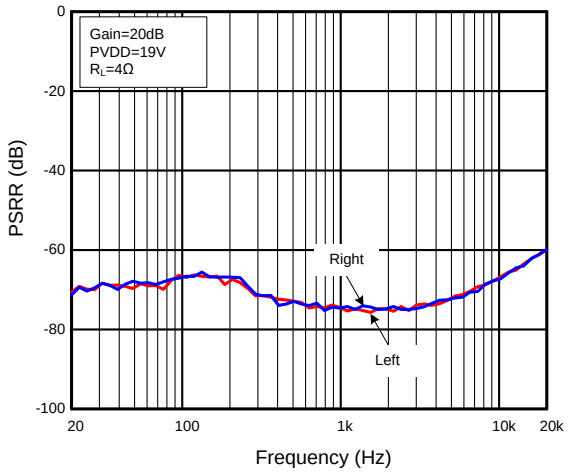
PSRR vs. Frequency



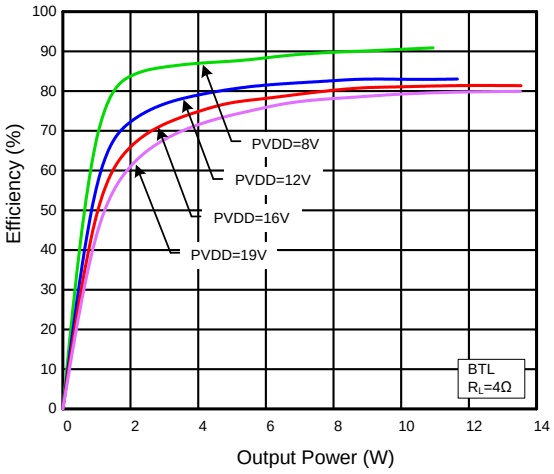
PSRR vs. Frequency



PSRR vs. Frequency

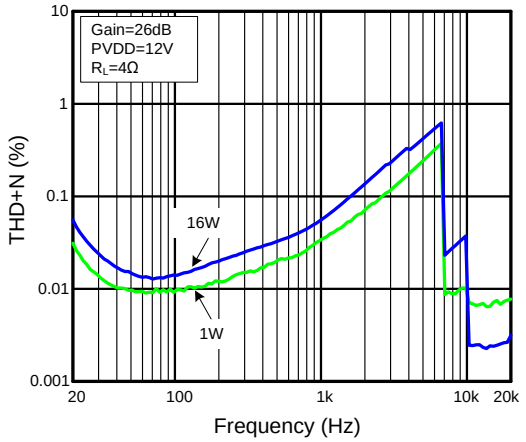


Efficiency vs. Power

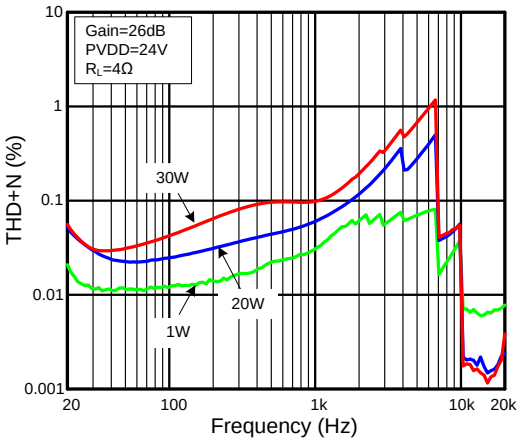


PBTL (4Ω)

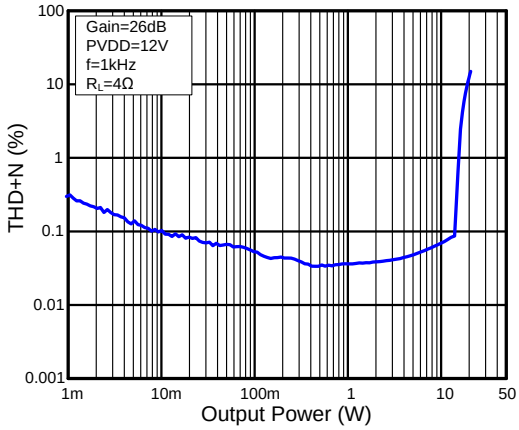
THD+N vs. Frequency



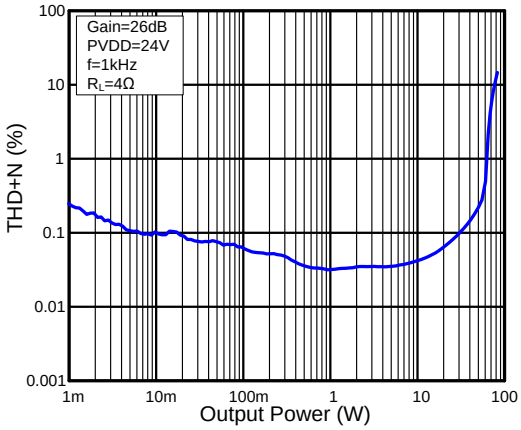
THD+N vs. Frequency



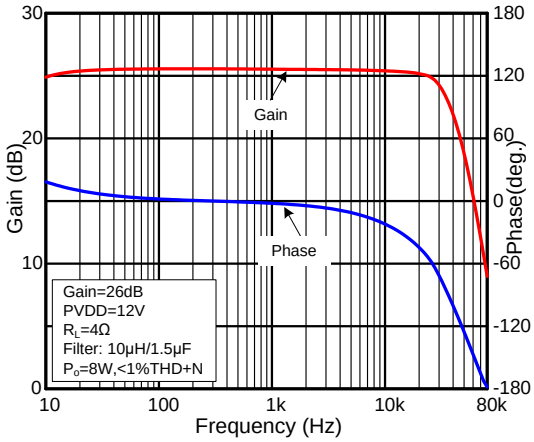
THD+N vs. Output Power



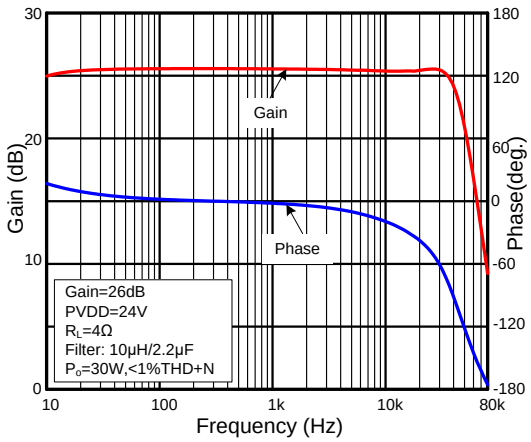
THD+N vs. Output Power



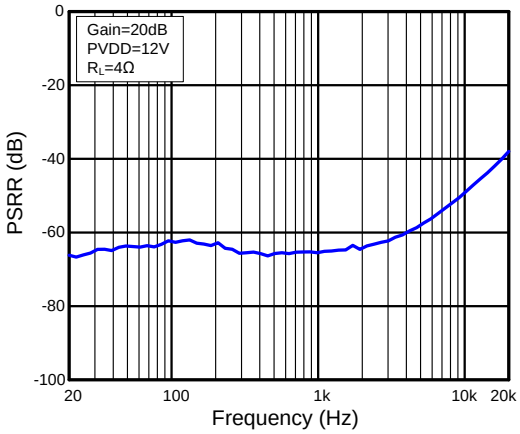
Gain/Phase vs. Frequency



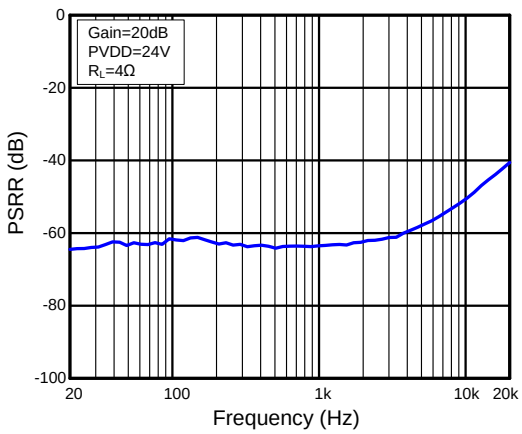
Gain/Phase vs. Frequency



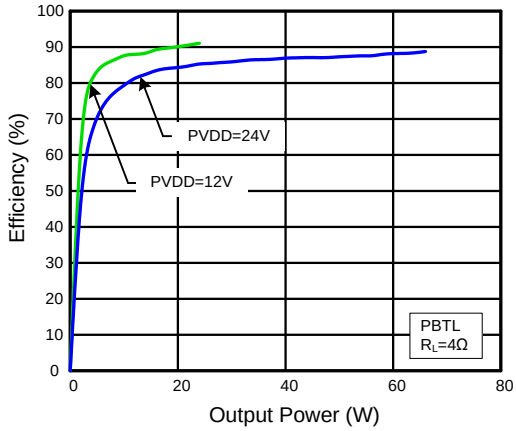
PSRR vs. Frequency



PSRR vs. Frequency



Efficiency vs. Power



Function Description

This section focuses on the description of SY6018 Class-D function block operation.

Gain & Master/Slave Mode Setting

The gain and master/slave mode of the SY6018 is set by the GAIN/SLV pin. An internal ADC is used to detect the 8 states. The first four stages set the GAIN in Master Mode in gains of 20dB, 26dB, 32dB, 36dB, while the other four stages set the GAIN in Slave Mode in gains of 20dB, 26dB, 32dB, 36dB respectively. The gain setting cannot be changed while device is powered as the setting is latched during power-up. Table 1 lists the recommended resistor and state as well as gain. Figure 3 is the typical circuit for GAIN/SLV pin. The resistor tolerance should be 5% or better.

In Master mode, SYNC terminal is an output, while in Slave mode, SYNC is an input for a clock input. TTL logic levels compliance to GREG.

Table1. Gain and Master/Slave Setting

MODE	GAIN(dB)	R1(to GREG, kΩ)	R2(to GND, kΩ)
Master	20	OPEN	5.6
Master	26	100	20
Master	32	100	39
Master	36	75	47
Slave	20	51	51
Slave	26	47	75
Slave	32	39	100
Slave	36	16	100

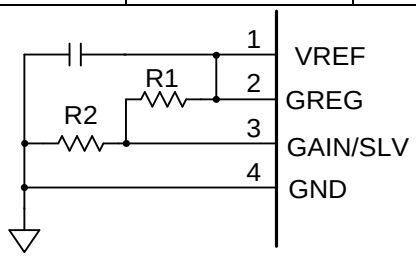


Fig.3 Gain and Master/Slave Setting Circuit

Modulation Scheme

The SY6018 has two modulation schemes: BD modulation or 1SPW modulation, which is set via the MODSEL pin.

MODSEL=LOW: BD Modulation

The SY6018 uses BD mode modulation scheme that allows operation without the classic LC reconstruction filter when the Class-D is driving an inductive load, see as Figure 4. Each output is switching from 0V to the supply voltage. The OUTP and OUTN are in phase with each other with no input so that there is little or no current in the speaker. The duty cycle of OUTP is greater than 50% and OUTN is less than 50% for positive output voltages. The duty cycle of OUTP is less than 50% and OUTN is greater than 50% for negative output voltages. The voltage across the load sits at 0V throughout most of the switching period, greatly reducing the switching current, which reduces any I^2R losses in the load.

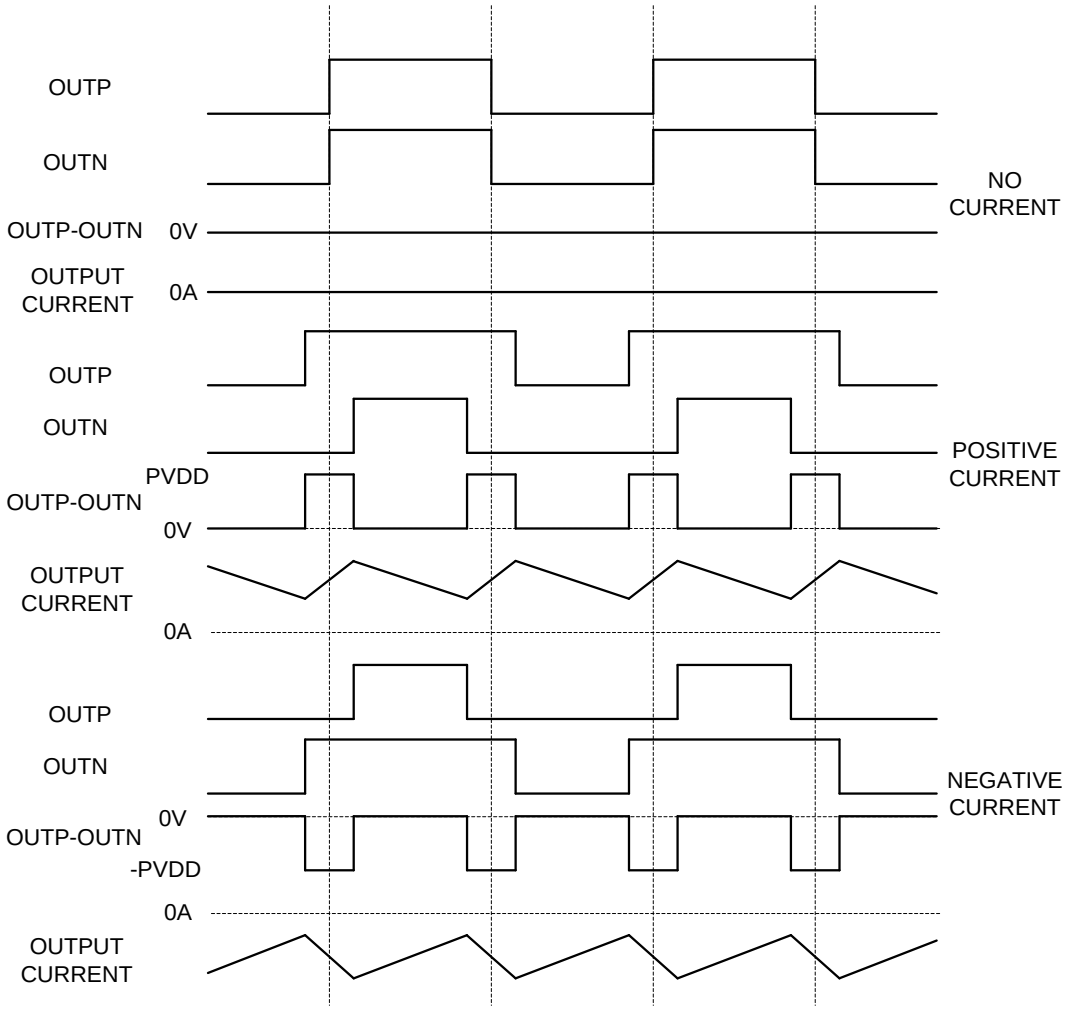


Fig.4 BD Modulation

MODSEL=HIGH: 1SPW Modulation

The 1SPW mode is different from traditional modulation scheme in order to achieve higher efficiency with a slight penalty in THD degradation and more required in the output filter. In 1SPW mode the output operates at 35% modulation when no audio input for less idle current. When a small audio signal is applied the switching is similar with BD mode ; When a large audio signal is applied , the decreasing output signal will quickly rail to GND at which point all the audio modulation takes place through the rising output. The result is that only one output is switching during a majority of the audio cycle. Efficiency is improved in this mode due to the reduction of switching losses. The THD penalty in 1SPW mode is minimized by the high performance feedback loop. The resulting audio signal at each half output has a discontinuity each time the output rails to GND. This can cause ringing in the audio reconstruction filter unless care is taken in the selection of the filter components and type of filter used.

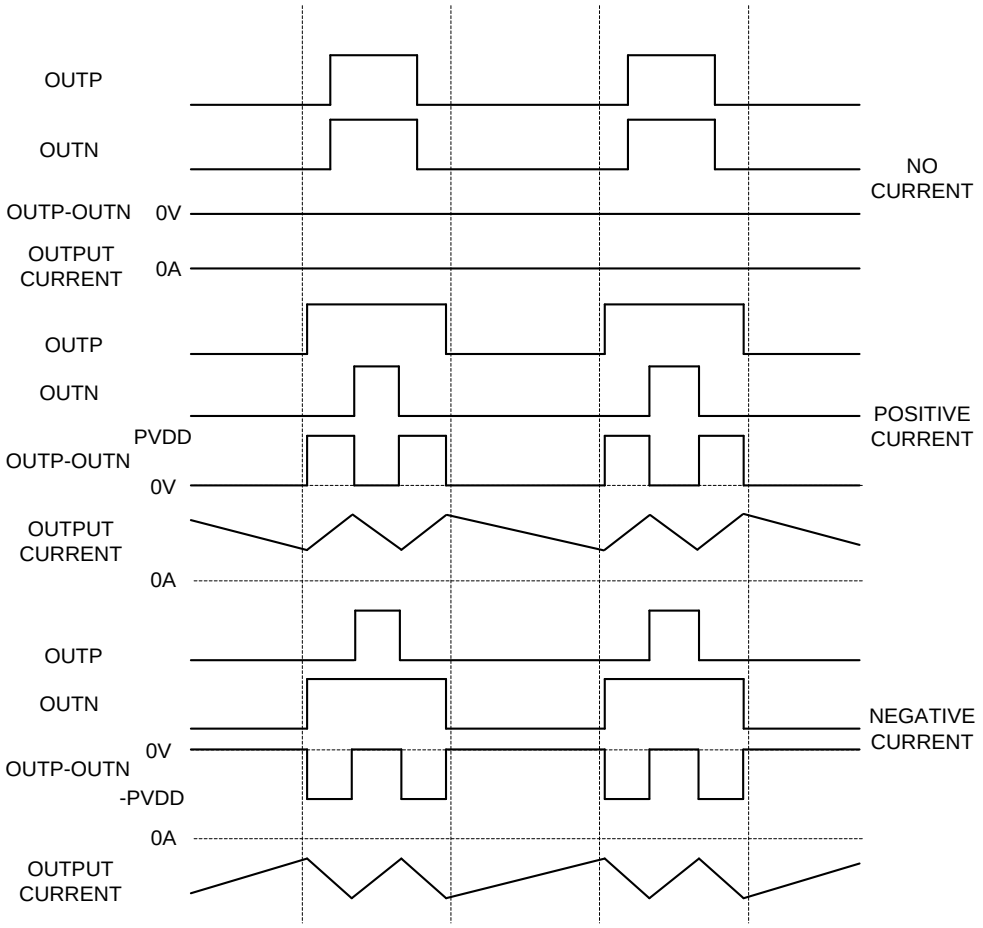


Fig.5 1SPW Modulation

Input Capacitor, C_I

In the typical application, input capacitor C_I is required to allow the amplifier to bias the input signal to the proper dc level for optimum operation. In this case C_I and the input impedance of the amplifier (Z_I) form a high-pass filter with the corner frequency determined in Equation 2.

$$f_c = \frac{1}{2\pi \cdot Z_I \cdot C_I} \qquad (2)$$

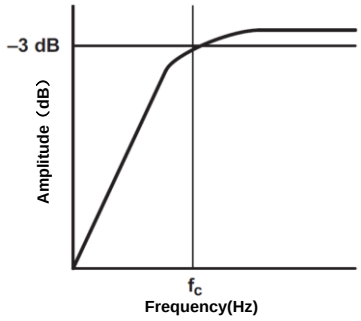


Fig.6 Amplitude vs. Frequency

The value of C_I is important, as it directly affects the bass (low-frequency) performance of the circuit. The input resistance of the SY6018 value is fixed at 15kΩ ±20%, Consider the specification calls for a flat bass response down to 20Hz. Equation 1 is reconfigured as Equation 3.

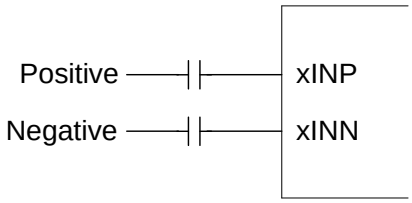
$$C_I = \frac{1}{2\pi \cdot Z_I \cdot f_c} \qquad (3)$$

In this example, C_I is 0.53μF; so, one would likely choose a value of 1μF as this value is commonly used. A further consideration for this capacitor is the leakage path from the input source through the input network, C_I, and the feedback network to the load. This leakage current creates a dc offset voltage at the input to the amplifier that reduces useful headroom, especially in high-gain applications. For this reason, a low-leakage tantalum or ceramic capacitor is the best choice. When polarized capacitors are used, the positive side of the capacitor should face the amplifier input in most applications as the dc level there is held at 1.7V, which is likely higher than the source dc level. Note that it is important to confirm the capacitor polarity in the application. Additionally, lead-free solder can create dc offset voltages, and it is important to ensure that boards are cleaned properly.

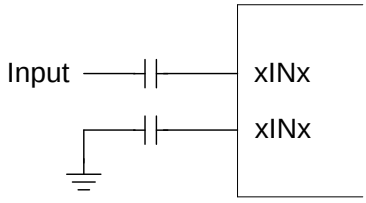
Differential Inputs

The differential input stage of the amplifier cancels any noise that appears on both input lines of the channel. To use the SY6018 with a differential source, connect the positive lead of the audio source to the INP input and the negative lead from the audio source to the INN input. To use the SY6018 with a single-ended source, ac ground the INP or INN input through a capacitor equal in value to the input capacitor on INN or INP and apply the audio source to either input. In a single-ended input application, the unused input should be ac grounded at the audio source instead of at the device input for best noise performance. For good transient performance, the impedance seen at each of the two differential inputs should be the same. The input signal connection is shown as Figure 6.

The impedance seen at the inputs should be limited to an RC time constant to allow the input dc blocking capacitors to become completely charged during the 47ms power-up time. If the input capacitors are not allowed to completely charge, there will be some additional sensitivity to component matching which can result in pop if the input components are not well matched.



(a) Differential Input



(b) Single-ended Input

Fig.7 Input Signal Connection

PBTL Select

The SY6018 offers the feature of parallel BTL operation with two outputs of each channel connected directly. Connect LINP and LINN directly to ground (without capacitors) that sets the device in PBTL(Mono) mode during power up. In the Mono mode, the positive and negative outputs of each channel (left and right) are synchronized and in phase, applying the input signal to the RIGHT input and place the speaker between the LEFT and RIGHT outputs. Connect the positive and negative output together for best efficiency.

BSN and BSP

The half H-bridge output stages use only NMOS transistors. Therefore, they require bootstrap capacitors for the high side of each output to turn on correctly. A 220nF ceramic capacitor, rated for at least 25V, must be connected from each output to its corresponding bootstrap input. Specifically, one 220nF capacitor must be connected from OUTP to BSP, and one 220nF capacitor must be connected from OUTN to BSN.

The bootstrap capacitors connected between the BSXX pins and their corresponding outputs function as a floating power supply for the high-side N-channel power MOSFET gate-drive circuitry. During each high-side switching cycle, the bootstrap capacitors hold the gate-to-source voltage high enough to keep the high-side MOSFETs turned on.

SDZ Operation

The SY6018 employs a shutdown mode of operation designed to reduce supply current to the absolute minimum level during periods of nonuse for power conservation. The SDZ input terminal should be held high (see specification table for trip point) during normal operation when the amplifier is in use. Pulling SDZ low causes the outputs to mute and the amplifier to enter a low-current state. Never leave SDZ unconnected, because amplifier operation would be unpredictable.

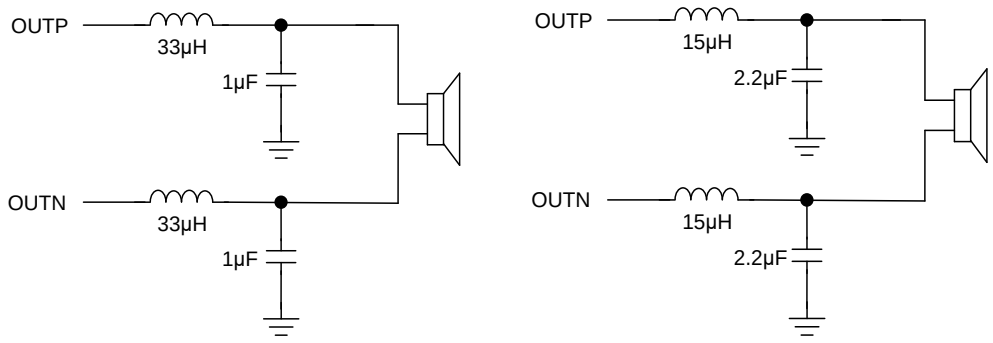
For the best power-up pop performance, place the amplifier in the shutdown or mute mode prior to applying the power supply voltage.

Efficiency: LC Filter Required With the Traditional Class-D Modulation Scheme

The main reason that the traditional Class-D amplifier needs an output filter is that the switching waveform results in maximum current flow. This causes more loss in the load, which causes lower efficiency. The ripple current is large for the traditional modulation scheme, because the ripple current is proportional to voltage multiplied by the time at that voltage. The differential voltage swing is $2\times V_{DD}$, and the time at each voltage is half the period for the traditional modulation scheme. An ideal LC filter is needed to store the ripple current from each half cycle for the next half cycle, while any resistance causes power dissipation. The speaker is both resistive and reactive, whereas an LC filter is almost purely reactive.

The SY6018 modulation scheme has little loss in the load without a filter because the pulses are short and the change in voltage is V_{DD} instead of $2\times V_{DD}$. As the output power increases, the pulses widen, making the ripple current larger. Ripple current could be filtered with an LC filter for increased efficiency, but for most applications the filter is not needed.

An LC filter with a cutoff frequency less than the Class-D switching frequency allows the switching current to flow through the filter instead of the load. The filter has less resistance but higher impedance at the switching frequency than the speaker, which results in less power dissipation, therefore increasing efficiency. Figure 7 is the typical LC filter structure.



(a) Speaker Resistor = 8Ω (b) Speaker Resistor = 4Ω

Fig.8 Typical LC Output Filter, Cutoff Frequency is 27 kHz

Ferrite Bead Filter Considerations

When SY6018 is used in low output power application it is possible to design a high efficiency Class-D audio amplifier while minimizing interference to surrounding circuits. It is also possible to accomplish this with only a low-cost ferrite bead filter. In this case it is necessary to carefully select the ferrite bead used in the filter.

One important aspect of the ferrite bead selection is the type of material used in the ferrite bead. Not all ferrite material is alike, so it is important to select a material that is effective in the 10MHz to 100MHz range which is the key to the operation of the Class-D amplifier. Many of the specifications regulating consumer electronics have emissions limits as low as 30MHz. It is important to use the ferrite bead filter to block radiation in the 30MHz and above range from appearing on the speaker wires and the power supply lines which are good antennas for these signals. The impedance of the ferrite bead can be used along with a small capacitor with a value in the range of 1nF to reduce the frequency spectrum of the signal to an acceptable level. For best performance, the resonant frequency of the ferrite bead/ capacitor filter should be less than 10MHz.

Also, it is important that the ferrite bead is large enough to maintain its impedance at the peak currents expected for the amplifier. Some ferrite bead manufacturers specify the bead impedance at a variety of current levels. In this case it is possible to make sure the ferrite bead maintains an adequate amount of impedance at the peak current the amplifier will see. If these specifications are not available, it is also possible to estimate the bead current handling capability by measuring the resonant frequency of the filter output at very low power and at maximum power. A change of resonant frequency of less than fifty percent under this condition is desirable.

A high quality ceramic capacitor is also needed for the ferrite bead filter. A low ESR capacitor with good temperature and voltage characteristics will work best.

Additional EMC improvements may be obtained by adding snubber networks from each of the class D outputs to ground. Suggested values for a simple RC series snubber network would be 10Ω in series with a 470pF capacitor although design of the snubber network is specific to every application and must be designed taking into account the parasitic reactance of the printed circuit board as well as the audio amp. Take care to evaluate the stress on the component in the snubber network especially if the amp is running at high PVDD. Also, make sure the layout of the snubber network is tight and returns directly to the PGND. The typical ferrite bead filter is shown as Figure 8.

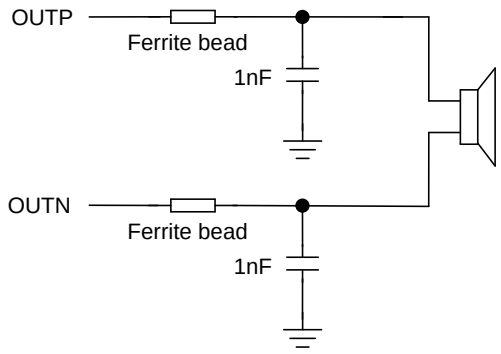


Fig.9 Typical Ferrite Bead EMI Filter

When to Use an Output Filter for EMI Suppression

There may be a few circuit instances where it is necessary to add a complete LC reconstruction filter. These circumstances might occur if there are nearby circuits which are very sensitive to noise. In these cases a classic second order Butterworth filter similar to those shown in the figures above can be used.

Some systems have little power supply decoupling from the AC line but are also subject to line conducted interference (LCI) regulations. These include systems powered by "wall warts" and "power bricks." In these cases, it LC reconstruction filters can be the lowest cost means to pass LCI tests. Common mode chokes using low frequency ferrite material can also be effective at preventing line conducted interference.

AM Avoidance EMI Reduction

To reduce interference in the AM radio band, the SY6018 has the ability to change the switching frequency via AM<2:0> pins. The recommended frequencies are listed in Table 2. The fundamental frequency and its second harmonic straddle the AM radio band listed. This eliminates the tones that can be present due to the switching frequency being demodulated by the AM radio.

Table2. AM Frequencies Setting

US AM FREQUENCY(kHz)	EUROPEAN AM FREQUENCY(kHz)	SWITCHING FREQUENCY(kHz)	AM2	AM1	AM0
	522-540				
540-917	540-914	500	0	0	1
917-1125	914-1122	600/400	0	1	0
			0	0	0
1125-1375	1122-1373	500	0	0	1
1375-1547	1373-1548	600/400	0	1	0
			0	0	0
1547-1700	1548-1701	600/500	0	1	0
			0	0	1

Protection Circuits

The device is fully protected against short circuit, over temperature, DC error, over voltage and under voltage. The FAULTZ pin will signal if an error is detected according Table 3.

Table3. Fault Reporting

FAULT	TRIGGERING CONDITION	FAULTZ STATE	ACTION	LATCHED/SELF-CLEARING
Short Circuit	Output short or short to PVDD or PGND	Low	Output high impedance	Latched
Over Temperature	T_J>150℃	Low	Output high impedance	Latched
Too High DC Offset	DC output voltage	Low	Output high impedance	Latched
Under Voltage for PVDD	PVDD<5.2V	-	Output high impedance	Self-clearing
Over Voltage for PVDD	PVDD>31V	-	Output high impedance	Self-clearing

DC Error Protection (DCP)

The SY6018 has circuitry which will protect the speakers from DC current which might occur due to defective capacitors on the input or shorts on the printed circuit board at the inputs. A DC error fault will be reported on the FAULTZ pin as a low state. The DC error fault will also cause the amplifier to shut down by changing the state of the outputs to Hi-Z.

If automatic recovery from the short circuit protection latch is desired, connect the FAULTZ pin directly to the SDZ pin. This allows the FAULTZ pin function to automatically drive the SDZ pin low which clears the DC error protection latch.

A DC error fault is issued when the output differential duty-cycle of either channel exceeds 20% for more than 840ms at the same polarity. Table 4 below shows some examples of the typical DC error protection threshold for several values of the supply voltage. This feature protects the speaker from large DC currents or AC currents less than 1Hz. To avoid nuisance faults due to the DC error circuit, hold the SDZ pin low at power up until the signals at the inputs are stable. Also, take care to match the impedance seen at the positive and negative inputs to avoid nuisance DC error faults.

Table4. DC Error Threshold

PVDD(V)	OUTPUT OFFSET VOLTAGE(V)
12	2.6
14	3.0
16	3.6
18	3.9

Short Circuit Protection (SCP)

The SY6018 has short circuit protection against load is shorted or exceeded. The short circuit protection fault is reported on the FAULTZ pin as a low state. The amplifier outputs are switched to a Hi-Z state when the short circuit protection latch is engaged. The latch can be cleared by cycling the SDZ pin through the low state.

If automatic recovery from the short circuit protection latch is desired, connect the FAULTZ pin directly to the SDZ pin. This allows the FAULTZ pin function to automatically drive the SDZ pin low which clears the short-circuit protection latch.

Under Voltage Lockout (UVLO) and Over Voltage Lockout (OVLO)

If at any time the voltage on the PVDD pin falls below the under voltage or rises above over voltage lockout threshold voltage, all circuitry in the device is disabled and internal logic is reset. Operation resumes when PVDD rises above the UVLO threshold with hysteresis or falls below OVLO threshold with hysteresis.

Over Temperature Protection (OTP)

Thermal protection on the SY6018 prevents damage to the device when the internal die temperature exceeds 150°C. There is a ±15°C tolerance on this trip point from device to device. Once the die temperature exceeds the thermal set point, the device enters into the shutdown state and the outputs are disabled. This is a latched fault.

Thermal protection faults are reported on the FAULTZ terminal as a low state.

If automatic recovery from the thermal protection latch is desired, connect the FAULTZ pin directly to the SDZ pin. This allows the FAULTZ pin function to automatically drive the SDZ pin low which clears the thermal protection latch.

Power Supply Recommendations

The power supply requirements for the SY6018 consist of one higher-voltage supply to power the output stage of the speaker amplifier. Several on-chip regulators are included on the SY6018 to generate the voltages necessary for the internal circuitry of the audio path. It is important to note that the voltage regulators which have been integrated are sized only to provide the current necessary to power the internal circuitry. The external pins are provided only as a connection point for off-chip bypass capacitors to filter the supply. Connecting external circuitry to these regulator outputs may result in reduced performance and damage to the device. The high voltage supply, between 5.6V and 26 V, supplies the analog circuitry (AVDD) and the power stage (PVDD). The AVDD supply feeds the internal LDO.

The SY6018 is a high-performance CMOS audio amplifier that requires adequate power-supply decoupling to ensure that the output total harmonic distortion (THD) is as low as possible. Power-supply decoupling also prevents oscillations for long lead lengths between the amplifier and the speaker. The optimum decoupling is achieved by using two capacitors of different types that target different types of noise on the power-supply leads. For higher-frequency transients, spikes, or digital hash on the line, a good low equivalent-series-resistance (ESR) ceramic capacitor, typically 0.1μF to 1μF, placed as close as possible to the device V_{DD} lead works best. For filtering lower frequency noise signals, a larger aluminum electrolytic capacitor of 220μF or greater placed near the audio power amplifier is recommended. The 220μF capacitor also serves as local storage capacitor for supplying current during large signal transients on the amplifier outputs. The PVDD terminals provide the power to the output transistors, so a 220μF or larger capacitor should be placed on each PVDD terminal. A 10μF capacitor on the AVDD terminal is adequate. These capacitors must be properly checked for voltage and ripple-current rating to ensure reliability.

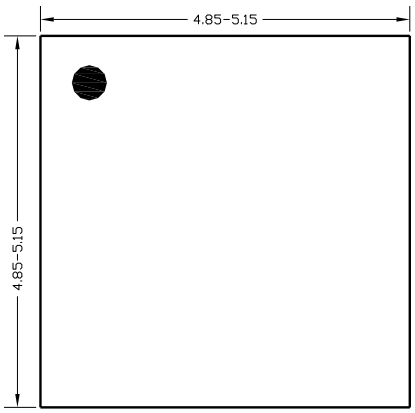
Printed Circuit Board (PCB) Layout

The SY6018 can be used with a small, inexpensive ferrite bead output filter for most applications. However, since the Class-D switching edges are fast, it is necessary to take care when planning the layout of the printed circuit board. The following suggestions will help to meet EMC requirements.

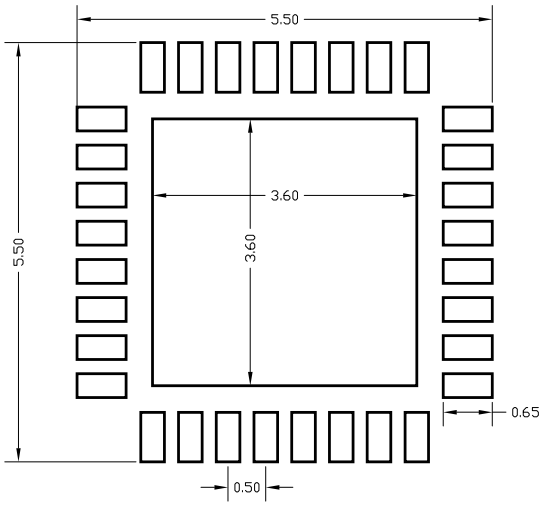
- Decoupling capacitors—The high-frequency decoupling capacitors should be placed as close to the PVDD and AVDD terminals as possible. Large (220μF or greater) bulk power supply decoupling capacitors should be placed near the SY6018 on the PVDD supplies. Local, high-frequency bypass capacitors should be placed as close to the PVDD pins as possible. These capacitors can be connected to the IC ground pad directly for an excellent ground connection. Consider adding a small, good quality low ESR ceramic capacitor between 220pF and 1000pF and a larger mid-frequency cap of value between 0.1μF and 1μF also of good quality to the PVDD connections at each end of the chip.

- Keep the current loop from each of the outputs through the ferrite bead and the small filter cap and back to PGND as small and tight as possible. The size of this current loop determines its effectiveness as an antenna.
- Grounding—The AVDD decoupling capacitor should be grounded to analog ground (AGND). The PVDD decoupling capacitors should connect to PGND. Analog ground and power ground should be connected at the thermal pad, which should be used as a central ground connection or star ground for the SY6018.
- Output filter—The ferrite EMI filter should be placed as close to the output terminals as possible for the best EMI performance. The LC filter should be placed close to the outputs. The capacitors used in both the ferrite and LC filters should be grounded to power ground.
- Thermal pad—The thermal pad must be soldered to the PCB for proper thermal performance and optimal reliability. The dimensions of the thermal pad and thermal land should be as large as possible. Solid vias should be equally spaced underneath the thermal land. The vias should connect to a solid copper plane, either on an internal layer or on the bottom layer of the PCB.

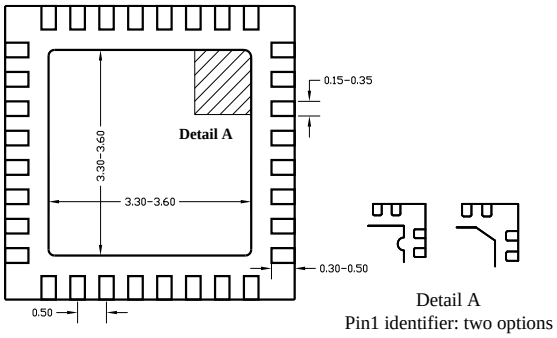
QFN5×5-32 Package Outline & PCB Layout



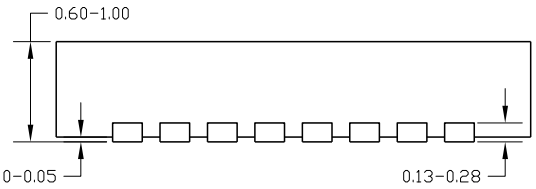
Top View



PCB layout (Recommended)



Bottom View

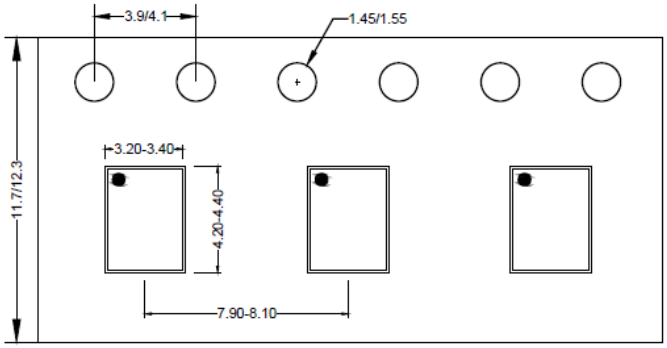


Side View

Notes: **All dimension in millimeter and exclude mold flash & metal burr**

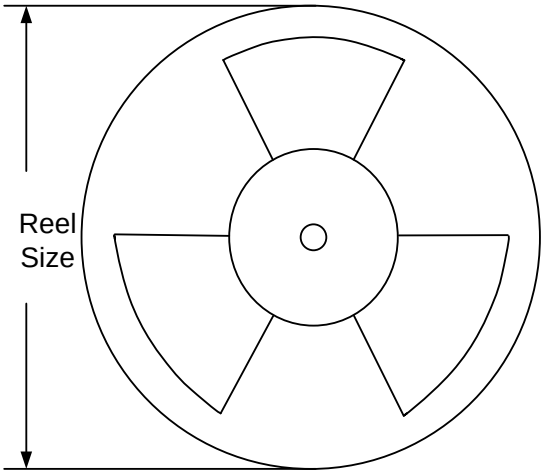
Taping & Reel Specification

1. QFN5×5 taping orientation



Feeding direction ⟶

2. Carrier Tape & Reel specification for packages



Package types	Tape width (mm)	Pocket pitch(mm)	Reel size (Inch)	Trailer length(mm)	Leader length (mm)	Qty per reel
QFN5x5	12	8	13"	400	400	5000

3. Others: NA

Revision History

The revision history provided is for informational purpose only and is believed to be accurate, however, not warranted. Please make sure that you have the latest revision.

Date	Revision	Change
Apr.25, 2023	Revision 1.0	Production Release
Apr.25, 2022	Revision 0.9D	1. modify the MUTE PIN description as: Mute pin (High=mute, Low=unmute), TTL logic levels with compliance to AVDD. 2. modify the SDZ PIN description as: Shutdown pin (low = enter shutdown, high = exit shutdown). TTL logic levels with compliance to AVDD.
Mar.11, 2021	Revision 0.9C	Change the pin1 from PLIMIT to VREF and delete the description of PLIMIT.
May28,2018	Revision 0.9B	To meet customer's request, We add the 1%THD+N and 10% THD+N Maximum Power vs. Voltage supply with 8Ω Load in P8； add the 1%THD+N and 10% THD+N Maximum Power vs. Voltage supply with 4Ω Load in P12.
Sept. 26, 2017	Revision 0.9A	1.Change ""AVDD, PVDD"" min value from 6V to 5.6V, 2.Change""VDD Under Voltage Lockout Voltage VUVLO_RISE"" max value from 5.6V to 5.8V, delete ""VUVLO_FALL"" max value."
Sept. 13, 2017	Revision 0.9	Initial Release

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