SQ24902

IEEE 802.3bt PD Interface Controller

General Description

The SQ24902 is an IEEE 802.3af/at/bt-compliant powered device (PD) interface controller. The $\overline{T2P}$ output indicates the number of classification events received during IEEE 802.3bt-compliant mutual identification and negotiation of available power.

The SQ24902 utilizes an external, low R_{DS}(ON) N-channel hot swap MOSFET to extend the end-to-end power delivery efficiency and eliminate costly heat sinks. The SQ24902 also includes a power good output, onboard signature resistor, under voltage lockout, and thermal protection. Start-up inrush current is adjustable with an external capacitor. Auxiliary power override is supported as low as 9V with the AUX pin.

The SQ24902 can be configured to support all possible 802.3bt, 802.3at and 802.3af power levels with external component changes.

Features

- IEEE 802.3af/at/bt Powered Device (PD) Controller
- Supports Up to 71.3W PDs
- 5-event Classification Sensing
- Superior Surge Protection (100V Absolute Maximum)
- Wide Junction Temperature Range (–40℃ to 125℃)
- Over Temperature Protection
- Integrated Signature Resistor
- External Hot Swap N-Channel MOSFET for Lowest Power Dissipation and Highest System Efficiency
- Configurable Aux Power Support as Low as 9V
- RoHS Compliant and Halogen Free
- Available in 10-Lead MSOP Package

Applications

- High Power Wireless Data Systems
- Outdoor Security Camera Equipment
- Commercial and Public Information Displays
- High Temperature Industrial Applications

Ordering Information

Ordering Number	Package type	Note
SQ24902FBC	MSOP10	----

Typical Application

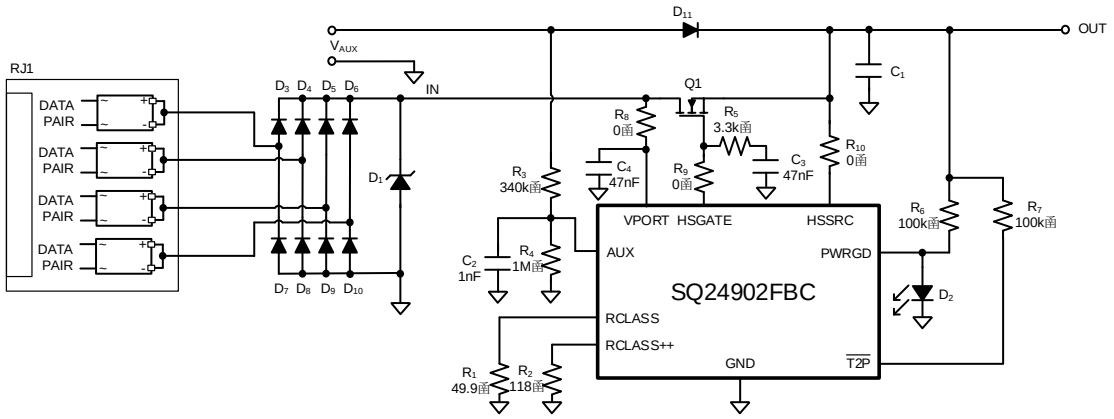
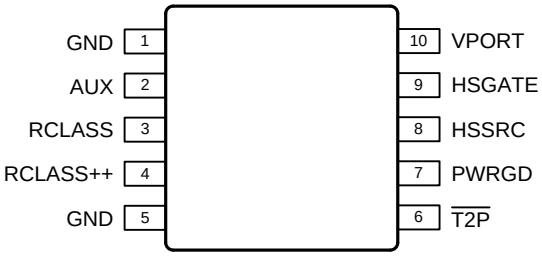


Figure1. Schematic Diagram

©2025 Silergy Corp. All Rights Reserved.

Pinout (top view)



(MSOP10)

Top Mark: **CXW*xyz*** **(**Device code: CXW; ***x=year code, y=week code, z= lot number code*****)**

Pin Name	NO.	TYPE	Pin Description
GND	1,5	-	Device ground.
AUX	2	I	Auxiliary sense. A resistive divider from the auxiliary power input to AUX sets the voltage at which the auxiliary supply takes over. In auxiliary power operation, HSGATE pulls down, the signature resistor disconnects, classification is disabled, the PWRGD pin is high impedance and $\overline{T2P}$ indicates max available power. Connect to GND when not used.
RCLASS	3	O	Configurable PoE classification resistor.
RCLASS++	4	O	Configurable PoE classification resistor.
$\overline{T2P}$	6	O	PSE type indicator; Open-drain output.
PWRGD	7	O	Power good indicator; Open-drain output. Pull to GND during V_{CLASS} and inrush.
HSSRC	8	I	External Hot Swap MOSFET source. Connect to source of the external MOSFET.
HSGATE	9	O	External Hot Swap MOSFET gate control output. Connect to gate of the external MOSFET.
VPORT	10	I	PD interface upper power rail and external Hot Swap MOSFET drain connection.

© 2025 Silergy Corp. All Rights Reserved.

Block Diagram

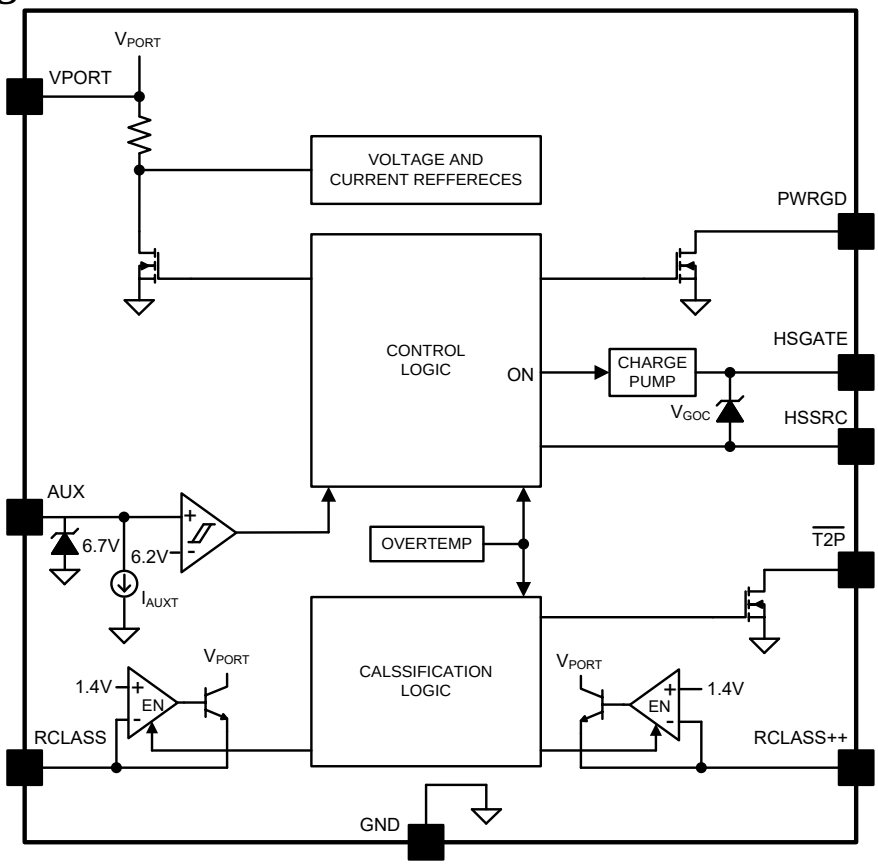


Figure2. Block Diagram

Absolute Maximum Ratings (Note 1, 4)

VPORT, HSSRC Voltage---------- –0.3V to 100V
HSGATE to HSSRC Voltage----------V_{HSSRC}-0.2V to V_{HSSRC} +14V
HSGATE Current---------- ±20mA
RCLASS, RCLASS++ Voltage---------- -0.3V to 6V (and ≤ VPORT)
AUX Current---------- ±1.4mA
$\overline{T2P}$, PWRGD Voltage---------- –0.3V to 100V
$\overline{T2P}$, PWRGD Current---------- 5mA
Power Dissipation, P_D @ T_A = 25°C---------- 0.74W
Package Thermal Resistance (Note 2)
θ_{JA} ---------- 135.2°C/W
θ_{JC} ---------- 25°C/W
Operating Junction Temperature Range ---------- –40°C to 125°C
Storage Temperature Range---------- –65°C to 150°C
Lead Temperature (Soldering, 10 sec.) ----------300°C

Recommended Operating Conditions (Note 5)

VPORT, HSSRC Voltage---------- 0V to 60V
HSGATE to HSSRC Voltage----------V_{HSSRC} to V_{HSSRC} +14V
RCLASS, RCLASS++ Voltage---------- 0V to 5V (and ≤ VPORT)
Ambient Temperature Range ---------- -40°C to 125°C

© 2025 Silergy Corp. All Rights Reserved.

Electrical Characteristics

Unless otherwise noted: –40℃≤ T_J ≤125℃. (Note 4)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
VPORT Operating Input Voltage		At VPORT pin			60	V
VPORT Signature Range	V_{SIG}	At VPORT pin	1.5		10	V
VPORT Classification Range	V_{CLASS}	At VPORT pin	12.5		21	V
VPORT Mark Range	V_{MARK}	At VPORT pin, preceded by V_{CLASS}	5.6		10	V
VPORT Aux Mode Range		At VPORT pin, AUX > V_{AUXT}	8		60	V
Signature/Class Hysteresis Window			1.0			V
Reset Threshold	V_{RESET}	At VPORT pin, preceded by V_{CLASS}	2.6		5.6	V
Power Good Threshold	V_{PG_TH}		7.1	8	8.9	V
Hot Swap Turn-on Voltage	V_{HSON}			35	37	V
Hot Swap Turn-off Voltage	V_{HSOFF}		30	31		V
Hot Swap On/Off Hysteresis Window			3			V
Supply Current						
Supply Current		V_{VPORT}=V_{HSSRC}=57V			1	mA
Supply Current During Classification		V_{VPORT} = 17.5 V, RCLASS and RCLASS++ open	0.1	0.2	0.5	mA
Supply Current During Mark Event		V_{VPORT}=V_{MARK} after 1st classification event	0.5		1.8	mA
Detection and Classification Signature						
Detection Signature Resistance		V_{SIG} (Note 3)	23.7	24.4	25.2	kΩ
Resistance During Mark Event		V_{MARK} (Note 3)	5.8	8.3	11	kΩ
RCLASS/RCLASS++ Operating Voltage		–10mA ≥ I_{RCLASS} ≥ –36mA, V_{CLASS}	1.32	1.40	1.43	V
Classification Signature Stability Time		V_{VPORT} Step to 17.5V, 34.8Ω from RCLASS or RCLASS++ to GND			2	ms
Analog/Digital Interface						
AUX Threshold	V_{AUXT}		6	6.2	6.4	V
AUX Hysteresis	$V_{AUX,HYS}$			0.4		V
AUX Pin Hysteresis Current	I_{AUXT}	V_{AUX} = 6.1V	0.8	2.1	4	μA
$\overline{T2P}$ Output Low		1mA Load			0.8	V
PWRGD Output Low		1mA Load			0.8	V
PWRGD Leakage Current		V_{PWRGD} = 60V			5	μA
$\overline{T2P}$ Leakage Current		$\overline{T2P}$ = 60V			5	μA
Hot Swap Control						
HSGATE Pull-up Current	I_{GPU}	V_{HSGATE} - V_{HSSRC} = 5V (Note 7)	-27	-22	-18	μA
HSGATE Open Circuit Voltage	V_{GOC}	-10μA Load, with Respect to HSSRC	10		17	V
HSGATE Pull-down Current		V_{HSGATE} - V_{HSSRC} = 5V	200			μA
Timing						
$\overline{T2P}$ Frequency	f_{T2P}	After PWRGD valid, if IEEE802.3bt PSE is mutually identified	690	840	990	Hz

© 2025 Silergy Corp. All Rights Reserved.

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
$\overline{T2P}$ Duty Cycle in PoE Operation (Note 6)		After 4-event Classification		50		%
		After 5-event Classification (RCLASS++ has resistor to GND) at T_A = 25°C.		25		%
$\overline{T2P}$ Duty Cycle in Auxiliary Supply Operation (Note 6)		V_{AUX} > V_{AUXT}, and RCLASS++ has resistor to GND at T_A = 25°C.		25		%

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: θ_{JA} is measured in the natural convection at T_A = 25°C on Silergy EVB test board of JEDEC 51-3 thermal measurement standard.

Note 3: Signature resistance specifications do not include resistance added by the external diode bridge which can add as much as 1.1k to the port resistance.

Note 4: All voltages with respect to GND unless otherwise noted. Positive currents are into pins; negative currents are out of pins unless otherwise noted.

Note 5: This IC includes over temperature protection that is intended to protect the device during momentary overload conditions. Junction temperature will exceed 150°C when over temperature protection is active. Continuous operation above the specified maximum operating junction temperature may impair device reliability.

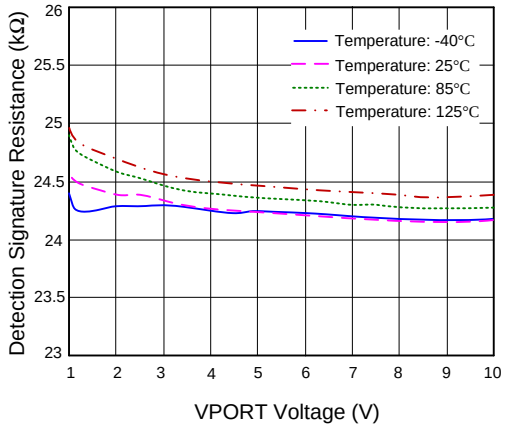
Note 6: Specified as the percentage of the period which $\overline{T2P}$ is low impedance with respect to GND.

Note 7: I_{GPU} available in PoE powered operation. That is, available after V_{VPORT} > V_{HSON} and V_{AUX} < $V_{AUXT,}$ over the range where V_{VPORT} is between V_{HSOFF} and 60V.

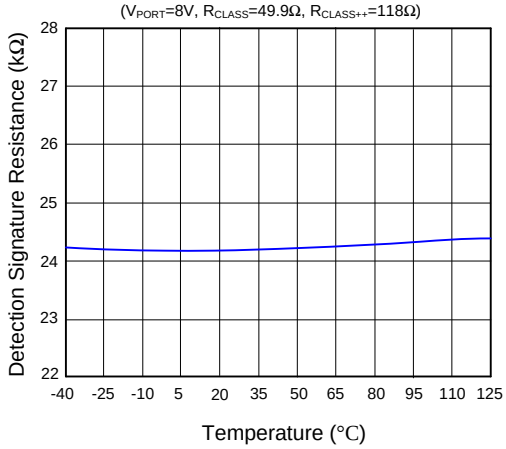
© 2025 Silergy Corp. All Rights Reserved.

Typical Performance Characteristics

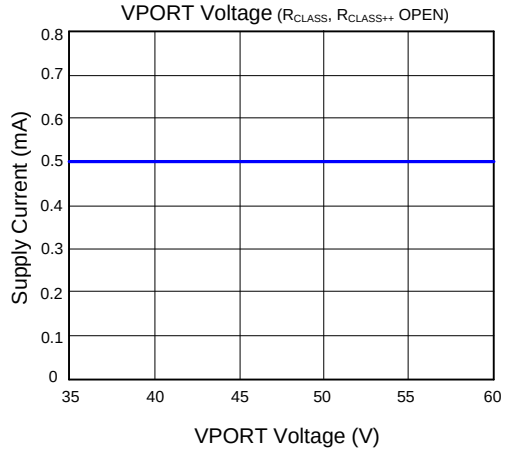
Detection Signature Resistance vs. VPORT Voltage



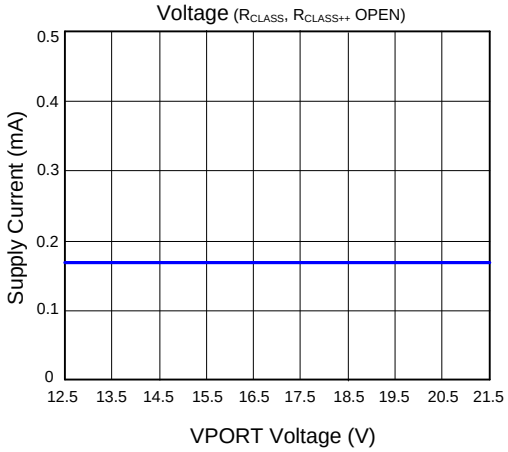
Detection Signature Resistance vs. Temperature
(V_{PORT}=8V, R_{CLASS}=49.9Ω, $R_{CLASS++}$=118Ω)



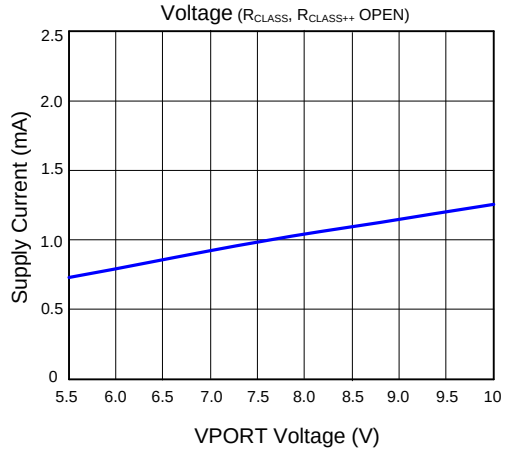
Supply Current during PWRFET Turn on vs. VPORT Voltage (R_{CLASS}, $R_{CLASS++}$ OPEN)



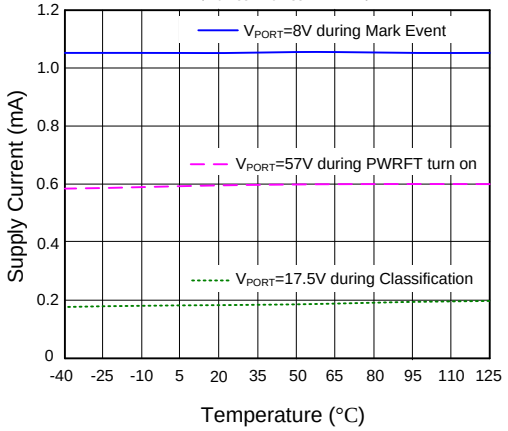
Supply Current during Classification vs. VPORT Voltage (R_{CLASS}, $R_{CLASS++}$ OPEN)



Supply Current during Mark Event vs. VPORT Voltage (R_{CLASS}, $R_{CLASS++}$ OPEN)

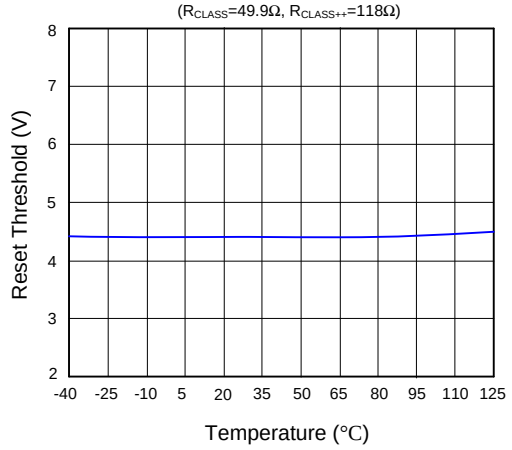


Supply Current vs. Temperature
(R_{CLASS}, $R_{CLASS++}$ OPEN)

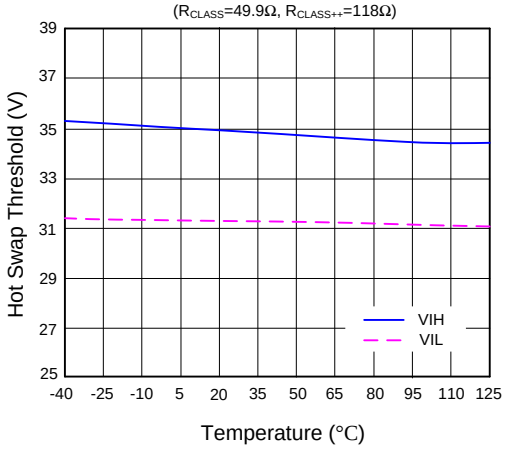


© 2025 Silergy Corp. All Rights Reserved.

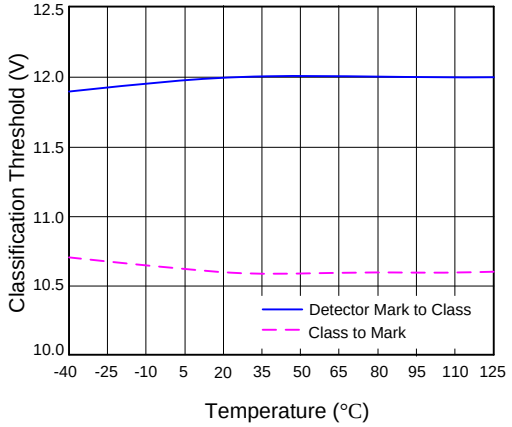
Reset Threshold vs. Temperature
(R_{CLASS}=49.9Ω, $R_{CLASS++}$=118Ω)



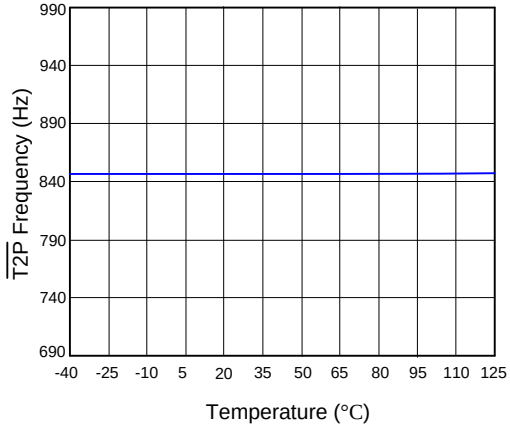
Hot Swap Threshold vs. Temperature
(R_{CLASS}=49.9Ω, $R_{CLASS++}$=118Ω)



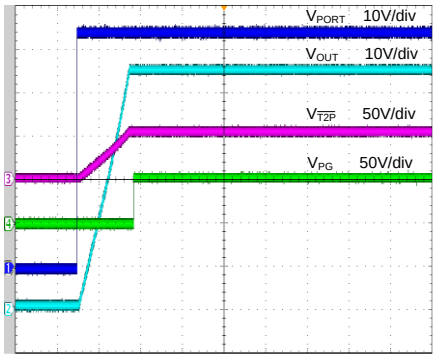
Classification Threshold vs. Temperature
(R_{CLASS}=49.9Ω, $R_{CLASS++}$=118Ω)



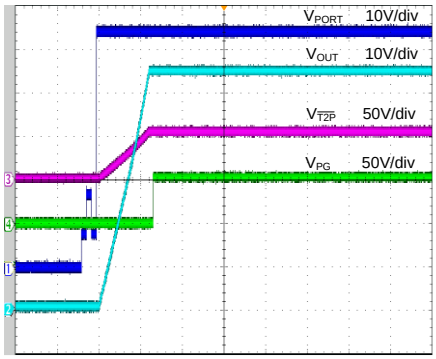
$\overline{T2P}$ Frequency vs. Temperature



Event 0 Operation Test
(V_{PORT}=0→54V, V_{AUX}=0V, R_{CLASS}=49.9Ω, $R_{CLASS++}$=118Ω)



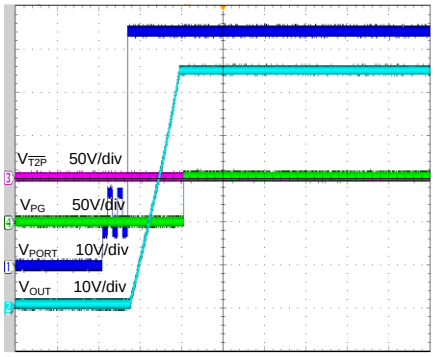
Event 1 Operation Test
(V_{PORT}=0→8V→17.5V→8V→54V, V_{AUX}=0V, R_{CLASS}=49.9Ω, $R_{CLASS++}$=118Ω)



© 2025 Silergy Corp. All Rights Reserved.

Event 2 Operation Test

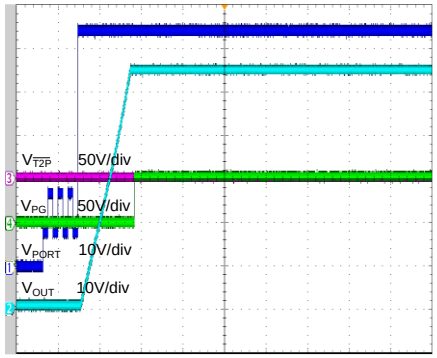
(V_{PORT}=0→8V→(17.5V→8V)$_2$→54V, V_{AUX}=0V, R_{CLASS}=49.9Ω, $R_{CLASS++}$=118Ω)



Time (100ms/div)

Event 3 Operation Test

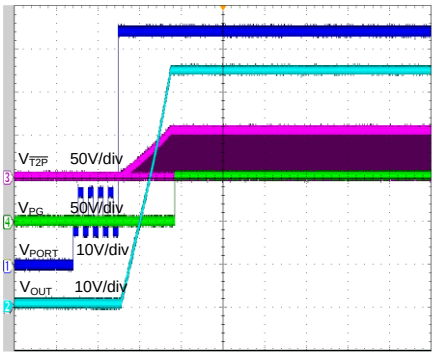
(V_{PORT}=0→8V→(17.5V→8V)$_3$→54V, V_{AUX}=0V, R_{CLASS}=49.9Ω, $R_{CLASS++}$=118Ω)



Time (100ms/div)

Event 4 Operation Test

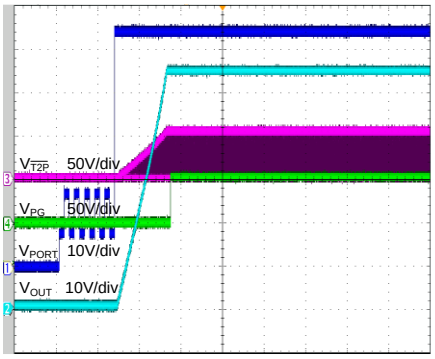
(V_{PORT}=0→8V→(17.5V→8V)$_4$→54V, V_{AUX}=0V, R_{CLASS}=49.9Ω, $R_{CLASS++}$=118Ω)



Time (100ms/div)

Event 5 Operation Test

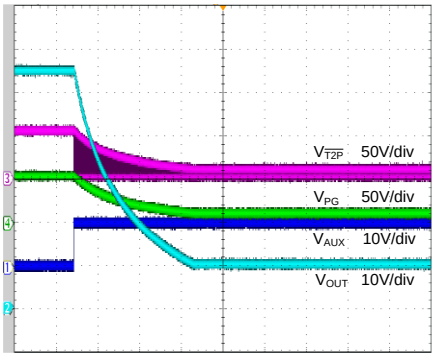
(V_{PORT}=0→8V→(17.5V→8V)$_5$→54V, V_{AUX}=0V, R_{CLASS}=49.9Ω, $R_{CLASS++}$=118Ω)



Time (100ms/div)

AUX ON

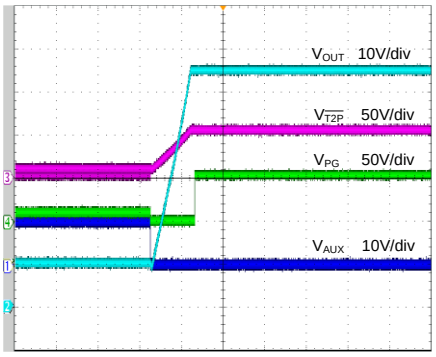
(V_{PORT}=54V, V_{AUX}=0→10V, R_{CLASS}=49.9Ω, $R_{CLASS++}$=118Ω)



Time (100ms/div)

AUX OFF

(V_{PORT}=54V, V_{AUX}=10→0V, R_{CLASS}=49.9Ω, $R_{CLASS++}$=118Ω)



Time (100ms/div)

© 2025 Silergy Corp. All Rights Reserved.

Applications Information

✧ OVERVIEW

Power over Ethernet (PoE) continues to gain popularity as products take advantage of DC power and high speed data available from a single RJ45 connector. Powered device (PD) equipment vendors are running into the 25.5W power limit established by the IEEE 802.3at standard.

The SQ24902 is an IEEE 802.3bt-compliant PD interface controller, and allows up to 71.3W operation while maintaining backwards compatibility with existing PSE systems. The $\overline{T2P}$ output indicates the number of classification events received during IEEE 802.3bt-compliant mutual identification and negotiation of available power. The SQ24902 controls a low $R_{DS(ON)}$ N-channel MOSFET to maximize efficiency and delivered power.

✧ MODES OF OPERATION

Detection Signature

During detection, the PSE looks for a 25k signature resistor which identifies the device as a PD. The PSE will apply two voltages in the range of 2.7V to 10V and measure the corresponding currents. Figure 3 shows the detection voltages. The PSE calculates the signature resistance using a $\Delta V/\Delta I$ measurement technique.

The SQ24902 presents its precision, temperature-compensated 24.4k resistor between the VPORT and GND pins, allowing the PSE to recognize a PD is present and requesting power to be applied. The SQ24902 signature resistor is smaller than 25k to compensate for the additional series resistance introduced by the IEEE required rectifier bridge.

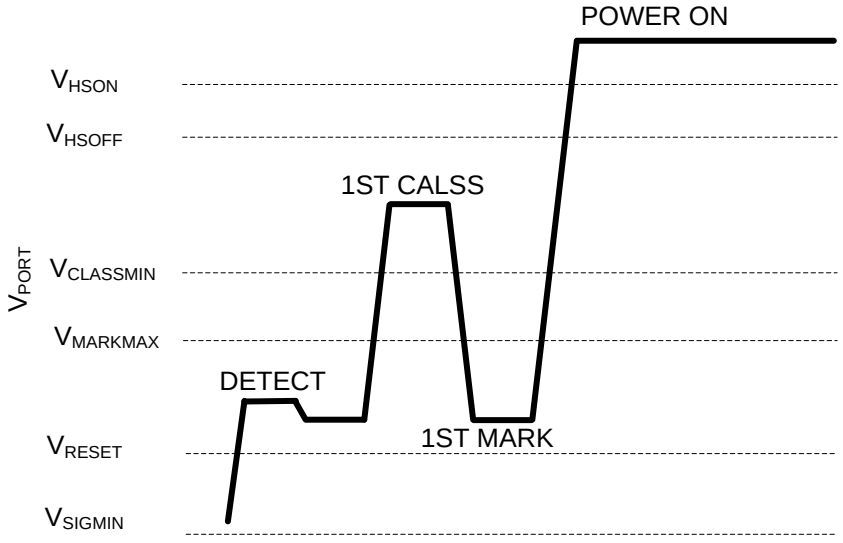


Figure3. Type 1 PSE, 1-Event Class Sequence

IEEE 802.3bt Single-Signature vs Dual-Signature PDs

IEEE 802.3bt defines two PD topologies: single-signature and dual-signature. The SQ24902 primarily targets single-signature PD topologies, eliminating the need for a second PD controller. All PD descriptions and IEEE 802.3 standard references in this data sheet are limited in scope to single-signature PDs.

Classification Signature and Mark

The classification/mark process varies depending on the PSE type. A PSE, after a successful detection, may apply a classification probe voltage of 14.5V to 20.5V and measure the PD classification signature current. Once the PSE applies a classification probe voltage, the PSE returns the PD voltage to the mark voltage range before applying another classification probe voltage, or powering up the PD.

An example of 1-Event classification is shown in Figure 3. In 2-Event classification, a PSE probes for power

© 2025 Silergy Corp. All Rights Reserved.

classification twice as shown in Figure 4. An IEEE 802.3bt PSE may apply as many as 5 events before powering up the PD.

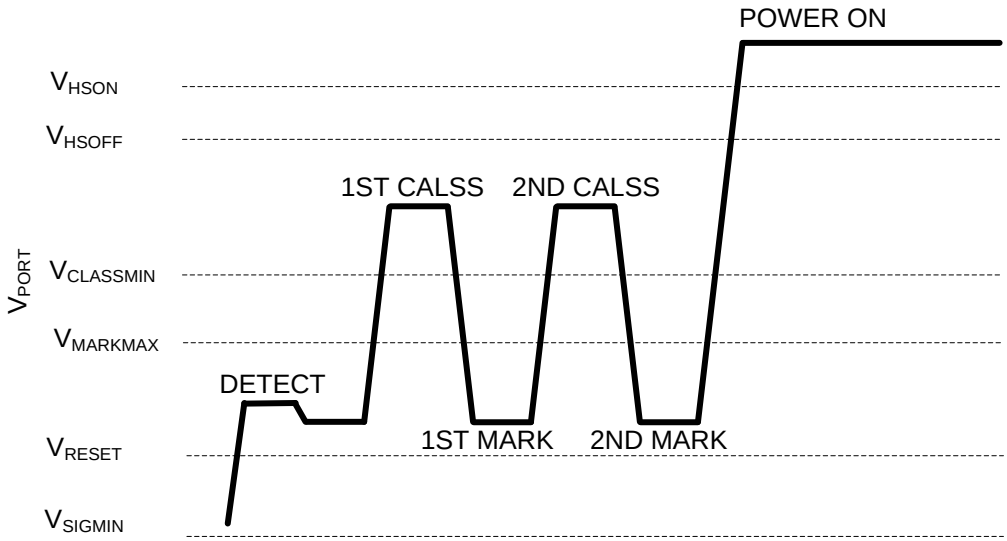


Figure 4. Type 2 PSE, 2-Event Class Sequence

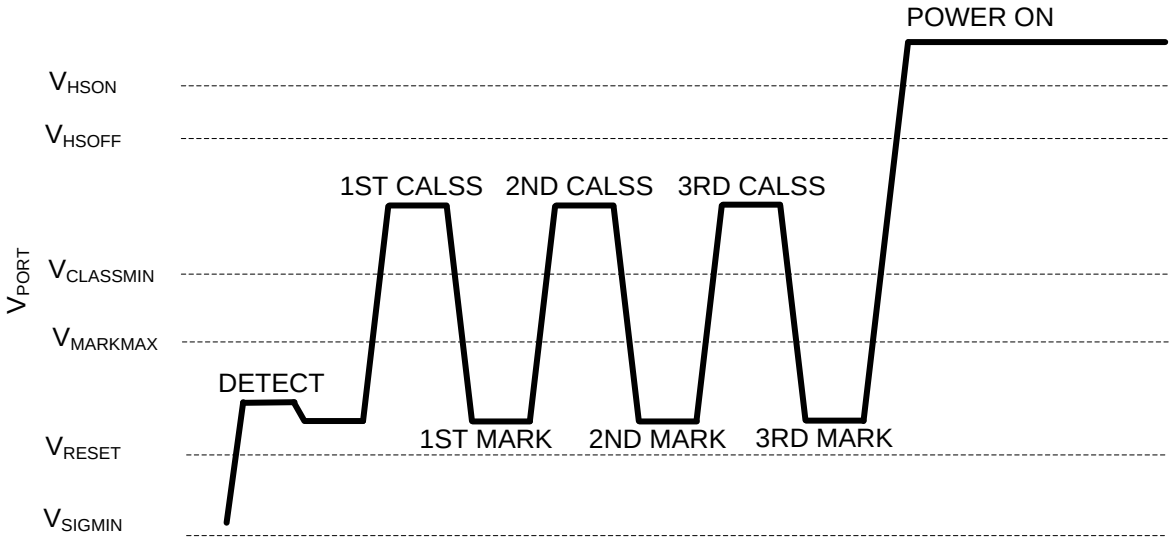


Figure 5. Type 3 or 4 PSE, 3-Event Class Sequence

IEEE 802.3bt Physical Classification and Demotion

IEEE 802.3bt defines physical classification to allow a PD to request a power allocation from the connected PSE and to allow the PSE to inform the PD of the PSE's available power. Demotion is provided if the PD requested power level is not available at the PSE. If demoted, the PD must operate in a lower power state.

The number of class/mark events issued by the PSE directly indicates the power allocated to the PD and is summarized in Table 1.

IEEE 802.3bt provides nine PD classes and four PD types, as shown in Table 2. The SQ24902 class is configured by setting the R_{CLS} and R_{CLS++} resistor values.

© 2025 Silergy Corp. All Rights Reserved.

Table1. PSE Allocated Class Power

PD REQUESTED CLASS	NUMBER OF PSE CLASS/MARK EVENTS				
	1	2	3	4	5
0	13W				
1	3.84W				
2	6.49W				
3	13W				
4	**13W**	25.5W			
5	**13W**	**25.5W**		40W	
6	**13W**	**25.5W**		51W	
7	**13W**	**25.5W**		**51W**	62W
8	**13W**	**25.5W**		**51W**	71.3W

Note: Bold indicates the PD has been demoted.

Table2. Single-Signature Classification Codes, Power Levels and Resistor Selection

PD REQUESTED CLASS	PD POWER AVAILABLE	PD TYPES	NOMINAL CLASS CURRENT	RESISTOR(1%)	
				R_{CLS}	R_{CLS++}
0	13W	Type 1	2.5mA	1.00kΩ	Open
1	3.84W	Type 1 or 3	10.5mA	140Ω	Open
2	6.49W	Type 1 or 3	18.5mA	76.8Ω	Open
3	13W	Type 1 or 3	28mA	49.9Ω	Open
4	25.5W	Type 2 or 3	40mA	34.8Ω	Open
5	40W	Type 3	40mA/2.5mA	1.00kΩ	37.4Ω
6	51W	Type 3	40mA/10.5mA	140Ω	46.4Ω
7	62W	Type 4	40mA/18.5mA	76.8Ω	64.9Ω
8	71.3W	Type 4	40mA/28mA	49.9Ω	118Ω

IEEE 802.3bt PSEs present a single classification event (see Figure 3) to Class 0 through 3 PDs. A Class 0 through 3 PD presents its class signature to the PSE and is then powered on if sufficient power is available. Power limited IEEE 802.3bt PSEs may issue a single event to Class 4 and higher PDs in order to demote those PDs to Class 3 (13W).

IEEE 802.3bt PSEs present up to three classification events, depending on PSE Type, to Class 4 PDs (see Figure 5). Class 4 PDs present a class signature 4 on all events. The third event differentiates a Class 4 PD from a higher Class PD. Power-limited IEEE 802.3bt PSEs may issue three events to Class 5 and higher PDs in order to demote those PDs to Class 4 (25.5W).

IEEE 802.3bt PSEs present four classification events (see Figure 6) to Class 5 and 6 PDs. Class 5 and 6 PDs present a class signature 4 on the first two events, then present a class signature 0 or 1, respectively, on the remaining events. Power limited IEEE 802.3bt PSEs may issue four events to Class 7 and higher PDs in order to demote those PDs to Class 6 (51W).

IEEE 802.3bt PSEs present five classification events (see Figure 7) to Class 7 and 8 PDs. Class 7 and 8 PDs present a class signature 4 on the first two events, then present a class signature 2 or 3, respectively, on the remaining events.

The number of classification/mark events is communicated through the SQ24902 $\overline{T2P}$ pin. See $\overline{T2P}$ Output section for more details.

© 2025 Silergy Corp. All Rights Reserved.

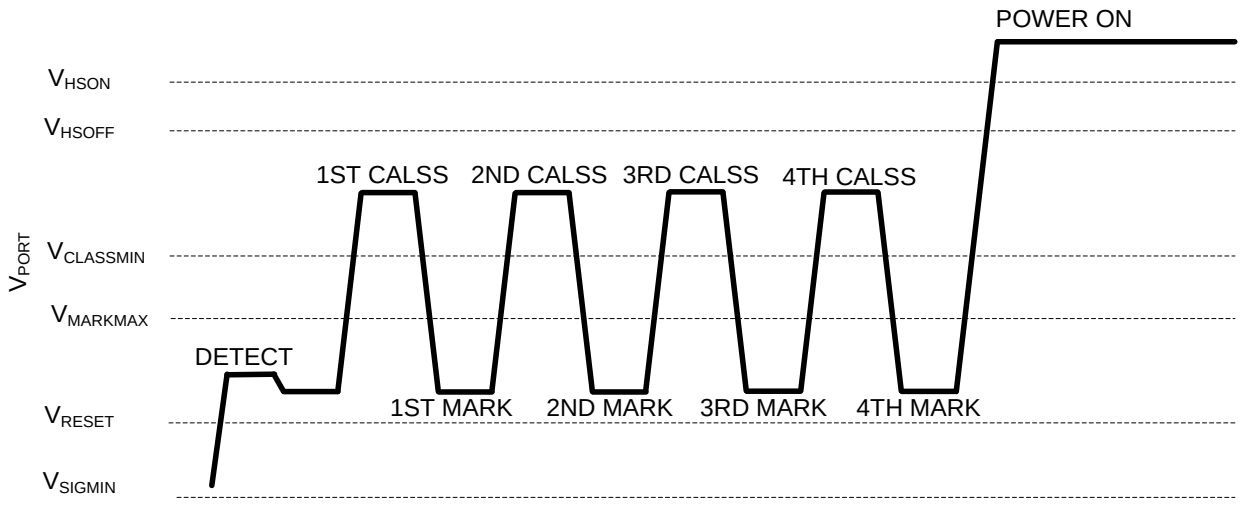


Figure 6. Type 3 or 4 PSE, 4-Event Class Sequence

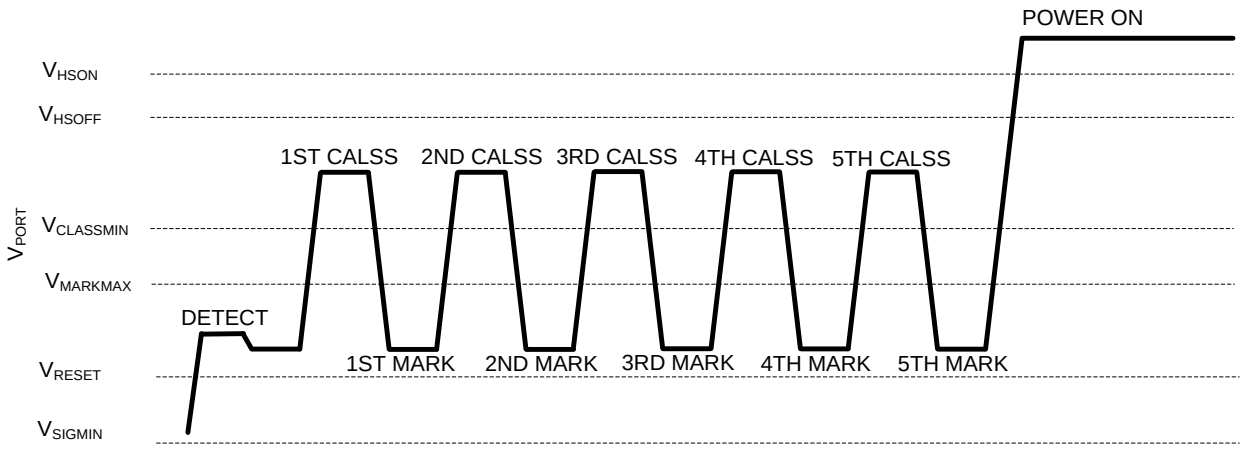


Figure 7. Type 4 PSE, 5-Event Class Sequence

Classification Resistors (R_{CLS} and R_{CLS++})

The R_{CLS} and R_{CLS++} resistors set the classification currents corresponding to the PD power classification. Select the value of R_{CLS} and R_{CLS++} from Table 2 and connect each 1% resistor between the R_{CLASS}, $R_{CLASS++}$ pins and GND.

Detection Signature Corrupt During Mark Event

During the mark event, the SQ24902 presents <11kΩ to the port as required by the IEEE 802.3 specification.

Inrush and Power On

Once the PSE detects and classifies the PD, the PSE then powers on the PD. When the port voltage rises above the V_{HSON} threshold, it begins to source I_{GPU} out of the HSGATE pin. This current flows into an external capacitor, C_{GATE} in Figure 8, that causes a voltage to ramp up the gate of the external MOSFET. The external MOSFET acts as a source follower and ramps the voltage up on the output bulk capacitor, C_{PORT}, thereby determining the inrush current, I_{INRUSH}. Design I_{INRUSH} to be approximately ~100mA. See equation below:

$$I_{INRUSH} = I_{GPU} \frac{C_{OUT}}{C_{GATE}}$$

© 2025 Silergy Corp. All Rights Reserved.

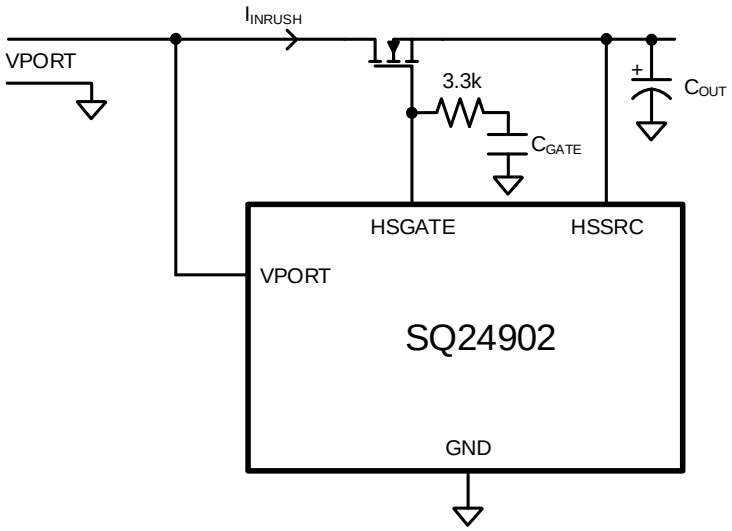


Figure 8. Configuring I_{INRUSH}

The SQ24902 internal charge pump provides an N-channel MOSFET solution, eliminating a larger and more costly P-channel MOSFET. The low $R_{DS(ON)}$ MOSFET also maximizes power delivery and efficiency, reduces power and heat dissipation, and eases thermal design.

Power Good

The PWRGD pin is held low by its open drain output until HSGATE charges up to approximately 8V above HSSRC. The PWRGD pin is used to hold off the downstream circuitry until inrush is complete and the external MOSFET is fully enhanced. The HSGATE pin remains high and the PWRGD pin remains open-drain until the port voltage falls below V_{HSOFF}.

Auxiliary Supply Override

If the AUX pin is held above V_{AUXT}, the SQ24902 enters auxiliary power supply override mode. In this mode the signature resistor disconnects, classification is disabled, HSGATE pulls down, the PWRGD pin is open drain and $\overline{T2P}$ pin indicates max available power.

The AUX pin allows for setting the auxiliary supply turn on and turn off voltage thresholds, V_{AUXON}, and V_{AUXOFF} respectively. Use the following equations to set V_{AUXON} and V_{AUXOFF} via R_1 and R_2 in Figure 9. Note that an internal 6.7V Zener limits the voltage on the AUX pin.

A capacitor up to 1000pF may be placed between the AUX pin and GND to improve noise immunity. V_{AUXON} must be lower than V_{HSOFF}.

$$V_{AUXON} = (\frac{R_1}{R_2} + 1)V_{AUXT} + I_{AUXT}R_1$$

$$V_{AUXOFF} = V_{AUXON} - (\frac{R_1}{R_2} + 1)V_{AUX\_HY}$$

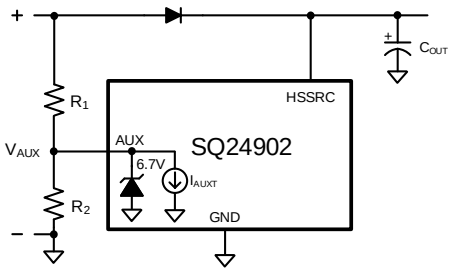


Figure 9. AUX Threshold and Hysteresis Calculation

© 2025 Silergy Corp. All Rights Reserved.

AUX Zener Limit

If the AUX pin is held above 6.7V of Zener**,** the SQ24902 will clamp 6.7V on the AUX pin. The current of the flowing AUX pin is not allowed larger than 1.4mA and R_1 calculation formula is as follows.

$$R_1 \geq \frac{V_{AUX(MAX)} - 6.7V}{1.4mA}$$

$\overline{\text{T2P}}$ Output

The SQ24902 communicates the PSE allocated power to the PD application via the $\overline{\text{T2P}}$ pin. The $\overline{\text{T2P}}$ pin state is determined by the AUX pin, the RCLASS++ pin, and the number of classification events. The SQ24902 uses a 4-state encoding for the $\overline{\text{T2P}}$ output. $\overline{\text{T2P}}$ state and the associated PSE allocated power are shown in Table 3.

Table 3. $\overline{\text{T2P}}$ Response to Determine PSE Allocated Power

AUX STATE	PD REQUESTED CLASS(RCALSS/ RCLASS++)	NUMBER OF CLASSIFICATIO N EVENTS	$\overline{\text{T2P}}$ WITH RESPECT TO GND	PSE ALLOCATED POWER
AUXILIARY	0-4	N/A	Low-Z	AUX Power
	5-8	N/A	25% Low-Z 75% HI-Z	AUX Power
PoE	0-4	1	HI-Z	13W
		≥2	Low-Z	25.5W
	5-8	1	HI-Z	13W
		2 or 3	Low-Z	25.5W
		4	50% Low-Z 50% HI-Z	Min(PD Requested Class, 51W)
		5	25% Low-Z 75% HI-Z	Min(PD Requested Class, 71.3W)

The highest priority input is the AUX pin. AUX is asserted to enter the auxiliary power state and deasserted to enter the PoE state. In the auxiliary power state, the $\overline{\text{T2P}}$ pin indicates the highest available power, based on PD Requested Class. The auxiliary power supply must be sized to provide at least the PD Requested Class Power.

Second, the PD Requested Class is configured using the RCLASS and RCLASS++ pins. The RCLASS++ pin alone can be used to determine if the PD Class is 0-4 or 5-8, as shown in Table 2.

Last, the number of classification events determines the amount of power allocated by the PSE as described in Table 1.

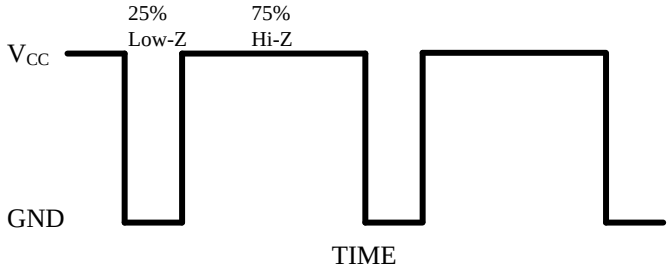


Figure10. Response Example for 25% Low-Z, 75% Hi-Z

© 2025 Silergy Corp. All Rights Reserved.

Over Temperature Protection

The IEEE 802.3 specification requires a PD to withstand any applied voltage from 0V to 57V indefinitely. During classification, however, the power dissipation in the SQ24902 may be as high as 1.5W. The SQ24902 can easily tolerate this power for the maximum IEEE classification timing but overheats if this condition persists abnormally. The SQ24902 includes an over temperature protection feature which is intended to protect the device during momentary overload conditions. If the junction temperature exceeds the over temperature threshold, the SQ24902 pulls down HSGATE pin, and disables classification.

✧ EXTERNAL INTERFACE AND COMPONENT SELECTION

PoE Input Bridge

A PD is required to polarity-correct its input voltage. There are several different options available for bridge rectifiers; silicon diodes, Schottky diodes, and ideal diodes. When silicon or Schottky diode bridges are used, the diode forward voltage drops affect the voltage at the VPORT pin. The SQ24902 is designed to tolerate these voltage drops. Note, the voltage parameters shown in the Electrical Characteristics are specified at the SQ24902 package pins.

A silicon diode bridge consumes up to 4% of the available power. In addition, silicon diode bridges exhibit poor pairset-to-pairset unbalance performance. Each branch of a silicon diode bridge shares source/return current, and thermal runaway can cause large, non-compliant current unbalances between pairsets.While using Schottky diodes can help reduce the power loss with a lower forward voltage, the Schottky bridge may not be suitable for high temperature PD applications.

Schottky diode bridges exhibit temperature induced leakage currents. The leakage current has a voltage dependency that can invalidate the measured detection signature. In addition, these leakage currents can back-feed through the unpowered branch and the unused bridge, violating IEEE 802.3 specifications.

Auxiliary Input Diode Bridge

Some PDs are required to receive AC or DC power from an auxiliary power source. A diode bridge is typically required to handle the voltage rectification and polarity correction.

Input Capacitor

A 0.1μF capacitor is needed from VPORT to GND to meet the input impedance requirement in IEEE 802.3 and to properly bypass the SQ24902.

Transient Voltage Suppressor

The SQ24902 specifies an absolute maximum voltage of 100V and is designed to tolerate brief over voltage events due to Ethernet cable surges. To protect the SQ24902 from an over voltage event, install a unidirectional transient voltage suppressor (TVS) such as an SMAJ60A between the VPORT and GND pins. For PD applications that require an auxiliary power input, install a TVS between VIN and GND. See Layout Considerations for TVS placement.

Layout Considerations

Avoid excessive parasitic capacitance on the RCLASS and RCLASS++ pins and place resistors R_1 and R_2 close to the SQ24902

It is strictly required for maximum protection to place the 0.1μF input capacitor, C_{PD}, and transient voltage suppressor as close to the SQ24902 as possible.

© 2025 Silergy Corp. All Rights Reserved.

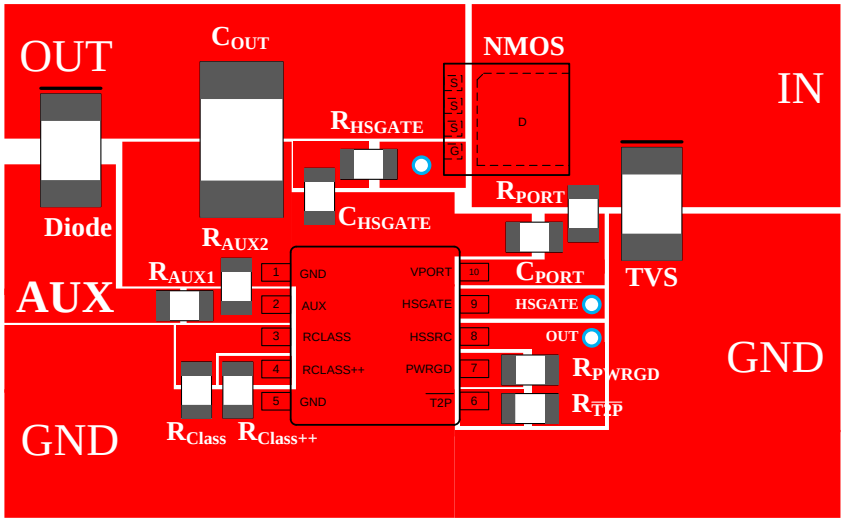
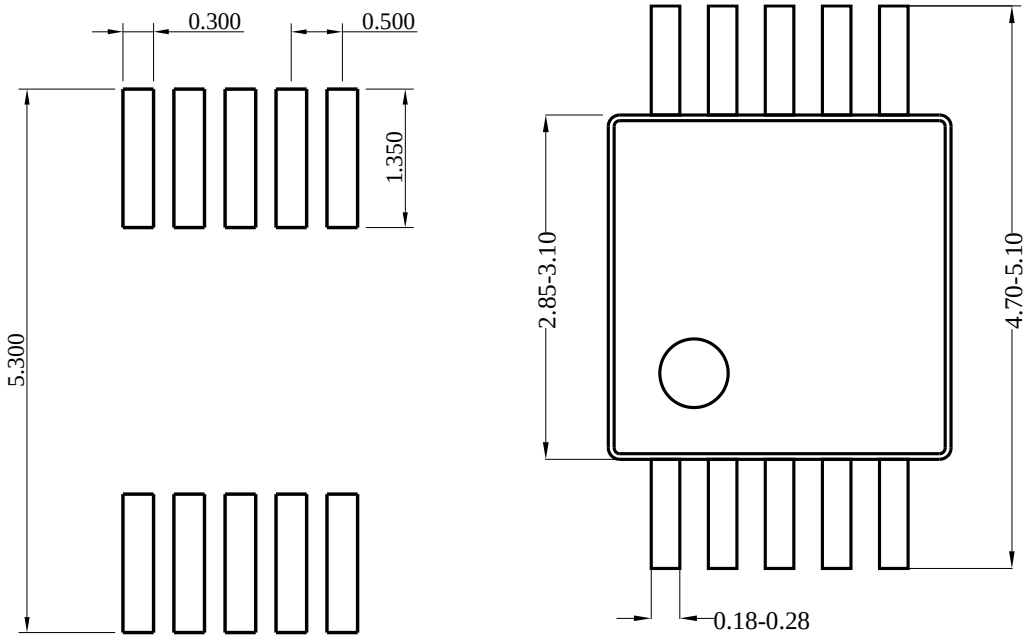


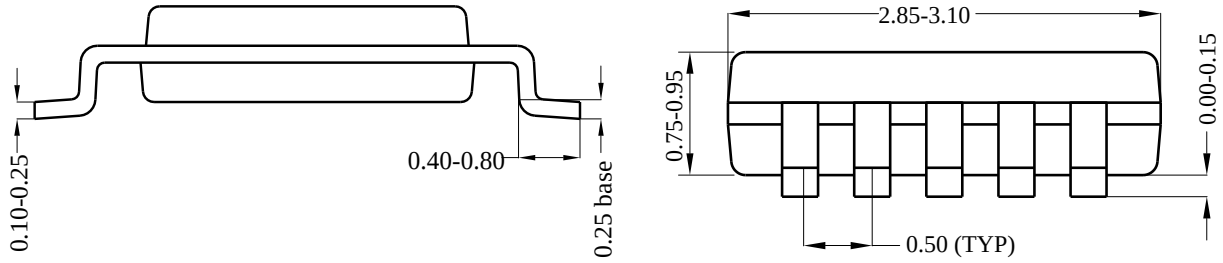
Figure11. PCB Layout Suggestion

© 2025 Silergy Corp. All Rights Reserved.

MSOP10 Package Outline & PCB Layout



Recommended Pad Layout



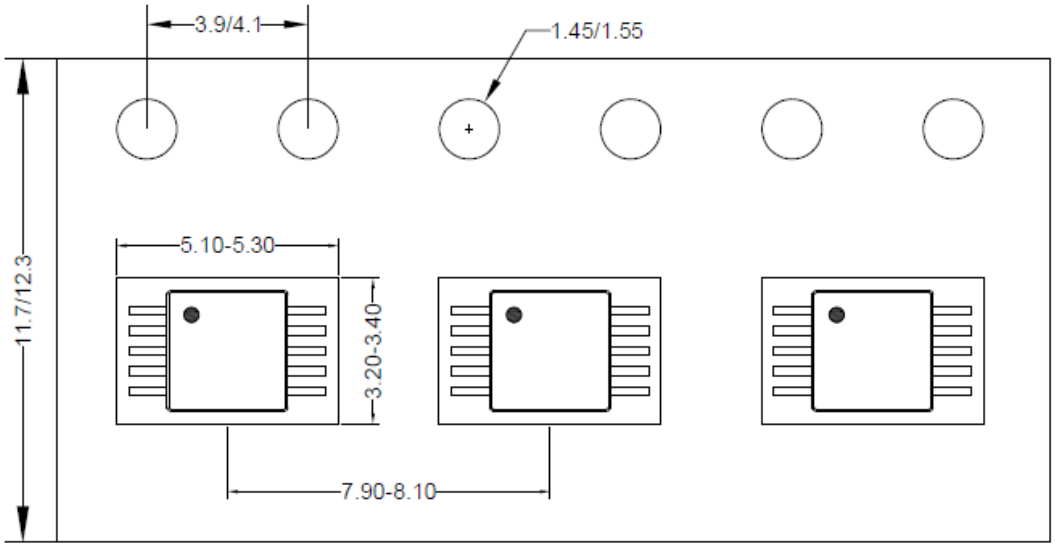
Notes: **All dimension in millimeter and exclude mold flash & metal burr.**

© 2025 Silergy Corp. All Rights Reserved.

Taping & Reel Specification

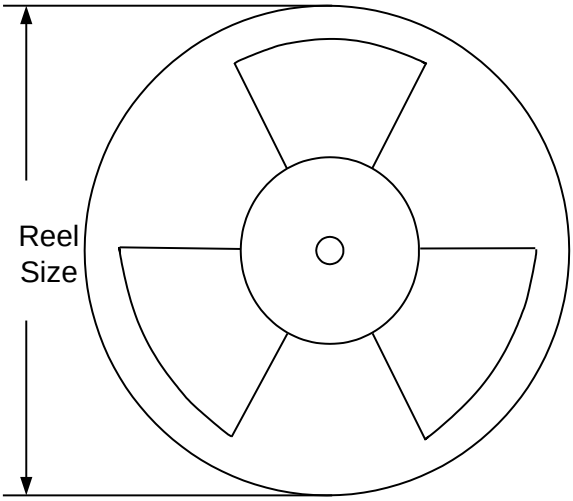
1. Taping Orientation

MSOP10



Feeding direction ⟶

2. Carrier Tape & Reel Specification for Packages



Package types	Tape width (mm)	Pocket pitch(mm)	Reel size (Inch)	Trailer length(mm)	Leader length (mm)	Qty per reel
MSOP10	12	8	13"	400	400	3000

3. Others: NA

© 2025 Silergy Corp. All Rights Reserved.

Revision History

The revision history provided is for informational purpose only and is believed to be accurate, however, not warranted. Please make sure that you have the latest revision.

Date	Revision	Change
Jan.20, 2023	Revision 1.0	Initial Production Release
Jan. 20, 2022	Revision 0.9	Initial Release

© 2025 Silergy Corp. All Rights Reserved.

IMPORTANT NOTICE

1. **Right to make changes.** Silergy and its subsidiaries (hereafter Silergy) reserve the right to change any information published in this document, including but not limited to circuitry, specification and/or product design, manufacturing or descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products are sold subject to Silergy's standard terms and conditions of sale.

2. Applications. Application examples that are described herein for any of these products are for illustrative purposes only. Silergy makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification. Buyers are responsible for the design and operation of their applications and products using Silergy products. Silergy or its subsidiaries assume no liability for any application assistance or designs of customer products. It is customer's sole responsibility to determine whether the Silergy product is suitable and fit for the customer's applications and products planned. To minimize the risks associated with customer's products and applications, customer should provide adequate design and operating safeguards. Customer represents and agrees that it has all the necessary expertise to create and implement safeguards which anticipate dangerous consequences of failures, monitor failures and their consequences, lessen the likelihood of failures that might cause harm and take appropriate remedial actions. Silergy assumes no liability related to any default, damage, costs or problem in the customer's applications or products, or the application or use by customer's third-party buyers. Customer will fully indemnify Silergy, its subsidiaries, and their representatives against any damages arising out of the use of any Silergy components in safety-critical applications. It is also buyers' sole responsibility to warrant and guarantee that any intellectual property rights of a third party are not infringed upon when integrating Silergy products into any application. Silergy assumes no responsibility for any said applications or for any use of any circuitry other than circuitry entirely embodied in a Silergy product.

3. **Limited warranty and liability.** Information furnished by Silergy in this document is believed to be accurate and reliable. However, Silergy makes no representation or warranty, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information. In no event shall Silergy be liable for any indirect, incidental, punitive, special or consequential damages, including but not limited to lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges, whether or not such damages are based on tort or negligence, warranty, breach of contract or any other legal theory. Notwithstanding any damages that customer might incur for any reason whatsoever, Silergy' aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the Standard Terms and Conditions of Sale of Silergy.

4. **Suitability for use.** Customer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of Silergy components in its applications, notwithstanding any applications-related information or support that may be provided by Silergy. Silergy products are not designed, authorized or warranted to be suitable for use in life support, life-critical or safety-critical systems or equipment, nor in applications where failure or malfunction of a Silergy product can reasonably be expected to result in personal injury, death or severe property or environmental damage. Silergy assumes no liability for inclusion and/or use of Silergy products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

5. **Terms and conditions of commercial sale**. Silergy products are sold subject to the standard terms and conditions of commercial sale, as published at http://www.silergy.com/stdterms, unless otherwise agreed in a valid written individual agreement specifically agreed to in writing by an authorized officer of Silergy. In case an individual agreement is concluded only the terms and conditions of the respective agreement shall apply. Silergy hereby expressly objects to and denies the application of any customer's general terms and conditions with regard to the purchase of Silergy products by the customer.

6. **No offer to sell or license**. Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights. Silergy makes no representation or warranty that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right. Information published by Silergy regarding third-party products or services does not constitute a license to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from Silergy under the patents or other intellectual property of Silergy.

For more information, please visit: www.silergy.com

©2025 Silergy Corp. **All Rights Reserved.**

© 2025 Silergy Corp. All Rights Reserved.