SY58215

Flyback Regulator For LED Lighting

General Description

SY58215 is a single stage Flyback PFC regulator targeting at LED lighting applications.

SY58215 integrates a 650V MOSFET to decrease physical volume. It adopts the proprietary control architecture to achieve an accurate regulation of LED current, unity power factor.Quasi-Resonant valley turn-on for high efficiency operation. Proprietary self-bias technique saves the bias supply and reduces the start up time.

SY58215 integrates open/short LED protection and eliminates the need for opto-coupler or auxiliary winding (in floating switch application), thus minimizing the component count and board size.

Ordering Information

SY58215□(□□)□
Temperature Code
Package Code
Optional Spec Code

Ordering Number	Package type	Note
SY58215FAC	SO8	----

Features

- Integrated 650V MOSFET
- Quasi-Resonant (QR) Mode to Achieve Low Switching Losses
- No Opto-coupler or Auxiliary Winding for Feedback in the Proprietary Floating Switch Configuration.
- Reliable Short LED and Open LED Protection
- Thermal Foldback Function
- Power Factor>0.9 with Internal Loop Compensation
- Maximum Output Power : 20W
- Compact Package: SO8

Applications

- LED Lighting

Typical Applications

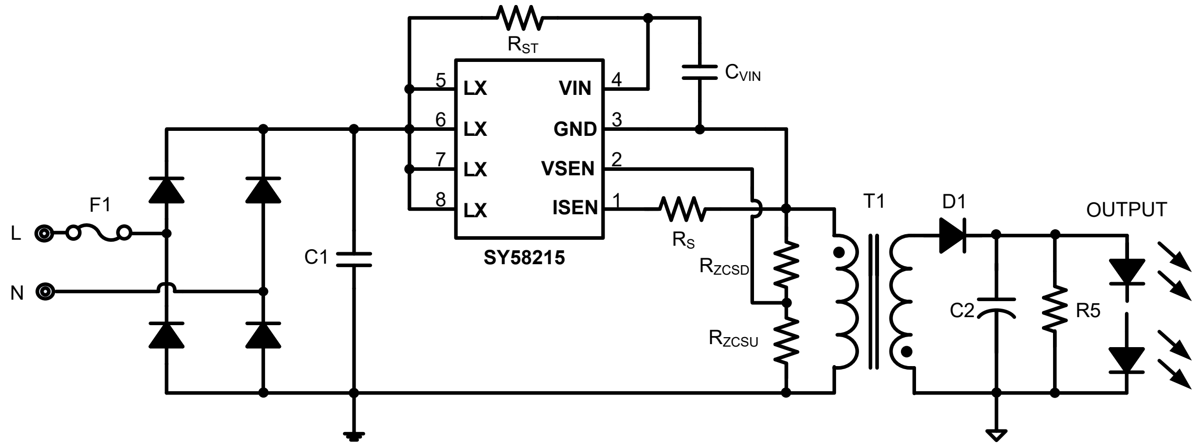
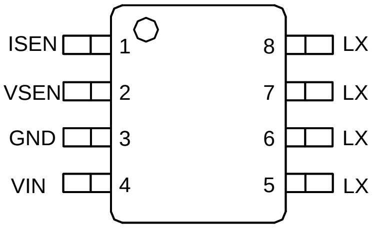


Fig.1 Schematic Diagram

Pinout (top view)



(SO8)

Top Mark: BIQ*xyz* (device code: BIQ, ***x=year code, y=week code, z= lot number code***)

Pin Name	Pin number	Pin Description
ISEN	1	Current set pin. Connect a resistor to program the reference output current. $I_O = \frac{V_{REF} \times N_{PS}}{2 \times R_{ISEN}}$
VSEN	2	Voltage sense pin. Connect to a resistor divider of inductor or auxiliary winding to sense output voltage.
GND	3	Ground Pin.
VIN	4	Power supply pin.
LX	5-8	Internal HV MOSFET drain pin.

Block Diagram

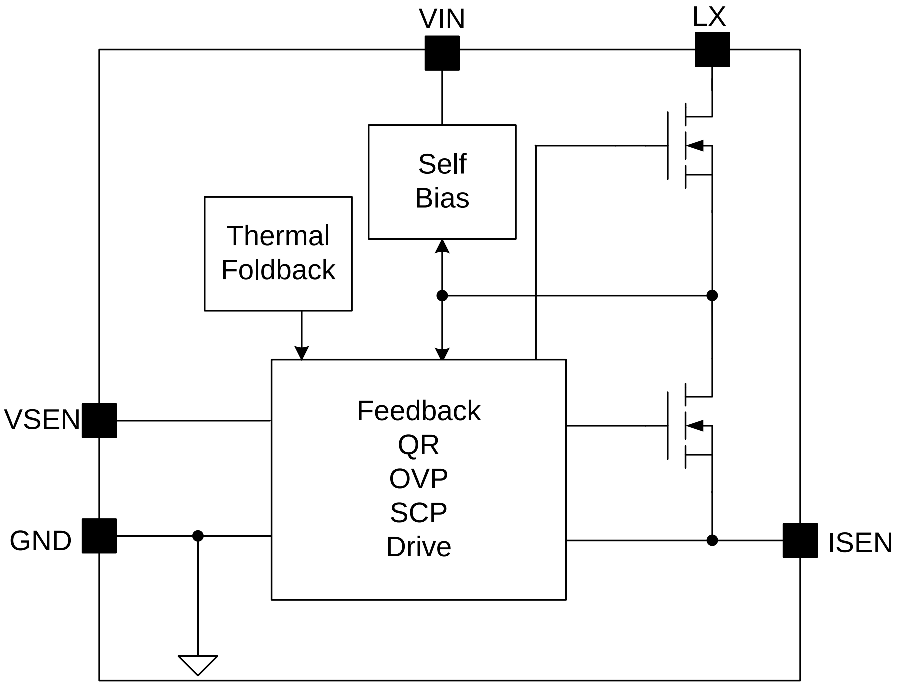


Fig.2 Simplified block diagram

Absolute Maximum Ratings (Note 1)

ISEN -- -0.3V~3.6V
VSEN -- -0.3V~16V
VIN -- -0.3V~22V
I_{VIN} -- 25mA
LX-- 650V
Power Dissipation, @ TA = 25°C SO8--1.1W
Package Thermal Resistance (Note 2)
    SO8, θ_{JA}-- 88°C/W
    SO8, θ_{JC}--45°C/W
Lead Temperature (Soldering, 10 sec.) -- 260°C
Storage Temperature Range -- -65°C to 150°C

Recommended Operating Conditions

Junction Temperature Range -- -40°C to 125°C

Electrical Characteristics

(V_{VIN}= 12V (Note 3), T_A = 25°C unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Power Supply Section						
VIN Turn-on Threshold	V_{VIN_ON}			14	15	V
VIN Turn-off Threshold	V_{VIN_OFF}		6	7		V
Start up Current	I_{ST}	VIN=13V		30	40	µA
Quiescent Current	I_Q	VIN=15V		300	390	µA
Shunt Current	I_{Shunt}	VIN=V_{VIN_ON}+4V	10	17		mA
VSEN Pin Section						
VSEN Pin Reference Voltage	V_{VSEN_OVP}		1.43	1.5	1.58	V
Driver Section						
Min ON Time	t_{ON_MIN}			320		ns
Max ON Time	t_{ON_MAX}			13		µs
Min OFF Time	t_{OFF_MIN}			1.7		µs
Max OFF Time	t_{OFF_MAX}			230		µs
Max Switching Frequency	f_{MAX}			150		kHz
ISEN Pin Section						
Current Limit Threshold Voltage	V_{ISEN_OCP}			850		mV
Current Reference	V_{REF}		294	300	306	mV
Integrated MOSFET Section						
BV of HV MOSFET	V_{BV}	I_{LX}=250uA	650			V
Rdson of HV MOSFET	R_{DSON}			4.4	6	Ω
Thermal Section						
Thermal Foldback Temperature	T_{FB}			155		ºC

Note 1: Stresses beyond the “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: θ_{JA} is measured in the natural convection at T_A = 25°C on a low effective single layer thermal conductivity test board of JEDEC 51-3 thermal measurement standard. Test condition: Device mounted on 2” x 2” FR-4 substrate PCB, 2oz copper, with minimum recommended pad on top layer and thermal vias to bottom layer ground plane.

Note 3: Increase VIN pin voltage gradually higher than V_{VIN_ON} voltage then turn down to 12V.

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Operation

SY58215 is a constant current Flyback PFC regulator targeting at LED lighting applications.

In order to reduce the switching losses and improve EMI performance, Quasi-Resonant switching mode is applied, which means to turn on the power MOSFET at valley of drain voltage.

Proprietary self-bias technique eliminates the need for bias winding thus minimizes the PCB footprint and associated power loss.

Short Circuit Protection works in hiccup mode. The resulting short circuit power loss is much less than continuous working mode.

SY58215 also provides reliable protections such as Open LED Protection (OLP), Over Temperature Protection (OTP), etc.

SY58215 is available with SO8 package.

Applications Information

Start up

After AC supply or DC BUS is powered on, the capacitor C_{VIN} across VIN and GND pin is charged up by BUS voltage through a start up resistor R_{ST}. Once V_{VIN} rises up to V_{VIN_ON}, the internal blocks start to work. Then IC can be supplied at every switching cycle. The supply current is balanced with IC consumption current to maintain V_{VIN} above V_{VIN_OFF}.

The whole start up procedure is divided into two sections shown below. t_{STC} is the C_{VIN} charged up section, and t_{STO} is the time V_{VIN} falls to a steady state value. Usually t_{STO} is much smaller than t_{STC}.

If bias supply has more power than IC consumption, V_{VIN} is greater than V_{VIN_Shunt}, then a shunt current works to maintain V_{VIN} under V_{VIN_Shunt}.

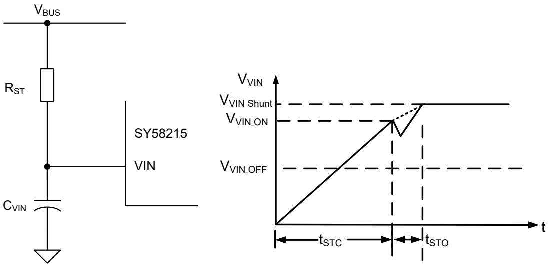


Fig.3 Start up

The start up resistor R_{ST} and C_{VIN} are designed by rules below:

(a) Preset start-up resistor R_{ST}, make sure that the current through R_{ST} is larger than I_{ST}.

$$R_{ST} < \frac{V_{BUS}}{I_{ST}}$$

Where V_{BUS} is the BUS line voltage.

(b) Select C_{VIN} to obtain an ideal start up time t_{ST}.

$$C_{VIN} = \frac{\left(\frac{V_{BUS}}{R_{ST}} - I_{ST}\right) \times t_{ST}}{V_{VIN\_ON}}$$

(c) If R_{ST} and C_{VIN} are chosen to a very small start up time, SCP and OVP power loss will be large. Then C_{VIN} and R_{ST} time constant should be increased.

Proprietary self-bias technique allows C_{VIN} to be charged every switching cycle. There is no need to add auxiliary winding for power supply. C_{VIN} can be chosen with small value and small package to save cost.

Shut down

After AC supply or DC BUS is powered off, the energy stored in the BUS capacitor will be discharged. When power supply for IC is not enough, V_{VIN} will drop down. Once V_{VIN} is below V_{VIN_OFF}, the IC will stop working.

Constant-current control

Primary side control is applied to eliminate secondary feedback circuit or opto-coupler, which reduces the circuit cost. The switching waveforms are shown in Fig.4.

The output current I_{OUT} can be represented by,

$$I_{OUT} = \frac{I_{SP}}{2} \times \frac{t_{DIS}}{t_S}$$

Where I_{SP} is the peak current of the secondary side; t_{DIS} is the discharge time of Flyback transformer; t_S is the switching period.

The secondary peak current is related with primary peak current, if the effect of the leakage inductor is neglected.

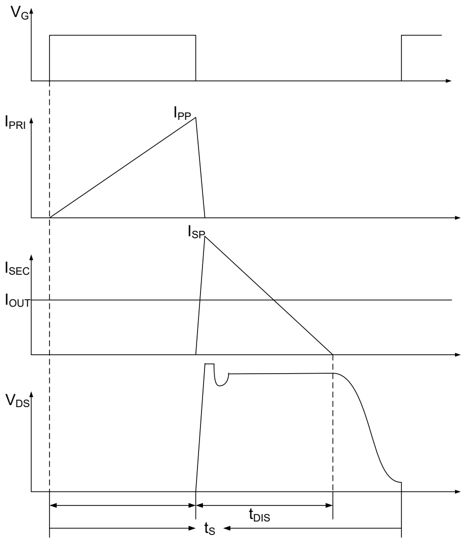


Fig.4 switching waveforms

$$I_{SP} = N_{PS} \times I_{PP}$$

Where N_{PS} is the turns ratio of primary to secondary of the Flyback transformer. Thus, I_{OUT} can be represented by

$$I_{OUT} = \frac{N_{PS} \times I_{PP}}{2} \times \frac{t_{DIS}}{t_S}$$

The primary peak current I_{PP} is detected by ISEN pin, and inductor current discharge time t_{DIS} is detected by internal circuit, which is shown in Fig.5. These singals are processed and applied to the negative input of the gain modulator. In static state, the positive and negative inputs are equal.

$$V_{REF} = I_{PP} \times R_S \times \frac{t_{DIS}}{t_S}$$

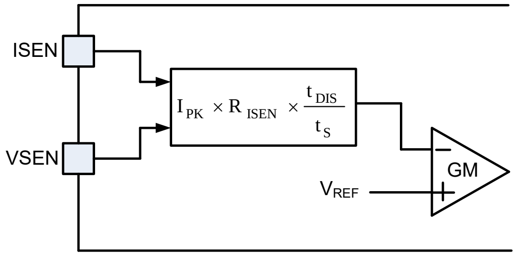


Fig.5 Output current detection diagram

Finally, the output current I_{OUT} can represented by

$$I_{OUT} = \frac{V_{REF} \times N_{PS}}{R_S \times 2}$$

Where V_{REF} is the internal reference voltage; R_S is the current sense resistor. I_{OUT} can be programmed by N_{PS} and R_S.

$$R_S = \frac{V_{REF} \times N_{PS}}{I_{OUT} \times 2}$$

Quasi-Resonant Operation

QR mode operation provides low turn-on switching losses for Flyback converter.

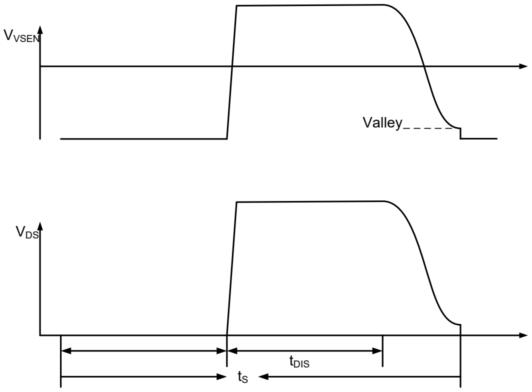


Fig.6 QR mode operation

The voltage across drain and source of the MOSFET is reflected by a resistor divider across Inductor. VSEN pin detects the voltage via this resistor divider. When the voltage across drain and source of the MOSFET is at voltage valley, the MOSFET would be turned on.

Over Voltage Protection (OVP) & Open LED Protection (OLP)

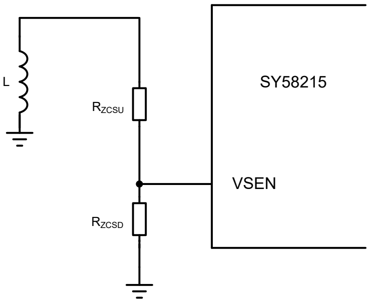


Fig.7 OVP&OLP

The output voltage is reflected by a resistor divider across Inductor to VSEN pin. When the load is null or large transient happens, the output voltage will exceed the rated value. When V_{VSEN} exceeds V_{VSEN_OVP}, the over voltage protection is triggered and the IC will discharge V_{VIN} by an internal current source I_{VIN_OVP}. Once V_{VIN} is below V_{VIN_OFF}, the IC will shut down and be charged again by BUS voltage through start up resistor. If the over voltage condition still exists, the system will operate in hiccup mode.

Thus, the resistor divider is related with the OVP function.

$$\frac{V_{VSEN\_OVP}}{N_{PS} \times V_{OVP}} = \frac{R_{ZCSD}}{R_{ZCSD} + R_{ZCSU}}$$

Where V_{OVP} is the output over voltage specification. R_{ZCSU} and R_{ZCSD} compose the resistor divider.

Short Circuit Protection (SCP)

When the output is shorted, demagnetizing voltage of inductor is zero, so t_{OFF} will be clamped at t_{OFF_MAX}, when t_{OFF_MAX} shows up for 64 times, SCP is triggered and the IC will discharge V_{VIN} by an internal current source I_{VIN_SCP}. Once V_{VIN} is below V_{VIN_OFF}, the IC will shut down and be charged again by BUS voltage through start up resistor. If the short circuit condition still exists, the system will operate in hiccup mode.

Thermal function

If the junction temperature T_J is higher than T_{FB}, the output current will be folded back to decrease LED temperature. With this function, high LED application efficiency is achieved.

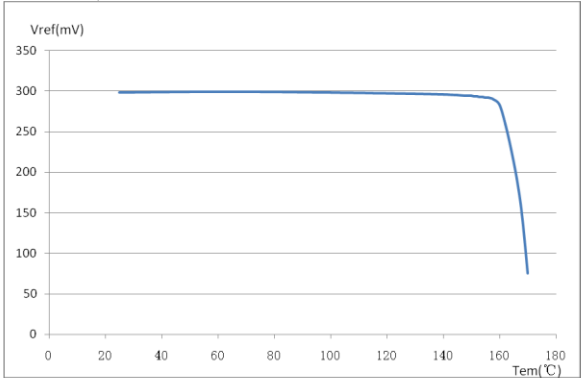


Fig.8 typical thermal foldback curve

Line regulation modification

The IC provides line regulation modification function to improve line regulation performance.

Due to the sample delay of ISEN pin and other internal delay, the output current increases with increasing input BUS line voltage. A small compensation voltage ΔV_{ISEN_C} is added to ISEN pin during ON time to improve such performance. This ΔV_{ISEN_C} is adjusted by the upper resistor of the divider connected to VSEN pin.

$$\Delta V_{ISET\_C} = \frac{V_{BUS}}{R_{ZCSU}} \times k_1$$

Where R_{ZCSU} is the upper resistor of the divider; k_1 is an internal constant as the modification coefficient, $k_1 = 9$.

The compensation is mainly related with R_{ZCSU}, larger compensation is achieved with smaller R_{ZCSU}. Normally, R_{ZCSU} ranges from 200kΩ~800kΩ.

Then R_{ZCSD} can be selected by formula

$$\frac{V_{VSEN\_OVP}}{N_{PS} \times V_{OVP}} = \frac{R_{ZCSD}}{R_{ZCSD} + R_{ZCSU}} .$$

Power Device Design

MOSFET and Diode

When the operation condition is with maximum input voltage and full load, the voltage stress of MOSFET and secondary power diode is maximized;

$$V_{MOS\_DS\_MAX}=\sqrt{2}V_{AC\_MAX}+N_{PS}\times(V_{OUT}+V_{D\_F})+\Delta V_S$$

$$V_{D\_R\_MAX}=\frac{\sqrt{2}V_{AC\_MAX}}{N_{PS}}+V_{OUT}$$

Where V_{AC-MAX} is maximum input AC RMS voltage; N_{PS} is the turns ratio of the Flyback transformer; V_{OUT} is the rated output voltage; V_{D-F} is the forward voltage of secondary power diode; ΔV_S is the overshoot voltage clamped by RCD snubber during OFF time.

When the operation condition is with minimum input voltage and full load, the current stress of MOSFET and power diode is maximized.

$$I_{MOS\_PK\_MAX}=I_{P\_PK\_MAX}$$

$$I_{MOS\_RMS\_MAX}=I_{P\_RMS\_MAX}$$

$$I_{D\_PK\_MAX}=N_{PS}\times I_{P\_PK\_MAX}$$

$$I_{D\_AVG}=I_{OUT}$$

Where $I_{P-PK-MAX}$ and $I_{P-RMS-MAX}$ are maximum primary peak current and RMS current, which will be introduced later.

Transformer (N_{PS} and L_M)

N_{PS} is limited by the electrical stress of the power MOSFET:

$$N_{PS}\le\frac{V_{MOS\_(BR)DS}\times 90\%-\sqrt{2}V_{AC\_MAX}-\Delta V_S}{V_{OUT}+V_{D\_F}}$$

Where $V_{MOS-(BR)DS}$ is the breakdown voltage of the power MOSFET(650V).

In Quasi-Resonant mode, each switching period cycle t_S consists of three parts: current rising time t_1, current falling time t_2 and quasi-resonant time t_3 shown in below.

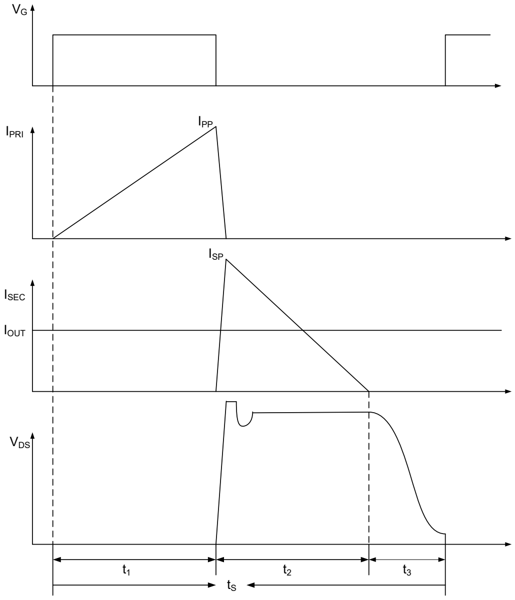


Fig.9 switching waveforms

The system operates in the constant on time mode to achieve high power factor. The ON time increases with the input AC RMS voltage decreasing and the load increasing. When the operation condition is with minimum input AC RMS voltage and full load, the ON time is maximized. On the other hand, when the input voltage is at the peak value, the OFF time is maximized. Thus, the minimum switching frequency f_{S-MIN} happens at the peak value of input voltage with minimum input AC RMS voltage and maximum load condition; meanwhile, the maximum peak current through MOSFET and the transformer happens.

Once the minimum frequency f_{S-MIN} is set, the inductance of the transformer could be induced. The design flow is shown as below:

(a) Select N_{PS}

$$N_{PS}\le\frac{V_{MOS\_(BR)DS}\times 90\%-\sqrt{2}V_{AC\_MAX}-\Delta V_S}{V_{OUT}+V_{D\_F}}$$

(b) Preset minimum frequency f_{S-MIN}

(c) Compute relative t_S, t_1 (t_3 is omitted to simplify the design here)

$$t_S=\frac{1}{f_{S\_MIN}}$$

$$t_1=\frac{t_S\times N_{PS}\times(V_{OUT}+V_{D\_F})}{\sqrt{2}V_{AC\_MIN}+N_{PS}\times(V_{OUT}+V_{D\_F})}$$

(d) Design inductance L_M

$$L_M=\frac{V_{AC\_MIN}^2\times t_1^2\times\eta}{2P_{OUT}\times t_S}$$

(e) Compute t_3

$$t_3=\pi\times\sqrt{L_M\times C_{Drain}}$$

Where C_{Drain} is the parasitic capacitance at drain of MOSFET.

(f) Compute primary maximum peak current $I_{P\text{-}PK\text{-}MAX}$ and RMS current $I_{P\text{-}RMS\text{-}MAX}$ for the transformer fabrication.

$$I_{P\_PK\_MAX}=\frac{2P_{OUT}\times[\frac{L_M}{\sqrt{2}V_{AC\_MIN}}+\frac{L_M}{N_{PS}\times(V_{OUT}+V_{D\_F})}]}{L_M\times\eta}$$
$$+\frac{\sqrt{4P_{OUT}^2\times[\frac{L_M}{\sqrt{2}V_{AC\_MIN}}+\frac{L_M}{N_{PS}\times(V_{OUT}+V_{D\_F})}]^2+4L_M\times\eta\times P_{OUT}\times t_3}}{L_M\times\eta}$$

Where η is the efficiency; P_{OUT} is rated full load power

Adjust t_1 and t_S to t_1' and t_S' considering the effect of t_3

$$t'_S=\frac{\eta\times L_M\times I_{P\_PK\_MAX}^2}{4P_{OUT}}$$

$$t'_1=\frac{L_M\times I_{P\_PK\_MAX}}{\sqrt{2}V_{AC\_MIN}}$$

$$I_{P\_RMS\_MAX}\approx\sqrt{\frac{t'_1}{6t'_S}}\times I_{P\_PK\_MAX}$$

(g) Compute secondary maximum peak current $I_{S\text{-}PK\text{-}MAX}$ and RMS current $I_{S\text{-}RMS\text{-}MAX}$ for the transformer fabrication.

$$I_{S\_PK\_MAX}=N_{PS}\times I_{P\_PK\_MAX}$$

$$t'_2=t'_S-t'_1-t_3$$

$$I_{S\_RMS\_MAX}\approx\sqrt{\frac{t'_2}{6t'_S}}\times I_{S\_PK\_MAX}$$

Transformer design (N_P,N_S)

The design of the transformer is similar with ordinary Flyback transformer. The parameters below are necessary:

Necessary parameters	
Turns ratio	N_{PS}
Inductance	L_M
Primary maximum current	$I_{P\text{-}PK\text{-}MAX}$
Primary maximum RMS current	$I_{P\text{-}RMS\text{-}MAX}$
Secondary maximum RMS current	$I_{S\text{-}RMS\text{-}MAX}$

The design rules are as followed:

(a) Select the magnetic core style, identify the effective area A_e.

(b) Preset the maximum magnetic flux ΔB

$$\Delta B=0.22\sim0.26T$$

(c) Compute primary turn N_P

$$N_P=\frac{L_M\times I_{P\_PK\_MAX}}{\Delta B\times A_e}$$

(d) Compute secondary turn N_S

$$N_S=\frac{N_P}{N_{PS}}$$

(e) Select an appropriate wire diameter

With $I_{P\text{-}RMS\text{-}MAX}$ and $I_{S\text{-}RMS\text{-}MAX}$, select appropriate wire to make sure the current density ranges from 4A/mm^2 to 10A/mm^2.

(f) If the winding area of the core and bobbin is not enough, reselect the core style, go to **(a)** and redesign the transformer until the ideal transformer is achieved.

Output capacitor C_{OUT}

Preset the output current ripple ΔI_{OUT}, C_{OUT} is induced by

$$C_{OUT}=\frac{\sqrt{(\frac{2I_{OUT}}{\Delta I_{OUT}})^2-1}}{4\pi f_{AC}R_{LED}}$$

Where I_{OUT} is the rated output current; ΔI_{OUT} is the demanded current ripple; f_{AC} is the input AC supply frequency; R_{LED} is the equivalent series resistor of the LED load.

RCD snubber for MOSFET

The power loss of the snubber P_{RCD} is evaluated first

$$P_{RCD} = \frac{N_{PS} \times (V_{OUT} + V_{D\_F}) + \Delta V_S}{\Delta V_S} \times \frac{L_K}{L_M} \times P_{OUT}$$

Where N_{PS} is the turns ratio of the Flyback transformer; V_{OUT} is the output voltage; V_{D-F} is the forward voltage of the power diode; ΔV_S is the overshoot voltage clamped by RCD snubber; L_K is the leakage inductor; L_M is the inductance of the Flyback transformer; P_{OUT} is the output power.

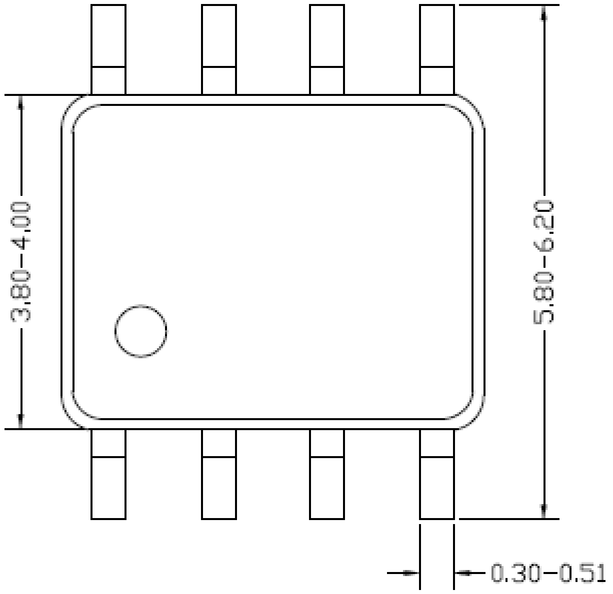
The R_{RCD} is related with the power loss:

$$R_{RCD} = \frac{(N_{PS} \times (V_{OUT} + V_{D\_F}) + \Delta V_S)^2}{P_{RCD}}$$

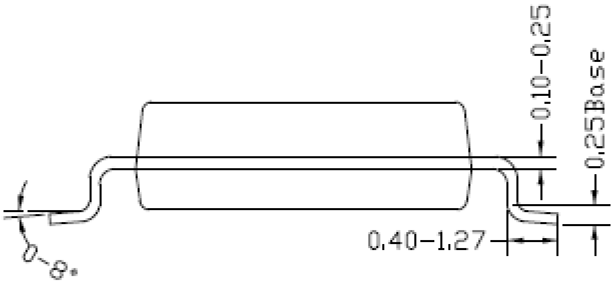
The C_{RCD} is related with the voltage ripple of the snubber ΔV_{C-RCD}:

$$C_{RCD} = \frac{N_{PS} \times (V_{OUT} + V_{D\_F}) + \Delta V_S}{R_{RCD} f_S \Delta V_{C\_RCD}}$$

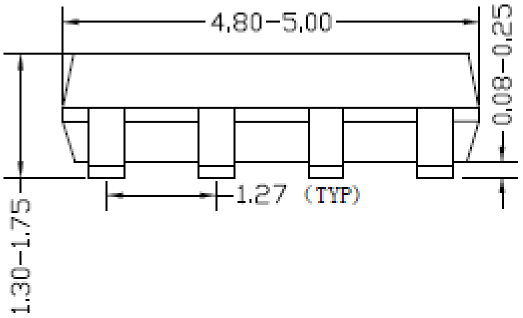
SO8 Package outline & PCB layout design



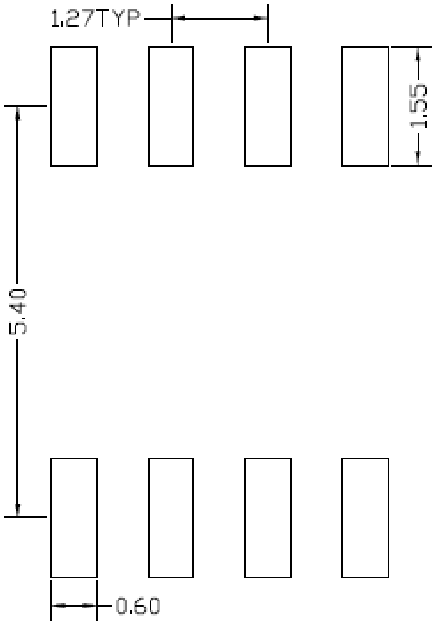
Top view



Side view



Front view

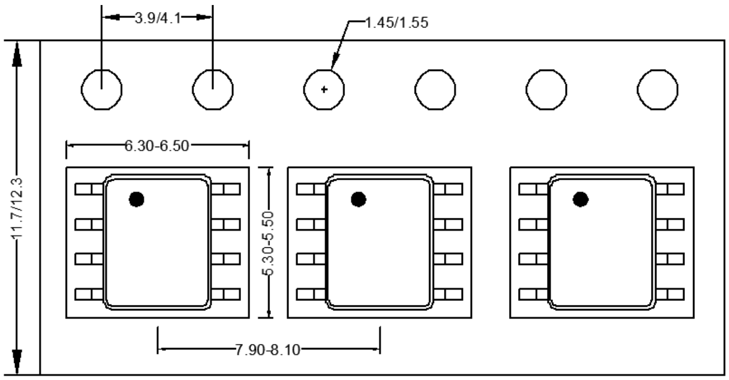


Recommended Pad Layout (Reference only)

Notes: All dimension in millimeter and exclude mold flash & metal burr.

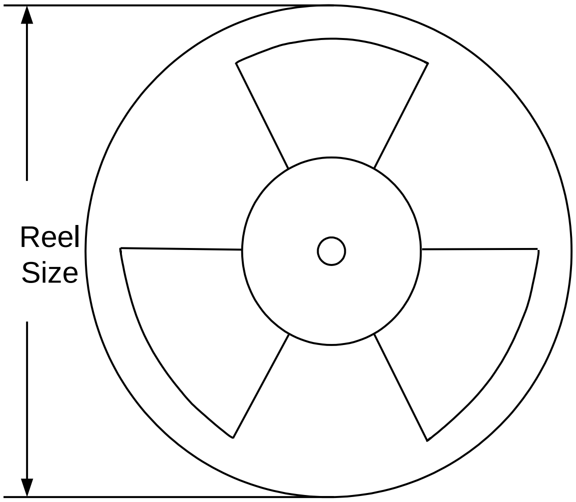
Taping & Reel Specification

1. Taping orientation for packages（SO8）



Feeding direction ⟶

2. Carrier Tape & Reel specification for packages



Package type	Tape width (mm)	Pocket pitch(mm)	Reel size (Inch)	Trailer length(mm)	Leader length (mm)	Qty per reel
SO8	12	8	13"	400	400	2500