SY50186

Single Stage BUCK PFC Constant-Voltage Regulator

General Description

The SY50186 is a single stage high PF Buck regulator, targeting at Constant Voltage (CV) applications. It adopts the proprietary control architecture to achieve accurate output voltage. Quasi-resonant valley turn-on operation and adaptive PWM/PFM control are adopted to achieve high efficiency.

Features

- Integrated 600V MOSFET
- Valley Turn-on to Achieve Low Switching Losses
- Power Factor >0.9 with Single-stage Conversion
- Maximum Switching Frequency Limitation 100kHz
- Compact Package: SO8

Applications

- AC/DC Adapters
- LED Lighting

Ordering Information

SY50186□(□□)□

- Temperature Code
- Package Code
- Optional Spec Code

Ordering Number	Package type	Note
SY50186FAC	SO8	----

Typical Applications

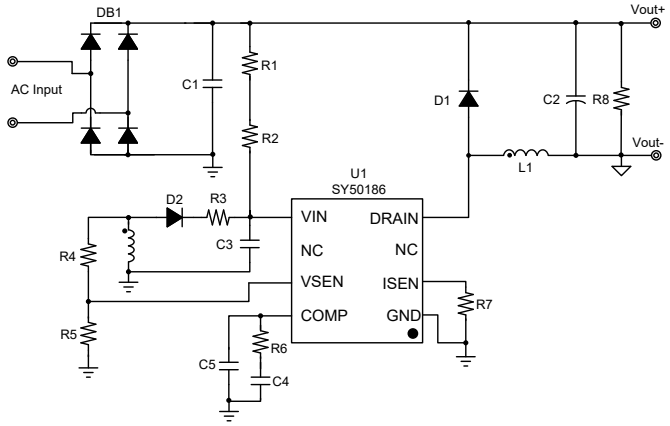


Fig. 1 Schematic Diagram

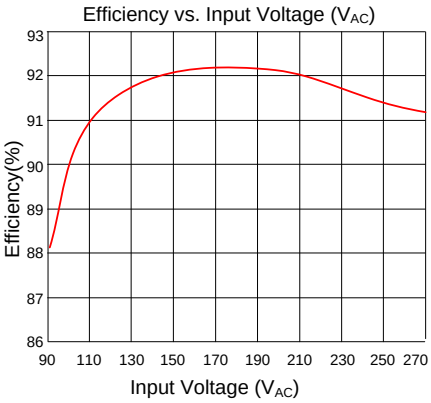
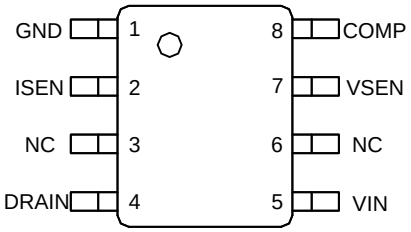


Fig. 2 Efficiency vs Input Voltage

Pinout (top view)



(SO8)

Top Mark: CBQ*xyz* (device code: CBQ, ***x=year code, y=week code, z= lot number code***)

Pin	Name	Description
1	GND	Ground pin.
2	ISEN	Current limit PIN.
3	NC	No connection.
4	DRAIN	Drain PIN of integrated MOSFET.
5	VIN	Power supply pin.
6	NC	No connection.
7	VSEN	Output voltage and inductor current zero detection PIN.
8	COMP	Loop compensation pin. Connect a RC network across this pin and ground.

Block Diagram

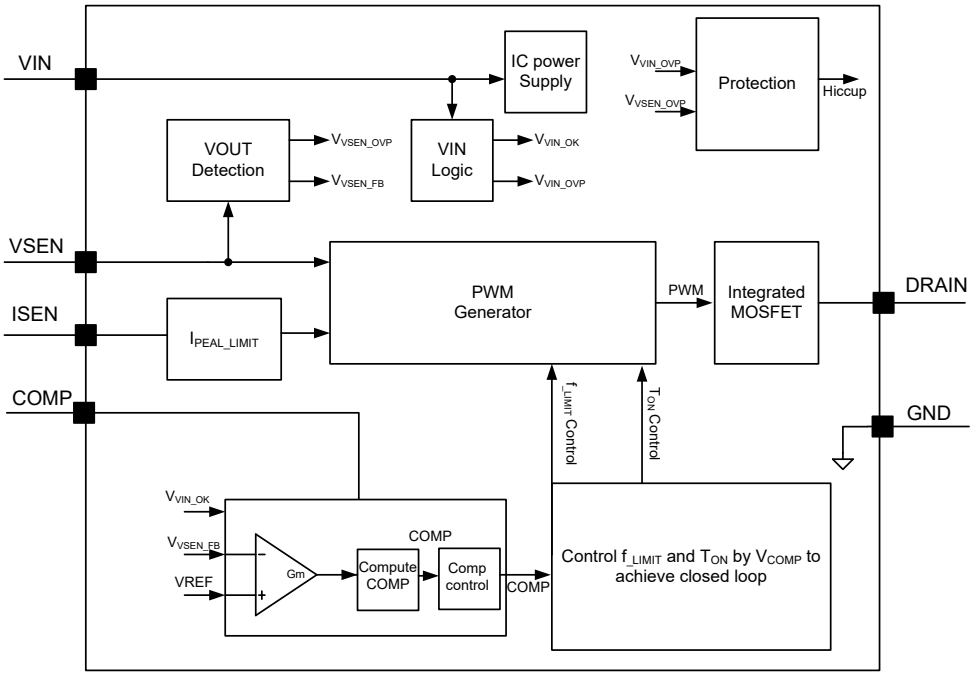


Fig.3 Block Diagram

Absolute Maximum Ratings (Note 1)

VIN---------- -0.3V to 27.0V
DRAIN---------- -0.3V to 600V
Supply current I_{VIN} ---------- 20mA
VSEN ---------- -0.3V to V_{IN}+0.3V
ISEN, COMP ---------- 3.6V
Power Dissipation, @ T_A = 25°C SO8 ---------- 1.1W
Package Thermal Resistance (Note 2)
SO8,θ_{JA}---------- 88°C/W
SO8,θ_{JC} ---------- 45°C/W
Temperature Range ---------- -40°C to 150°C
Lead Temperature (Soldering, 10 sec.) ---------- 260°C
Storage Temperature Range ---------- -65°C to 150°C

Recommended Operating Conditions (Note 3)

VIN----------10V~20V
Junction Temperature Range---------- ---------- -40°C to 125°C

Electrical Characteristics

(V_{IN} = 12V (Note 3), T_A = 25°C unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Power Supply Section						
Input Voltage Range	V_{VIN}		9		22	V
VIN Turn-on Threshold	V_{VIN_ON}		18.5	21.5	23.5	V
VIN Turn-off Threshold	V_{VIN_OFF}		6	7.5	9	V
VIN OVP Voltage	V_{VIN_OVP}		22	24.5	27	V
Start-up Current	I_{ST}	$V_{VIN}<V_{VIN\_OFF}$	1	2	3.5	μA
Operating Current	I_{VIN}			0.45		mA
Shunt Current in OVP Mode	I_{VIN_OVP}	$V_{VIN}>V_{VIN\_OVP}$		15		mA
Quick Start up Section						
Internal Pre-charge Current Source	I_{PRE_CHARGE}	$V_{FB}< V_{FB\_LOW}$		12		μA
Error Amplifier Section						
Current Limit Voltage	V_{ISEN_LIMIT}	$V_{FB}<0.2V$		0.4		V
		$0.2V<V_{FB}<1V$	0.9	1.0	11	V
Over Current Protect Voltage	V_{ISEN_OCP}		1.2	1.5	1.8	V
V_{FB} at End of Fast Start up	V_{FB_LOW}		1.04	1.1	1.14	V
Internal Reference Voltage	V_{FB_REF}		1.225	1.25	1.275	V
V_{FB} for Max off Time Mode	V_{FB_HIGH}		1.33	1.40	1.45	V
OVP Voltage Threshold	V_{FB_OVP}			V_{FB_HIGH}+1		V
Blanking Time for OFF Time	T_{OFF_MIN}	V_{ISEN_HOLD}=0.15V	0.7	1.0	1.3	μs
BV of Integrated MOSFET	V_{DRAIN}		600			V
Rds_on of MOSFET	RDS_ON		1	2	3	Ω
Max ON Time	T_{ON_MAX1}	$1V\leq V_{FB}<1.5V, V_{COMP}$=2.5V	9	16	23	μs
	T_{ON_MAX2}	$V_{FB}<1V$		20		μs
Min ON Time	T_{ON_MIN}		0.3	0.45	0.6	μs
Max OFF Time	T_{OFF_MAX1}	V_{FB}=0	100	132	165	μs
	T_{OFF_MAX2}	$V_{FB} > V_{FB\_HIGH}$	400	525	650	μs
Maximum Switching Frequency	F_{MAX}		80	100	125	kHz
Thermal Section						
Thermal Shutdown Temperature	T_{SD}			155		℃

Note 1: Stresses beyond the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: θ_{JA} is measured in the natural convection at T_A = 25°C on a low effective single layer thermal conductivity test board of JEDEC 51-3 thermal measurement standard. Test condition: Device mounted on 2" x 2" FR-4 substrate PCB, 2oz copper, with minimum recommended pad on top layer and thermal vias to bottom layer ground plane.

Note 3: Increase VIN pin voltage gradually higher than $V_{VIN,ON}$ voltage then turn down to 12V.

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Operation

The SY50186 is a constant voltage Buck regulator targeting at LED lighting applications.

It integrates a MOSFET with 600V breakdown voltage to decrease physical volume.

High power factor is achieved by constant on operation mode, with which the control scheme and the circuit structure are both simple.

Start up process is optimized inside SY50186, and quick start up (less than 500ms) is achieved without any additional circuit.

In order to reduce the switching losses and improve EMI performance, Quasi-Resonant switching mode is applied, which means to turn on the power MOSFET at voltage valley; The start-up current of SY50186 is rather small to reduce the standby power loss further. The maximum switching frequency is clamped to 100kHz to reduce switching losses and improve EMI performance; Specific design is adopted to ensure good performance when transition.

Adaptive PWM/PFM control is adopted for highest average efficiency.

SY50186 provides reliable protections such as Short Circuit Protection (SCP), Open LED Protection (OLP), Over Temperature Protection (OTP), transformer shorted protection and power diode shorted protection, etc.

SY50186 is available with SO8 package.

Applications Information

Start up

After AC supply or DC BUS is powered on, the capacitor C_{VIN} across VIN and GND pin is charged up by BUS voltage through a start up resistor R_{ST}. Once V_{VIN} rises up to V_{VIN_ON}, the internal blocks start to work. V_{VIN} will be pulled down by internal consumption of IC until the auxiliary winding of Buck transformer could supply enough energy to maintain V_{VIN} above V_{VIN_OFF}.

The whole start up procedure is divided into two sections shown in Fig.4. t_{STC} is the C_{VIN} charged up section, and t_{STO} is the output voltage built-up section. The start-up time t_{ST} composes of t_{STC} and t_{STO}, and usually t_{STO} is much smaller than t_{STC}.

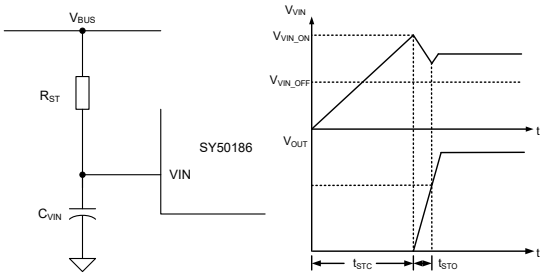


Fig.4 Start up

The start-up resistor R_{ST} and C_{VIN} are designed by rules below:

(a) Preset start-up resistor R_{ST}, make sure that the current through R_{ST} is larger than I_{ST} and smaller than I_{VIN_OVP}

$$\frac{V_{BUS}}{I_{VIN\_OVP}} < R_{ST} < \frac{V_{BUS}}{I_{ST}}$$

Where V_{BUS} is the BUS line voltage.

(b) Select C_{VIN} to obtain an ideal start up time t_{ST}, and ensure the output voltage is built up at one time.

$$C_{VIN} = \frac{(\frac{V_{BUS}}{R_{ST}} - I_{ST}) \times t_{ST}}{V_{VIN\_ON}}$$

(c) If the C_{VIN} is not big enough to build up the output voltage at one time. Increase C_{VIN} and decrease R_{ST}, go back to step (a) and re-do such design flow until the ideal start up procedure is obtained.

Internal Pre-charge Design for Quick Start up

After V_{VIN} exceeds V_{VIN_ON}, PWM output is enabled. If V_{FB} is lower than certain threshold V_{FB_LOW}, V_{COMP} is pre-charged by the internal current source I_{PRE_CHARGE}, so the output voltage can be built up quickly.

When V_{FB}<0.2V, V_{ISEN} will be limited at 0.4V, when 1.0V ≥V_{FB}≥0.2V, V_{ISEN} will be limited at 1.0V.

The V_{COMP_INT} in start-up procedure can be programmed by R_{COMP}:

$$V_{COMP\_INT} = I_{PRE\_CHARGE} \times R_{COMP}$$

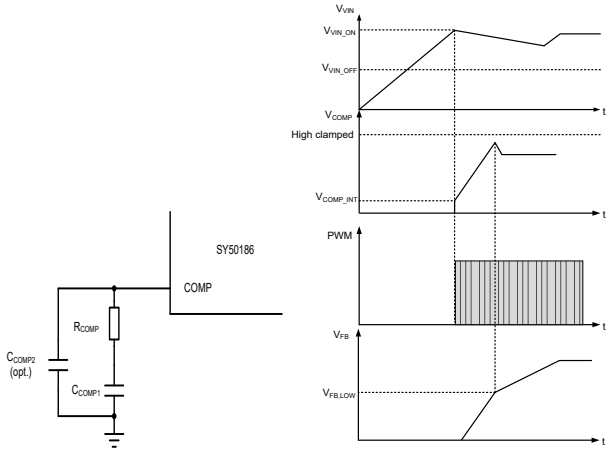


Fig.5 Pre-charge scheme in start up

Once V_{FB} is over V_{FB_LOW}, I_{PRE_CHARGE} is quit and V_{COMP} is under charged of the internal gain modulator. The quick start up process is finished.

Shut down

After AC supply or DC BUS is powered off, the energy stored in the BUS capacitor will be discharged. When the auxiliary winding of Buck transformer cannot supply enough energy to VIN pin, V_{VIN} will drop down. Once V_{VIN} is below V_{VIN_OFF}, the IC will stop working and V_{COMP} will be discharged to zero.

Quasi-Resonant Operation

QR mode operation provides low turn-on switching losses for Buck converter.

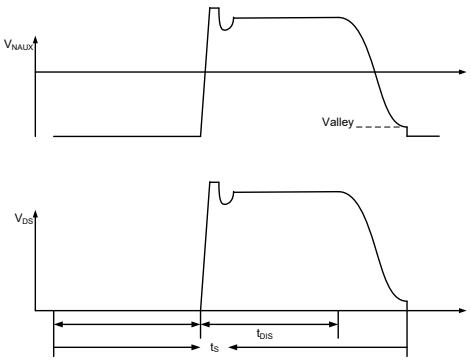


Fig. 6 QR mode operation

The voltage across drain and source of the MOSFET is reflected by the auxiliary winding of the Buck transformer. VSEN pin detects the voltage across the auxiliary winding by a resistor divider. When the voltage across drain and source of the primary MOSFET is at voltage valley, the MOSFET would be turned on.

Output Voltage Control

In order to achieve constant voltage control, the output voltage is detected by the auxiliary winding voltage.

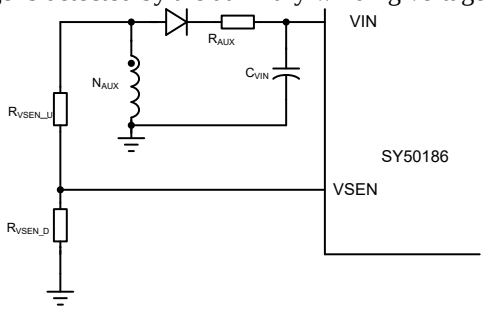


Fig. 7 VSEN pin connection

As shown in Fig.7, during OFF time, the voltage across the auxiliary winding is

$$V_{AUX} = (V_{OUT} + V_{D,F}) \times \frac{N_{AUX}}{N_S}$$

N_{AUX} is the turns of auxiliary winding; N_S is the turns of main winding; $V_{D,F}$ is the forward voltage of the power diode.

At the current zero-crossing point, $V_{D,F}$ is nearly zero, so V_{OUT} is proportional with V_{AUX} exactly. The voltage of this point is sampled by the IC as the feedback of output voltage. The resistor divider is designed by

$$V_{OUT} = \frac{V_{FB\_REF}}{\frac{R_{VSEN\_D}}{R_{VSEN\_U} + R_{VSEN\_D}} \times \frac{N_{AUX}}{N_S}}$$

Where V_{FB_REF} is the internal voltage reference.

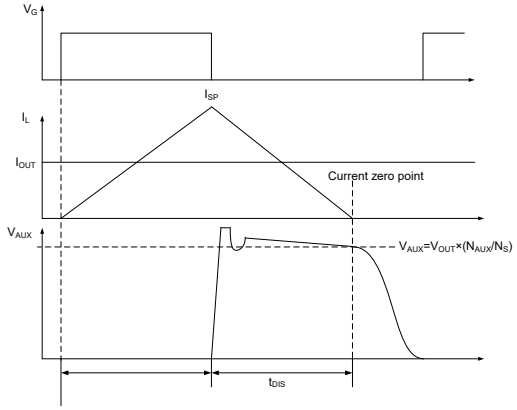


Fig.8 Auxiliary winding voltage waveforms

Special Design for Transition

To have good transition performance, special design is integrated into SY50186.

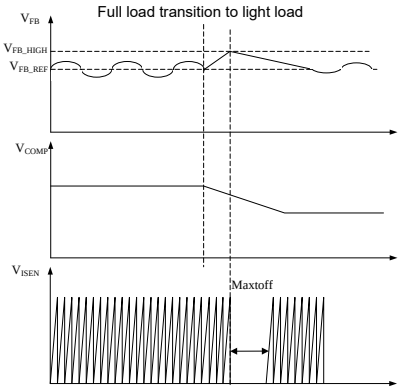


Fig.9 Full load transition to light load

When V_{FB} touch V_{FB_HIGH}, IC work at Max toff mode to decrease output energy, and COMP is pulled down to decrease the energy output.

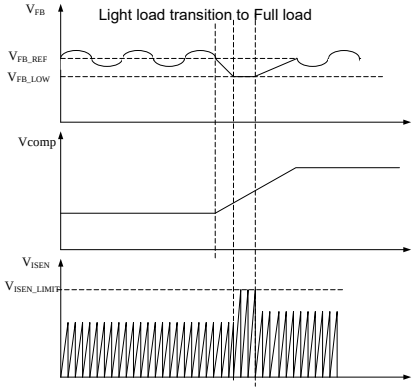


Fig.10 Light load transition to full load

When V_{FB} < 1V, IC work at Max Ipeak to expedite output energy, and COMP is charged by internal current source I_{PRE_CHARGE} to increase the energy output when V_{FB} < V_{FB_LOW}.

Design of R_{ISEN}

The maximum power inductor current ($I_{P\_PK\_MAX}$) occur in peak of input voltage when full load. So R_{ISEN} could be selected by:

$$R_{ISEN} = \frac{90\% \times V_{ISEN,LIMIT}}{I_{P\_PK\_MAX}}$$

Where V_{ISEN_LIMIT} is a protection for core saturation (If V_{ISEN} touch this voltage, gate will turn off), and $I_{P\_PK\_MAX}$ is the maximum power inductor in steady.

Short Circuit Protection (SCP)

When the output is shorted to ground, the output voltage is clamped to zero. The voltage of the auxiliary winding is proportional to the output winding, so valley signal cannot be detected by VSEN. Without valley detection, MOSFET cannot be turned ON until maximum off time t_{OFF_MAX1} is matched. If MOSFET is turned on by t_{OFF_MAX1} 64 times continuously, IC will be shut down and enter into hiccup mode.

Single Fault Design

If VSEN pin is shorted to GND pin or floating, valley detection is failed, which is similar to SLP, the system will operate in hiccup mode.

If the transformer is shorted, V_{ISEN} will exceeds $V_{ISEN,EX}$, which will trigger IC hiccup operation. The protection above is also suitable for secondary diode short.

Power Device Design

MOSFET and Diode

When the operation condition is with maximum input voltage and full load, the voltage stress of MOSFET and output power diode is maximized;

$$V_{MOS\_DS\_MAX} = \sqrt{2} V_{AC\_MAX}$$

$$V_{D\_R\_MAX} = \sqrt{2} V_{AC\_MAX}$$

Where V_{AC_MAX} is maximum input AC RMS voltage.
When the operation condition is with minimum input voltage and full load, the current stress of MOSFET and power diode is maximized.

Inductor (L)

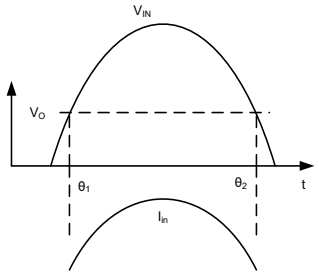


Fig.11 Input waveforms

The power is transferred from AC input to output only when the input voltage is higher than output voltage in Buck converter. The input voltage and inductor current waveforms are shown in Fig.11, where θ_1 and θ_2 are the time that input voltage is equal to output voltage.

In Quasi-Resonant mode, each switching period cycle t_S consists of three parts: current rising time t_1, current falling time t_2 and quasi-resonant time t_3 shown in Fig.12.

The system operates in the constant on time mode to achieve high power factor. The ON time increases with the input AC RMS voltage decreasing and the load increasing. When the operation condition is with minimum input AC RMS voltage and full load, the ON time is maximized. On the other hand, when the input voltage is at the peak value, the OFF time is maximized. Thus, the minimum switching frequency f_{S_MIN} happens at the peak value of input voltage with minimum input AC RMS voltage and maximum load condition; meanwhile, the maximum peak current through MOSFET and the transformer happens.

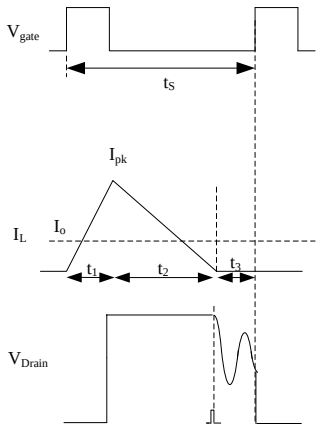


Fig.12 switching waveforms

Once the minimum frequency f_{S_MIN} is set, the inductance of the transformer could be calculated. The design flow is shown as below:

(a) Preset minimum frequency f_{S_MIN}

(b) Compute relative t_S, t_1

$$t_S = \frac{1}{f_{S\_MIN}}$$

$$t_1 = \frac{t_S \times (V_{OUT} + V_{DF})}{(\sqrt{2}V_{AC\_MIN} + V_{DF})}$$

$$t_2 = t_S - t_1$$

Where V_{DF} is the forward voltage of the diode.

(c) Design inductance L

$$\theta_1 = \arcsin\left(\frac{V_{OUT}}{\sqrt{2}V_{AC\_MIN}}\right) \times \frac{1}{\pi} \times \frac{1}{2 \times f_{AC}}$$

$$\theta_2 = \frac{1}{2 \times f_{AC}} - \theta_1$$

$$L = \frac{\eta \times f_{AC} \times V_{OUT} \times t_1}{P_{OUT}} \times \left[\sqrt{2}V_{AC\_MIN} \times \frac{\cos(2\pi f_{AC} \times \theta_1) - \cos(2\pi f_{AC} \times \theta_2)}{2\pi f_{AC}} - V_{OUT}(\theta_2 - \theta_1)\right]$$

Where η is the efficiency; P_{OUT} is rated full load power;

(d) Compute inductor maximum peak current $I_{L\_PK\_MAX}$.

$$I_{L\_PK\_MAX} = \frac{(\sqrt{2}V_{AC\_MIN} - V_{OUT}) \times t_1}{L}$$

Where $I_{L\_PK\_MAX}$ is the maximum inductor peak current;

(e) Compute the RMS current of Buck inductor

$I_{L\_RMS\_MAX}$ is inductor RMS current of whole AC period

$$I_{L\_RMS\_MAX} = \frac{t_1}{\sqrt{3} \times L}\sqrt{V_{AC\_MIN}^{\ 2} + V_{OUT}^{\ 2} - \frac{4\sqrt{2}V_{AC\_MIN} \times V_{OUT}}{\pi}}$$

(f) Compute RMS current of the MOSFET

$$I_{L\_RMS\_MAX} = \sqrt{\frac{t_1}{3t_S}} \times \frac{t_1}{L}\sqrt{V_{AC\_MIN}^{\ 2} + V_{OUT}^{\ 2} - \frac{4\sqrt{2}V_{AC\_MIN} \times V_{OUT}}{\pi}}$$

Inductor Design (N, N_{AUX})

These parameters below are necessary:

Necessary parameters	
Inductance	L
inductor maximum current	$I_{L\_PK\_MAX}$
inductor maximum RMS current	$I_{L\_RMS\_MAX}$

The design rules are as followed:

(a) Select the magnetic core style, identify the effective area A_e.

(b) Preset the maximum magnetic flux ΔB

ΔB=0.22~0.26T

(c) Compute the turns N

$$N = \frac{L_M \times I_{L\_PK\_MAX}}{\Delta B \times A_e}$$

(d) Compute the auxiliary turns N_{AUX}

$$N_{AUX} = N \times \frac{V_{VIN}}{V_{OUT}}$$

Where V_{VIN} is the working voltage of VIN pin (10V~20V is recommended).

(e) Select an appropriate wire diameter

With $I_{L\_RMS\_MAX}$, select appropriate wire to make sure the current density ranges from 4A/mm^2 to 10A/mm^2.

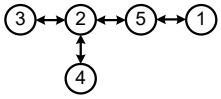
(f) If the winding area of the core and bobbin is not enough, reselect the core style, go to **(a)** and redesign the transformer until the ideal transformer is achieved.

Layout

(a) To achieve better EMI performance and reduce line frequency ripples, the output of the bridge rectifier should be connected to the BUS line capacitor first, then to the switching circuit.

(b) The circuit loop of all switching circuit should be kept small.

(c) The connection of ground is recommended as:



Ground ①: ground of BUS line capacitor
Ground ②: ground of bias supply capacitor and GND pin
Ground ③: ground node of auxiliary winding
Ground ④: ground of signal trace except GND pin
Ground ⑤: ground node of current sample resistor.

(d) Bias supply trace should be connected to the bias supply capacitor first instead of GND pin. The bias supply capacitor should be put beside the IC.

(e) Loop of ′Source pin – current sample resistor – GND pin′ should be kept as small as possible.

(f) The resistor divider connected to ZCS pin is recommended to be put beside the IC.

(g) The control circuit is recommended to be put outside the power circuit loop.

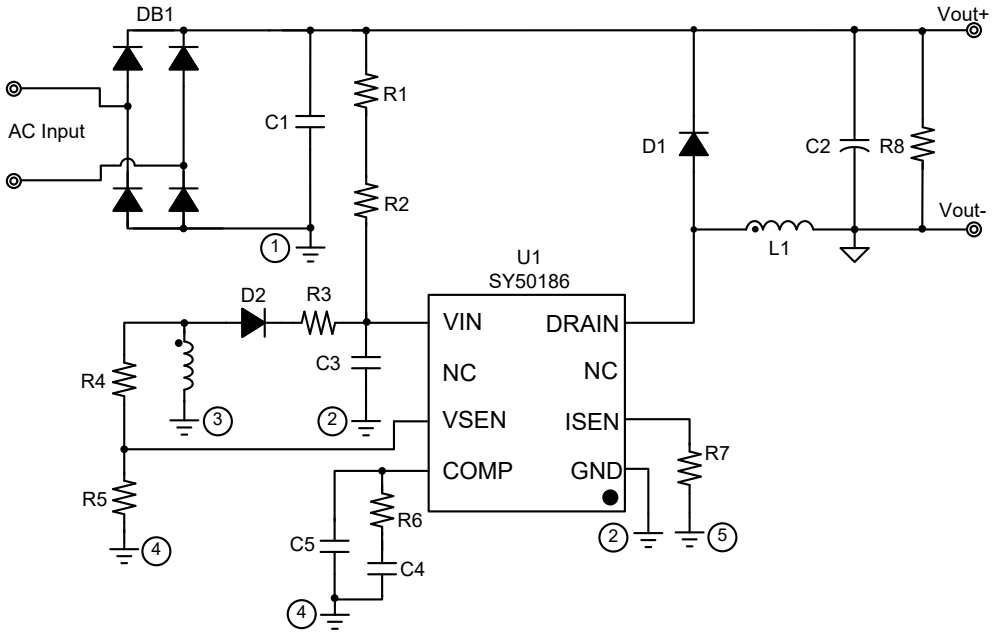
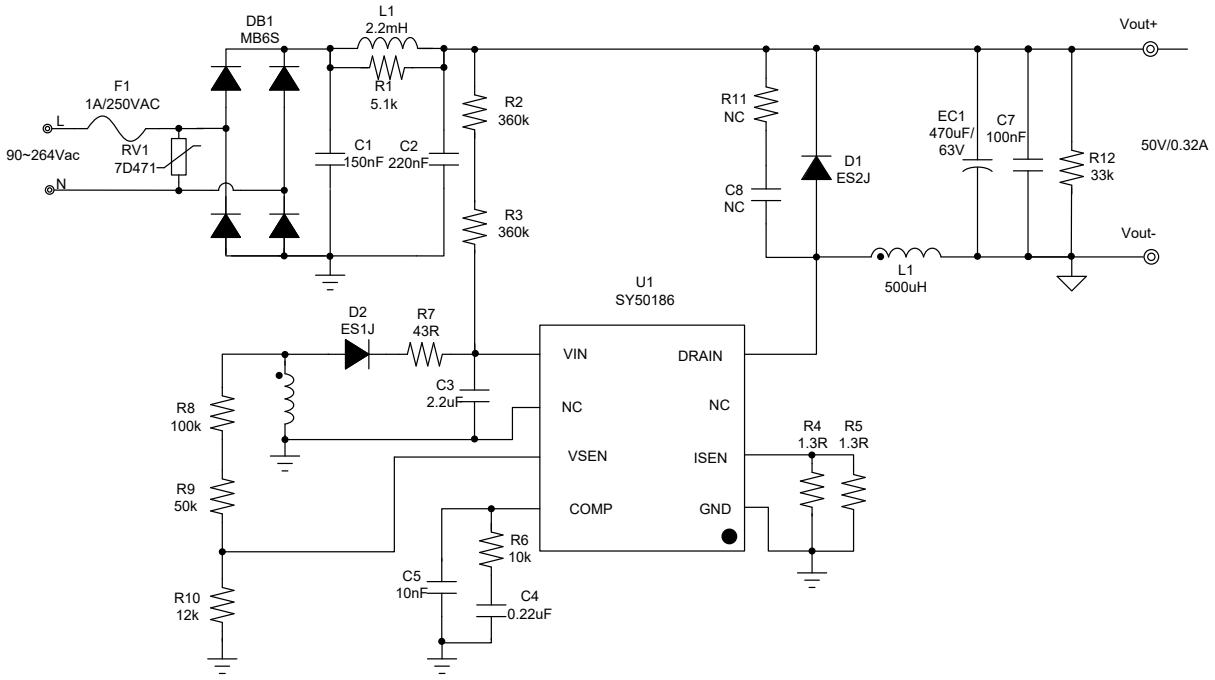
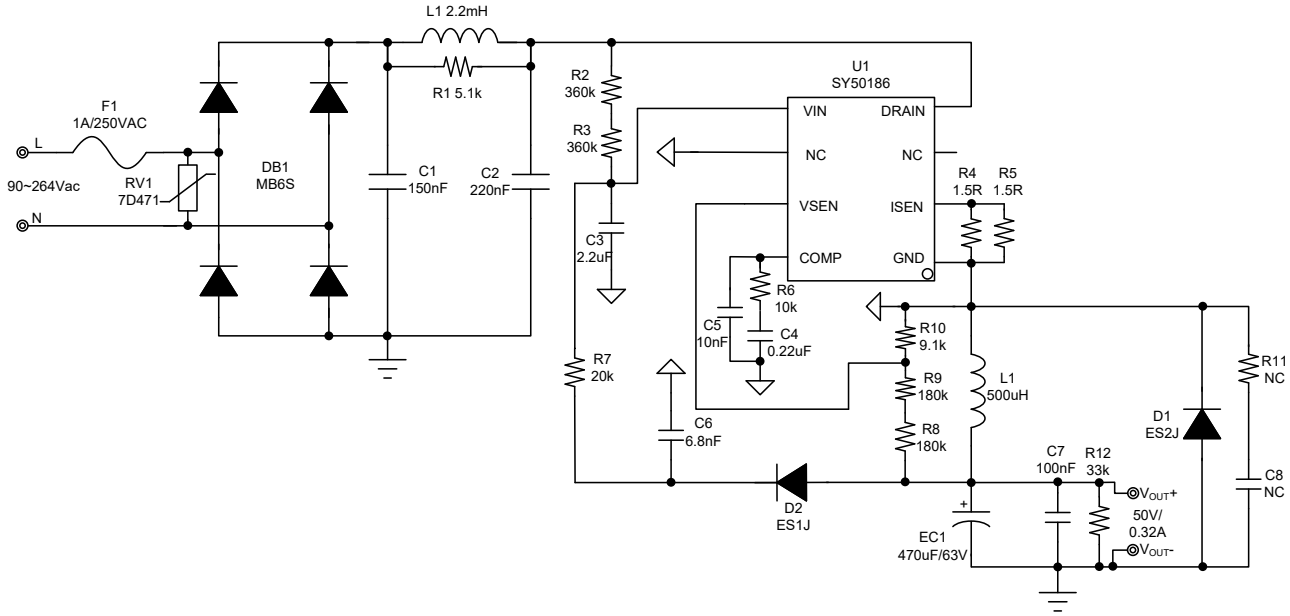


Fig.13 Recommended connection of GND

Typical Application



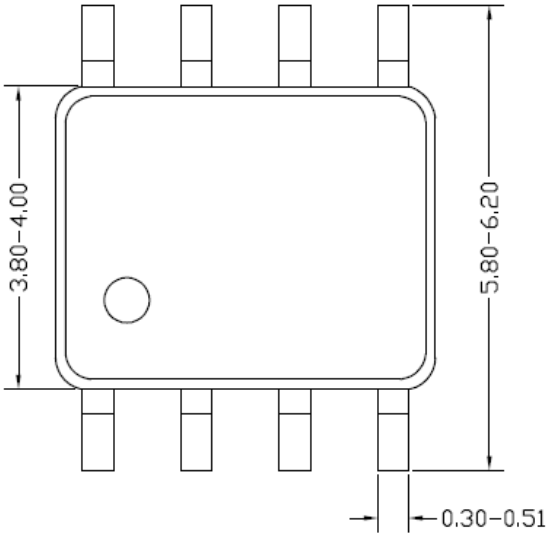
(a) Ground-switch Buck circuit @ 90~264Vac Input, 50V/0.32A Output



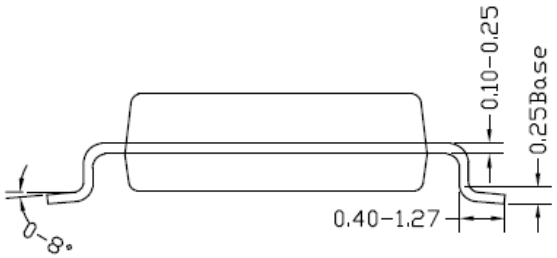
(b) Floating-switch Buck circuit @ 90~264Vac Input, 50V/0.32A Output

Fig.14 Typical Application Circuit

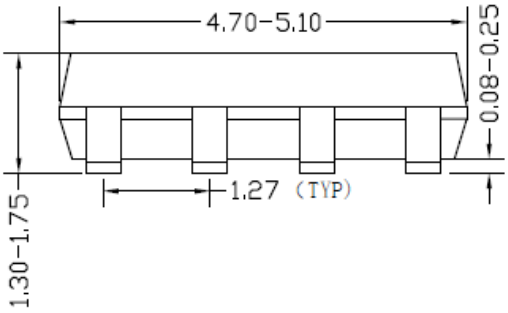
SO8 Package Outline & PCB Layout Design



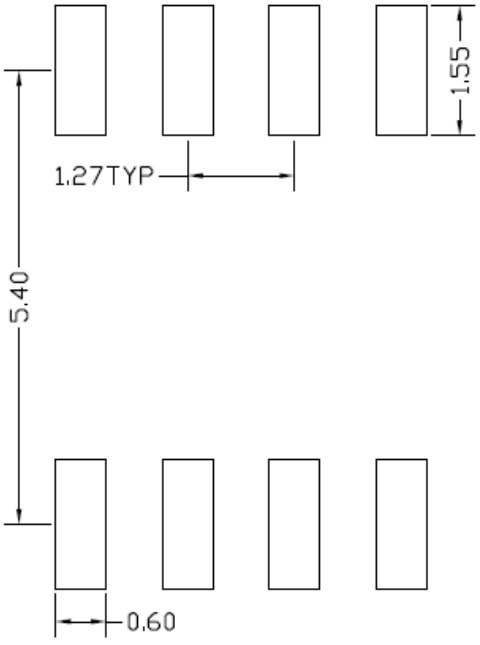
Top view



Side view



Front view

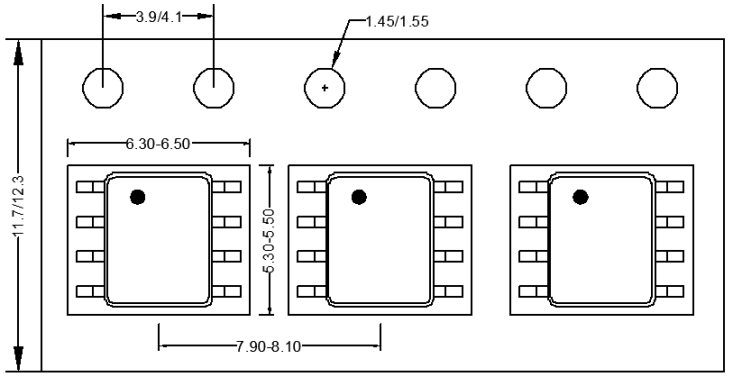


Recommended Pad Layout (Reference only)

Notes: **All dimension in millimeter and exclude mold flash & metal burr.**

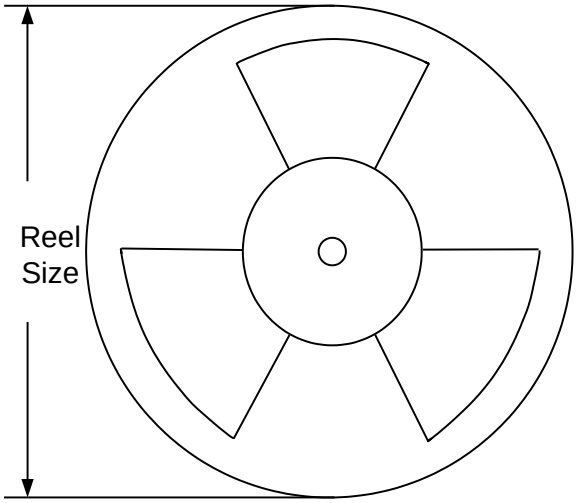
Taping & Reel Specification

1. Taping orientation for packages（SO8）



Feeding direction ⟶

2. Carrier Tape & Reel specification for packages



Package type	Tape width (mm)	Pocket pitch(mm)	Reel size (Inch)	Trailer length(mm)	Leader length (mm)	Qty per reel
SO8	12	8	13"	400	400	2500

Revision History

The revision history provided is for informational purpose only and is believed to be accurate, however, not warranted. Please make sure that you have the latest revision.

Date	Revision	Change
January 8,2021	Revision 0.9	Initial Release

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