# SY6884

## Programmable High Current Overvoltage Protection Switch

## General Description

SY6884 is a programmable over voltage protection switch with 5A current capability to prevent damage to the downstream system with low voltage rating. It achieves wide input voltage range from 2.5$V_{DC}$ to 25$V_{DC}$. Extremely low power path on resistance $R_{PWPT}$ helps to reduce power loss during the normal operation. It integrates the over-temperature protection and auto-recovery with hysteresis to protect against over current events. This IC along with small CSP (0.89mm×1.43mm) footprint provides small PCB area application.

## Features

- $V_{IN}$=2.5V to 25V, Absolute Maximum $V_{IN}$=28V
- Extremely Low Power Path on Resistance $R_{PWPT}$: 30mΩ Typ.
- Fast OVP Response Time: 100 ns.
- Auto-enabled Switch with 15ms Debounce Time
- Programmable Over Voltage Threshold From +4V to +20V
- Internal Soft-start to Prevent Inrush Current
- Thermal Shutdown Protection & Auto Recovery
- Short Circuit Protection
- Compact Package: CSP 0.89×1.43-6

## Ordering Information

SY6884 □(□□)□
- Temperature Code
- Package Code
- Optional Spec Code

| Ordering Number | Package Type | Note |
|---|---|---|
| SY6884PYC | CSP0.89×1.43-6 | |

## Applications

- Smart Phone
- Tablet PCs
- Mobile Device

## Typical Applications

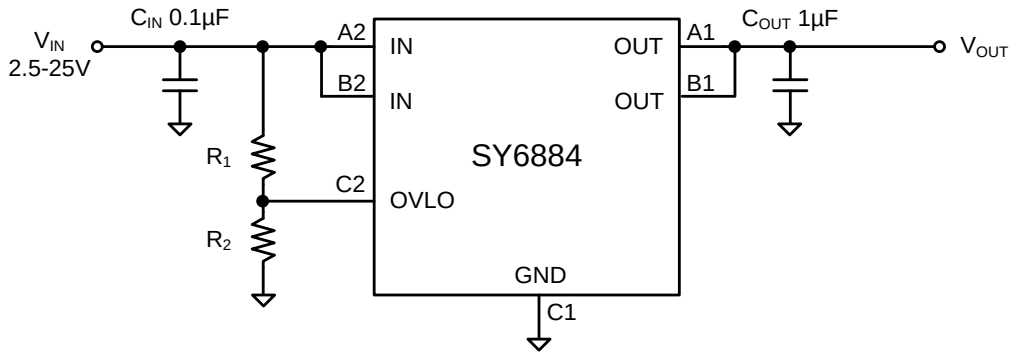
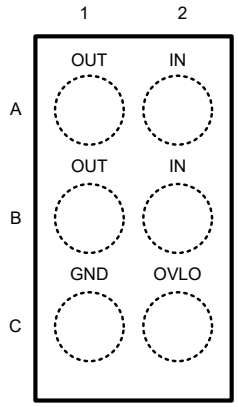



Figure1. Schematic Diagram

## Pinout (top view)




(CSP0.89×1.43-6)

Top Mark: **cE*xyz***, **(**Device code: cE; ***x=year code, y=week code, z= lot number code*****)**

| Pin Name | Pin Number | Pin Description |
|---|---|---|
| IN | A2, B2 | Power input pin. Connect IN pins together. Decouple high frequency noise by connecting at least a 0.1μF MLCC to ground. |
| OUT | A1, B1 | Output voltage pin. Source side of the internal FET. Connect OUT pins together for normal operation. |
| OVLO | C2 | External OVLO program pin. Connect resistor divider to this pin to program the OVLO threshold. Make sure $V_{OVLO}$ is higher than external OVLO select threshold 0.28V; otherwise the internal default OVP threshold 6.75V (typ.) is active. Pull down this pin to ground to disable external program function. |
| GND | C1 | Power ground pin. |

## Block Diagram

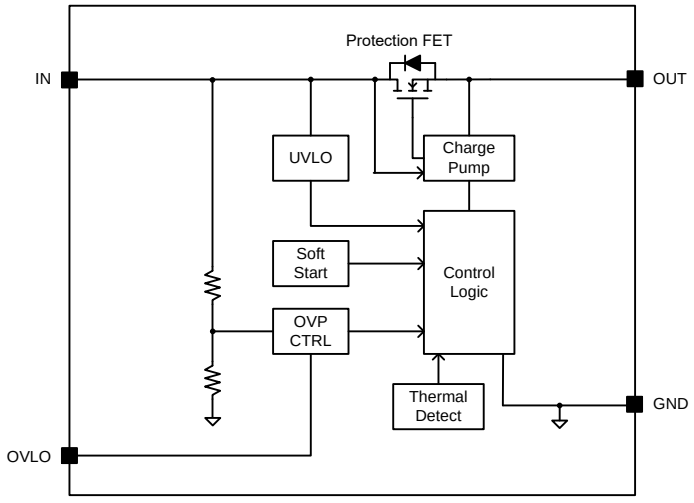



Figure2. Block Diagram

## Absolute Maximum Ratings (Note 1)

IN ---------- -0.3 to 28V
OUT ---------- -0.3 to IN + 0.3V
OVLO ---------- -0.3 to 28V
Continues IN, OUT Current ---------- 5 A
Power Dissipation, $P_D$ @ $T_A$ = 25°C CSP ---------- 1.1W
Package Thermal Resistance (Note 2)
$\theta_{JA}$ ---------- 91.1°C/W
$\theta_{JC}$ ---------- 35.5°C/W
Junction Temperature Range ---------- 150°C
Lead Temperature (Soldering, 10 sec.) ---------- 260°C
Storage Temperature Range ---------- -65°C to 150°C

## Recommended Operating Conditions (Note 3)

IN ---------- 2.5 to 25V
OUT ---------- 0 to 25V
OVLO ---------- 0 to 25V
Junction Temperature Range ---------- -40°C to 125°C
Ambient Temperature Range ---------- -40°C to 85°C

# Electrical Characteristics

($V_{IN}$ = 2.5V to 25V, $C_{IN}$=1μF, $C_{OUT}$=1μF, $T_A$ = 25°C, unless otherwise specified.)

| Parameter | Symbol | Test Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Input Voltage Range | $V_{IN}$ | | 2.5 | | 25 | V |
| Input UVLO Rising Threshold | $V_{UVLO}$ | | | | 2.45 | V |
| UVLO Hysteresis | $V_{HYS}$ | | | 0.15 | | V |
| Bias Current | $I_{BIAS}$ | $V_{IN}$=5V,$V_{IN}$<$V_{IN\_OVLO}$ | | 110 | | μA |
| OVLO Input Leakage Current | $I_{OVLO}$ | $V_{OVLO}$= $V_{OVLO\_TH}$ | -100 | | 100 | nA |
| Internal Default OVP threshold | $V_{OV\_INTL}$ | $V_{OVLO}$=0V, $V_{IN}$ rising | 6.5 | 6.75 | 7.0 | V |
| Internal Default OVP Hysteresis | $V_{OV\_HYS}$ | $V_{OVLO}$=0V, $V_{IN}$ falling | | 0.2 | | V |
| OVLO Preset Threshold | $V_{OVLO\_TH}$ | $V_{IN}$=5V,$V_{OVLO}$ rising | 1.14 | 1.20 | 1.26 | V |
| External OVLO Select Threshold | $V_{OVLO\_SEL}$ | $V_{IN}$=8V, $V_{OVLO}$ falling | | 0.2 | 0.28 | V |
| Programmable OVLO Range | $V_{OV\_EXTNL}$ | | 4 | | 20 | V |
| On Resistance of Power Path | $R_{PWPT}$ | $V_{IN}$=5V, $I_{OUT}$=500mA, from IN to OUT | | 30 | 39 | mΩ |
| Debounce Time | $t_{DEB}$ | Time from 2.5V<$V_{IN}$<$V_{IN\_OVLO}$ to $V_{OUT}$=10% of $V_{IN}$ | | 15 | | ms |
| Switch Turn-On Time | $t_{ON}$ | $V_{IN}$=5V, $R_L$=100, $C_{OUT}$=100μF; $V_{OUT}$=10% of $V_{IN}$ to 90% of $V_{IN}$ | | 245 | | μs |
| Switch Turn-Off Time | $t_{OFF}$ | $V_{IN}$> $V_{IN\_OVLO}$ to $V_{OUT}$ stop rising | | 100 | | ns |
| Thermal Shutdown Temperature | $T_{SD}$ | | | 150 | | °C |
| Thermal Shutdown Hysteresis | $T_{HYS}$ | | | 20 | | °C |

**Note 1**: Stresses beyond the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

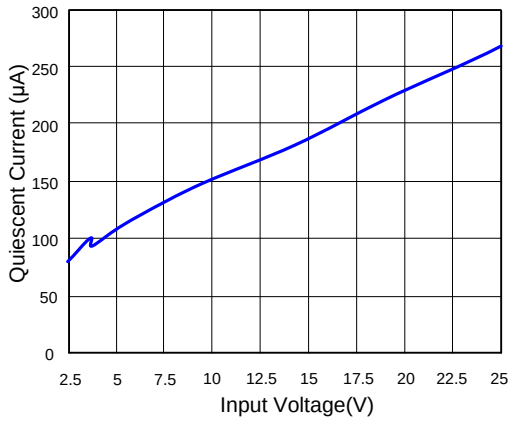
**Note 2**: $\theta_{JA}$ is measured in the natural convection at $T_A$ = 25°C on a Silergy's test board.

**Note 3:** The device is not guaranteed to function outside its operating conditions.

**Note 4:** R1=1MΩ is a good starting value for minimum current consumption. Since $V_{IN\_OVLO}$, $V_{OVLO\_TH}$, and R1 are known, R2 can be calculated from the following formula:
$V_{IN\_OVLO}=V_{OVLO\_TH} \times (1+R1/R2) = 1.2V \times (1+R1/R2)$

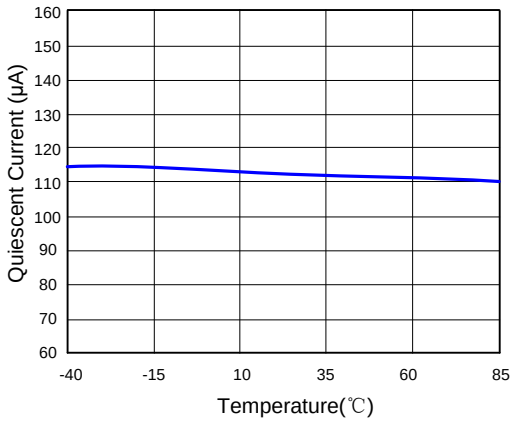
# Typical Performance Characteristic

Quiescent Current vs. Input Voltage



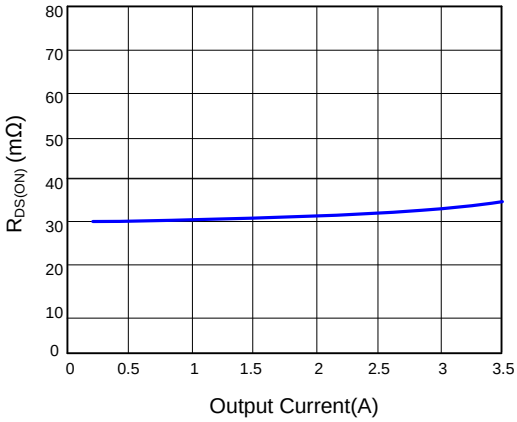

Quiescent Current vs Temperature

($V_{IN}$=5V, $C_{IN}$=$C_{OUT}$=1μF)



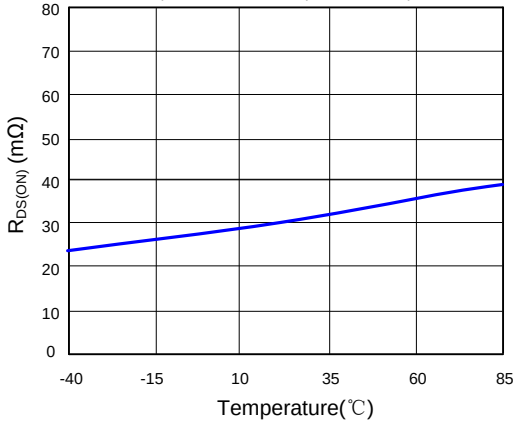

$R_{DS(ON)}$ vs. Output Current

($V_{IN}$=5V, $C_{IN}$=$C_{OUT}$=1μF)



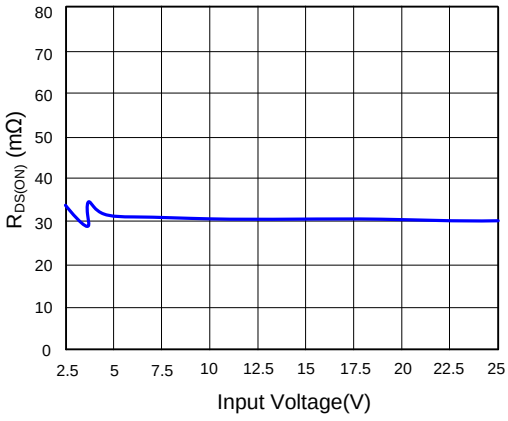

$R_{DS(ON)}$ vs. Temperature

($V_{IN}$=5V, $C_{IN}$=$C_{OUT}$=1μF, $I_{LOAD}$=0.5A)



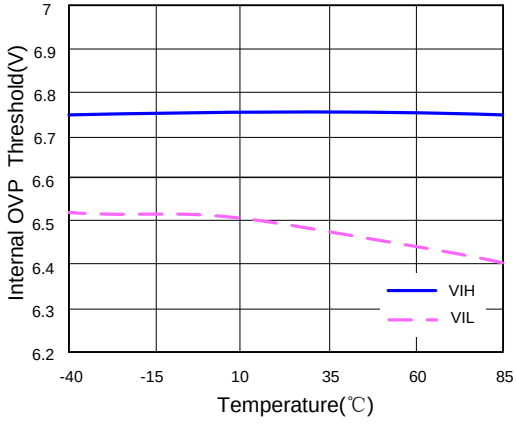

$R_{DS(ON)}$ vs. Input Voltage

($C_{IN}$=$C_{OUT}$=1μF, $I_{LOAD}$=0.5A)



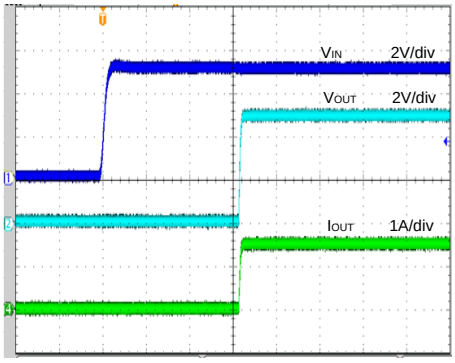

Internal OVP Threshold vs Temperature

($C_{IN}$=$C_{OUT}$=1μF, $V_{OVLD}$=0V)



Startup From $V_{IN}$

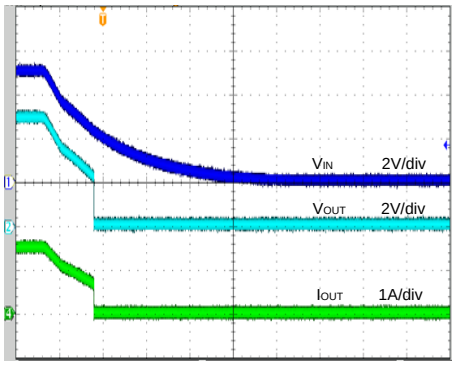
($V_{IN}$=5V, $C_{IN}$=$C_{OUT}$=1μF, 3.3Ω Load)




Time (4ms/div)

Shutdown From $V_{IN}$

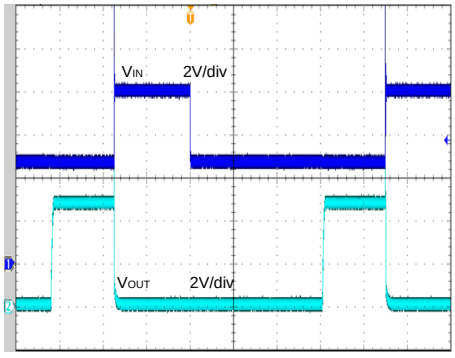
($V_{IN}$=5V, $C_{IN}$=$C_{OUT}$=1μF, 3.3Ω Load)




Time (4ms/div)

OVP and Recovery

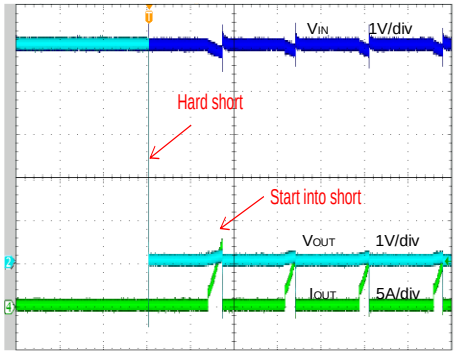
($V_{IN}$=5 to 8V, $V_{OVLO}$=0V, $C_{IN}$=$C_{OUT}$=1μF, 100Ω Load)




Time (4ms/div)

Short Circuit Response

($V_{IN}$=5V, $C_{IN}$=$C_{OUT}$=1μF)




Time (10ms/div)

## Timing Diagram

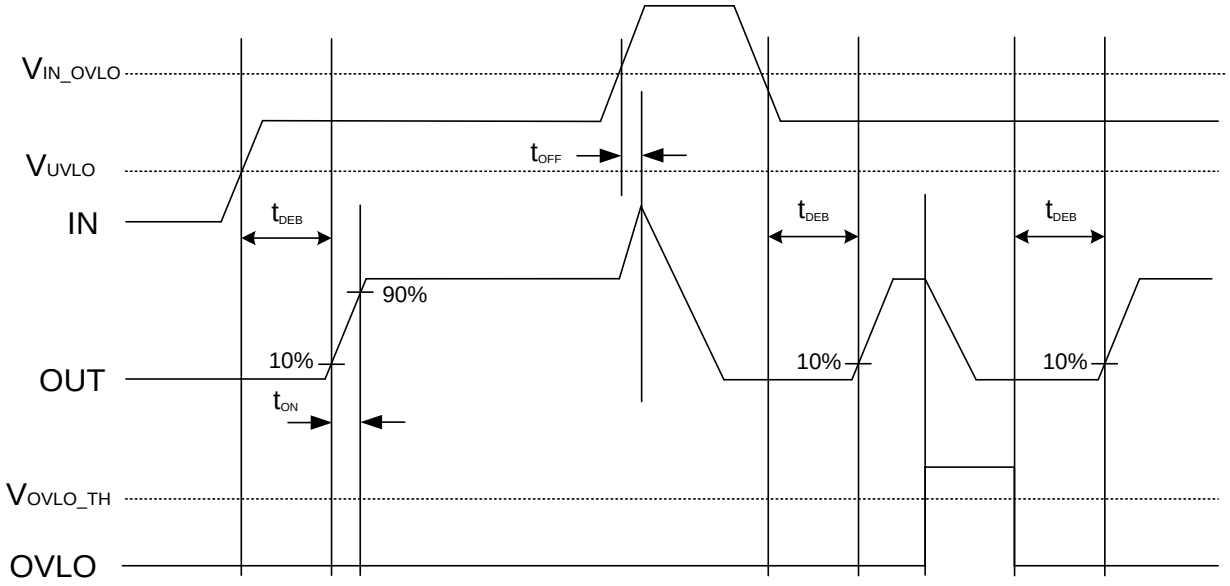



Figure3. Timing Diagram

# Applications Information

The SY6884 is a programmable over voltage protection switch designed for preventing damage to the downstream system with low voltage rating. If power dissipation causes the chip temperature to exceed its maximum temperature setting, and the over-temperature protection will shut down the device. Once the chip temperature drops below the hysteresis temperature, SY6884 will restart.

**Over Voltage Lockout Protection**

When the OVLO input is set below the external OVLO select voltage, the SY6884 automatically chooses the internal fixed OVLO threshold, preset to 6.75V(typ). In the event that an external resistor-divider is connected to OVLO and $V_{OVLO}$ exceeds the OVLO select voltage($V_{OVLO\_SEL}$), the internal OVLO comparator reads the IN fraction fixed by the external resistor divider.

R1=1MΩ is a good starting value for minimum current consumption. Since $V_{IN\_OVLO}$, $V_{OVLO\_TH}$, and R1 are known. R2 can be calculated from the following formula:

$$V_{IN\_OVLO} = V_{OVLO\_TH} \times \left(1+\frac{R1}{R2}\right) = 1.2 \times \left(1+\frac{R1}{R2}\right)$$

The Over-voltage protection threshold can be adjusted with optional resistor divider to a voltage between 4V and 20V.

**On-The-Go(OTG) Functionality**

During OTG operation, the SY6884 is initially disabled and the power FET's bulk diode is forward biased. The bulk diode represents ~0.7V drop across the device, which remains until the input voltage increases past 2.5V, when the device is fully enabled. While the device is disabled and the body diode is forward biased, the max DC current through the diode is 1.5A. This current is limited by the thermal performance of the device (0.7V×1.5A=1.05W). This current should be transient. The transient should not exceed the RC time constant of the input and output capacitors.

**Supply Filter Capacitor**

A 0.1μF or larger input ceramic capacitor is strongly recommended to be placed close to the IC. Furthermore, an output short will cause ringing on the input without the input capacitor. It could destroy the internal circuitry when the input transient exceeds the absolute maximum supply voltage even for a short duration.

**Output Filter Capacitor**

A 1μF output ceramic capacitor is recommended to be placed close to the IC and output connector to reduce voltage drop during load transient. Higher values of output capacitor can be used to further reduce the drop during high current application.

**PCB Layout Guide**

For best performance of the SY6884, the following guidelines must be strictly followed:

1. Keep all VBUS traces as short and wide as possible and use at least 2 ounce copper for all VBUS traces.

2. Locate the output capacitor as close to the connectors as possible to lower impedance (mainly inductance) between the port and the capacitor and improve transient performance.

3. Input and output capacitors should be placed closed to the IC and connected to ground plane to reduce noise coupling.

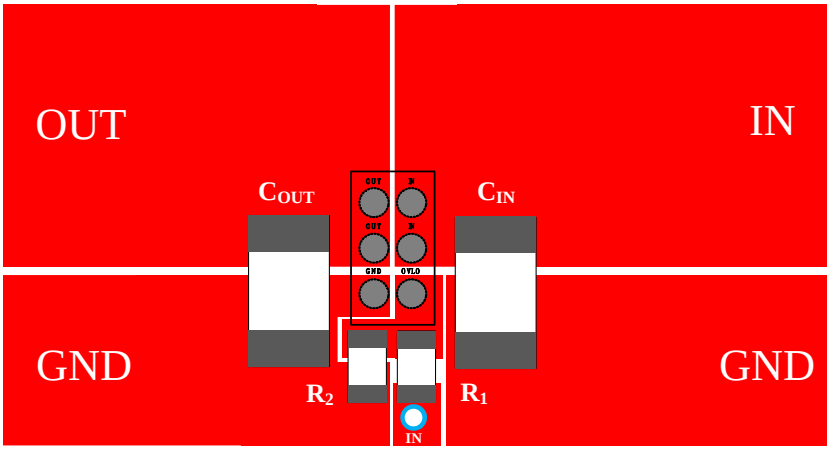
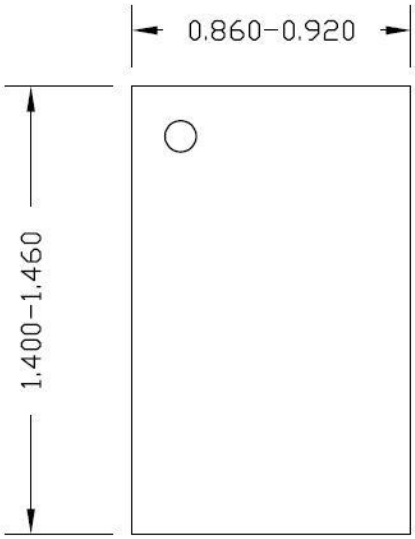
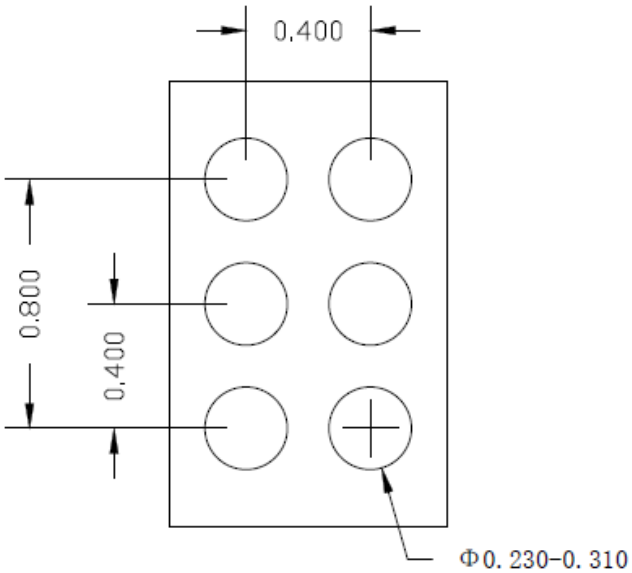



Figure4. PCB Layout Suggestion

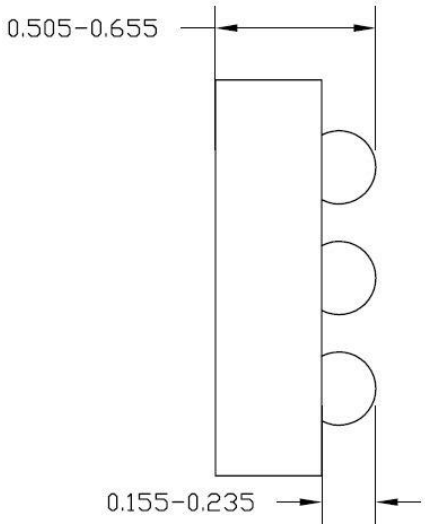
# CSP0.89*1.43-6 Package Outline Drawing



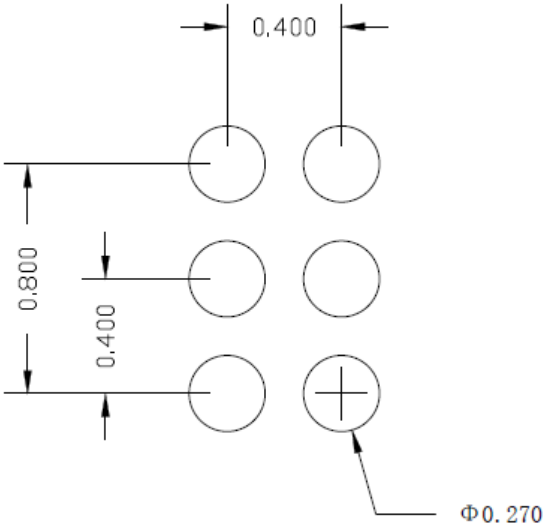

Top view




Bottom view




Side view

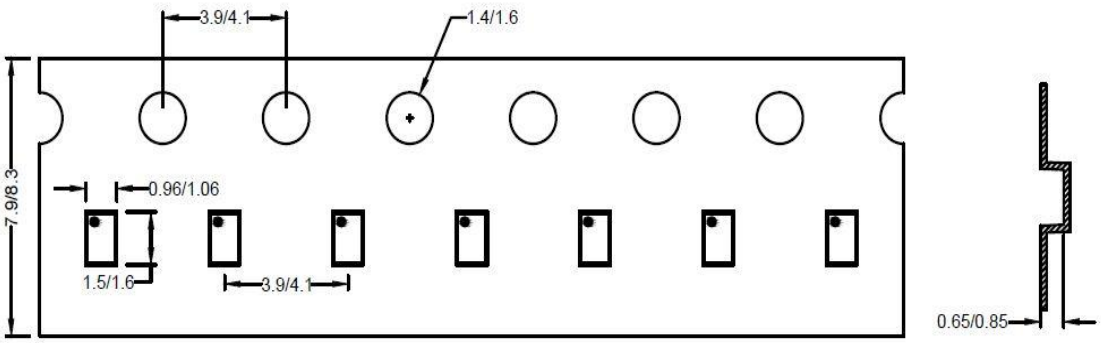



Recommended PCB layout
(Reference only)

**Notes:** **All dimension in millimeter and exclude mold flash & metal burr.**

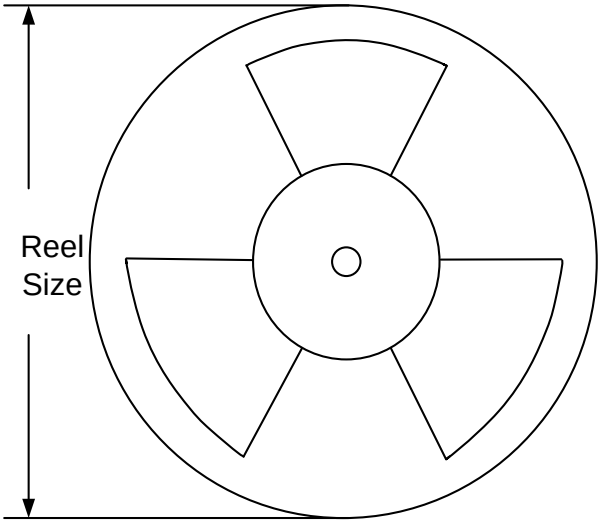
# Taping & Reel Specification

## 1. CSP0.89×1.43 Taping Orientation




**Feeding direction** ⟶

## 2. Carrier Tape & Reel specification for packages




| Package type | Tape width (mm) | Pocket pitch(mm) | Reel size (Inch) | Trailer length(mm) | Leader length (mm) | Qty per reel |
|---|---|---|---|---|---|---|
| CSP0.89×1.43 | 8 | 4 | 7" | 400 | 160 | 3000 |

## 3. Others: NA

# Revision History

The revision history provided is for informational purpose only and is believed to be accurate, however, not warranted. Please make sure that you have the latest revision.

| Date | Revision | Change |
|---|---|---|
| July 07, 2023 | Revision 0.9A | Update the waveform (Short Circuit Response) |
| Oct.16, 2017 | Revision 0.9 | Initial Release |

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