SQ24901

–48V Hot Swap and Single OR-ing Controller

General Description

The SQ24901 is an integrated hot swap and OR-ing controller that enables high power telecom systems to comply with stringent transient requirements. The 200V absolute maximum rating makes it easier to survive lightning surge tests (IEC61000-4-5). The soft-start cap disconnect allows for the use of smaller hot swap FETs by limiting the inrush current, without hurting the transient response. The dual hot swap gate driver saves space and BOM cost in high power applications that require multiple hot swap FETs. The 340μA sourcing current allows fast recovery, which helps to avoid system resets during lightning surge tests. The dual current limit makes it easier to pass brown outs and input steps such as required by the ATIS 0600315.2013. Finally, it offers accurate under-voltage and overvoltage protection with programmable thresholds and hysteresis.

The SQ24901 integrates an OR-ing controller, making it ideal for –48V systems those require reverse hook-up protection and reverse-current protection. The OR-ing controller protects the output when the input drops avoiding system resets.

Features

- –10V to –80V DC Operation, –200V Absolute Maximum
- Soft-start Cap Disconnect
- Dual Hot Swap Gate Drive
- 340μA Gate Sourcing Current
- Dual Current Limit (based on V_{DS})
  - 26 mV ±8% When Low V_{DS}
  - 3.7 mV ±22% When High V_{DS}
- Programmable UV(±1.5%) and OV (±2%)
  - Programmable Hysteresis (±11%)
- Integrated OR-ing Controller
  - Regulation: 25 mV ±15 mV
  - Fast Turn off: –25 mV ±4 mV
- Retries After Time Out
- RoHS Compliant and Halogen Free
- TSSOP16

Applications

- Remote Radio Units
- Baseband Units
- Routers and Switchers
- Small Cells
- –48V Telecommunications Infrastructure

Ordering Information

SQ24901 □(□□)□
- Temperature Code
- Package Code
- Optional Spec Code

Ordering Number	Package type	Note
SQ24901HKC	TSSOP16	----

Typical Application

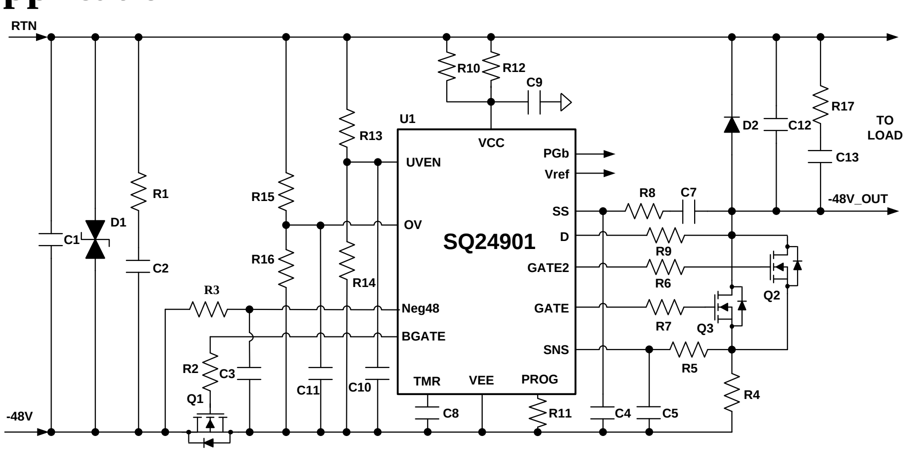
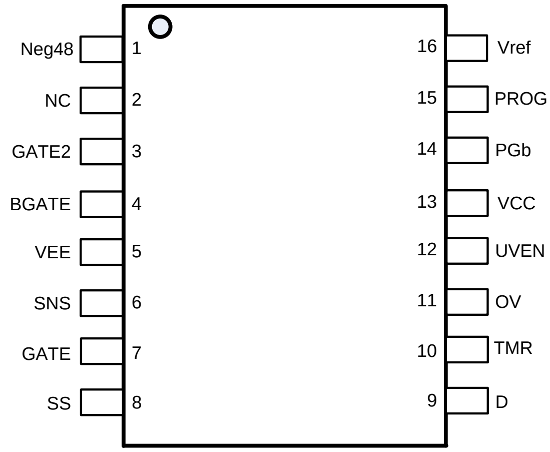


Figure1. Schematic Diagram

Pinout (top view)



(TSSOP16)

Top Mark: **CLY*xyz*** for SQ24901HKC **(**Device code: CLY; ***x=year code, y=week code, z= lot number code*)**

Pin Name	NO.	TYPE	Pin Description
Neg48	1	I	Input to the OR-ing controller for the –48 feed. The SQ24901 will regulate the drop from VEE to Neg48 to 25 mV to mimic an ideal diode.
NC	2	-	Not connected to space high voltage pins.
GATE2	3	O	Gate driver for the 2nd hot swap FET. NC if feature isn't used.
BGATE	4	O	Gate driver for the OR-ing FET.
VEE	5	GND	This pin corresponds to the IC GND. Kelvin sense to the bottom of RSNS to ensure accurate current limit.
SNS	6	I	Sense pin, used for measuring current and regulating it. Kelvin sense to RSNS to ensure accurate current limits.
GATE	7	O	Gate drive for the main hot swap FET.
SS	8	O	This pin is used for soft starting the output. Connect a capacitor (C_{SS}) between the SS pin and -48V_OUT. The dv/dt rate on the -48V_OUT pin is proportional to the gate sourcing current divided by C_{SS}.
D	9	I	This pin is used for sensing the drain of the hot swap FET and to program the threshold where the hot swap switches from the CL1 and CL2. Connect a resistor from this pin to the drain of the hot swap FET (also called -48V_OUT) to program the threshold.
TMR	10	O	Timer pin, used for programing the duration when the hot swap FET can be in current limit. Program this time by adding a capacitor between the TMR pin and VEE.
OV	11	I	Input over voltage comparator. Tie a resistor divider to program the threshold where the device turns off due to over voltage event.
UVEN	12	I	Input under voltage comparator. Tie a resistor divider to program the threshold where the device turns on.
VCC	13	S	Clamped supply. Tie to RTN through resistor.
PGb	14	O	Power Good Bar, which is an open drain output that indicated when the power is good and the load can start drawing full power. PGb goes low when the hot swap is fully on and the DC/DC can draw full power.
PROG	15	I	Adjust current limit and fast trip threshold by tying to VEE, floating, or tying to VEE through resistor.
Vref	16	O	5V reference output. Connect to the base of a BJT to generate a rail that can be used to power current monitors and digital Isolators.

Block Diagram

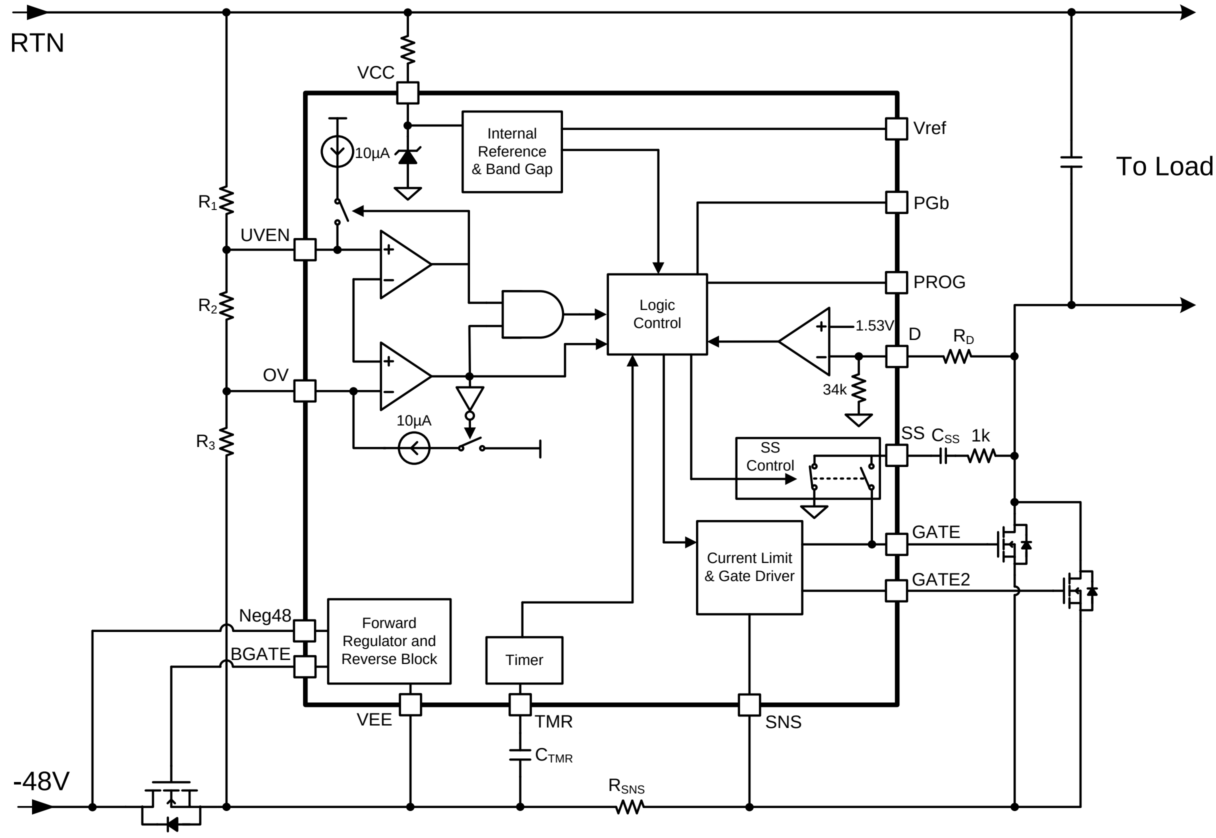


Figure2. Block Diagram

Absolute Maximum Ratings (Note 1, 3)

VCC (Current into VCC <10 mA) -- -0.3V to 20V
SNS, OV, TMR , PROG, VREF -- -0.3V to 6.5V
UVEN, D, SS --- -0.3V to 30V
Neg48, PGb -- -0.3V to 200V
Neg48 through 100Ω resistor -- -1V to 200V
Neg48 through 1kΩ resistor -- -2V to 200V
GATE, GATE2, BGATE --- -0.3V to VCC
Power Dissipation, P_D @ T_A = 25°C--- 0.99W
Package Thermal Resistance (Note 2)

θ_{JA} -- 101° C/W

θ_{JC} -- 34.5° C/W

Junction Temperature Range --- -40°C to +150°C
Lead Temperature (Soldering, 10 sec.) -- 260°C
Storage Temperature Range --- -65°C to 150°C

Recommended Operating Conditions (Note 3)

VCC (current into VCC <10 mA) --- 0V to 20V
SNS, OV, TMR , PROG, VREF --- 0V to 5.5V
UVEN, D, SS -- 0V to 18V
Neg48 through 100Ω resistor -- -0.2V to 150V
PGb -- 0V to 80V

Neg48 through 1kΩ resistor ---------- -2V to 200V
GATE, GATE2, BGATE ---------- 0V to VCC
C_{SS} ---------- 1nF to 200nF
R_{SS} ---------- 1kΩ to 10kΩ
R_D ---------- 120kΩ to 2000kΩ
R_{NEG48V} ---------- 100Ω to 1kΩ
Junction Temperature Range ---------- -40°C to 125°C
Ambient Temperature Range ---------- -40°C to 85°C

Electrical Characteristics

Unless otherwise noted: –40℃≤ T_J ≤125℃, 1.1 mA < I_{VCC} < 10 mA, V_{UVEN} = 2 V, V_{OV} = V_{SNS} = V_D = 0 V, V_{SS} = GATEx = Hi-Z, V_{TMR} = 0 V, –1V < $V_{NEG48Vx}$ < 150 V, V_{Vref} = V_{PROG} = Hi-Z; All pin voltages are relative to VEE.

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
VCC – Clamped Supply						
UVLO on VCC	V_{UVLO_VCC}	rising	8	9.5	11	V
UVLO Hysteresis on VCC	$V_{UVLO\_VCC,hyst}$	hysteresis		1		V
VCC Regulation	V_{VCC}	1.1< I_{VCC} < 10 mA (current into VCC)	12	14.5	18	V
Quiescent Current	I_Q	V_{VCC} = 10V. OFF			1	mA
		V_{VCC} = 10V. ON			1.65	mA
		V_{VCC} = 10V, Gate and BGATE in regulation			1.9	mA
UVEN – Under Voltage and Enable						
Threshold Voltage for V_{UVEN}	V_{UVEN_T}		0.985	1	1.015	V
Hysteresis Current, Sourcing from UV Pin	I_{UV_hyst}	V_{UV} = 1.5 V	9	10	11.2	µA
OV – Over Voltage						
Threshold Voltage for V_{OV}	V_{OV_T}		0.98	1	1.02	V
Hysteresis Current, Sourcing from OV Pin	I_{OV_hyst}	V_{OV} = 1.5 V	9	10	11.2	µA
TMR – Timer						
Voltage on Timer When Part Times Out.	V_{TMR}	V_D = 0V, TMR↑, measure V_{TMR} when V_{GATE} = 0	1.50	1.53	1.56	V
Voltage on Timer When Part Times Out.	V_{TMR2}	V_D = 1 V, TMR↑, measure V_{TMR} when V_{GATE} = 0	0.735	0.75	0.765	V
Timer Sourcing Current When in Fault Condition or When Retrying.	$I_{TMR,SRC}$	V_{SNS} = 0.1V, V_D = 0V, V_{TMR} = 0V, measure I out from TMR	9	10	11	µA
		V_{SNS} = 0.1V, V_D = 2V, V_{TMR} = 0V, measure I out from TMR	45	50	55	µA
Timer Sinking Current When not in Fault Condition.	$I_{TMR,SNC}$	V_{SNS} = 0V, V_D = 0V, V_{TMR} = 2V	1.5	2	2.5	µA
Voltage on Timer When the Timer Starts Going Back up in Retry. Retry Version Only.	$V_{TMR,RETRY}$	V_{SNS} = 0V, V_D = 0V, TMR↑= 2V, TMR↓, measure V_{TMR} when I into TMR change polarity	0.475	0.5	0.525	V
Number of Retry Duty Cycles. Retry Version Only.	N_{RETRY}			64		
Retry Duty Cycle. Retry Version Only.	D_{RETR}			0.4%		
Sense Voltage When Timer Starts to Run.	$V_{SNS,TMR1}$	V_D = 2 V, V_{TMR} = 0 V, V_G = 5 V; V_{SNS}↑, measure V_{SNS} when	1.5	3		mV

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
		TMR sources current				
Sense Voltage When Timer Starts to Run	$V_{SNS,TMR2}$	V_D = 0 V, V_{TMR} = 0 V, V_G = 5 V; V_{SNS}↑, measure V_{SNS} when TMR sources current	23.25	25.3		mV
SNS – Sense Pin For Current Limit						
Leakage Current on Sense Pin	$I_{SNS,LEAK}$		-2		2	µA
PROG = Float	$V_{SNS,CL1}$	V_{TMR} = 0V. V_{GATE} = 5V. V_D = 0V, V_{SNS} ↑, measure when I_{GATE} = 0;	24	26	28	mV
PROG = VEE			38	40	42	mV
PROG = FLOAT	$V_{SNS,FST}$	V_{TMR} = 0V. V_{GATE} = 5V. V_D = 0V, V_{SNS}↑, measure when I_{GATE}> 100mA	45	50	55	mV
PROG = VEE			72	80	88	mV
R_{PROG} = 78.7kΩ			110	120	130	mV
R_{PROG} = 162 kΩ			68	75	82	mV
Fold Back Current Limit	$V_{SNS,CL2}$	V_{TMR} = 0V. V_{GATE} = 5V. V_D = 5V, V_{SNS} ↑, measure when I_{GATE} = 0; T_J=25°C	2.9	3.7	4.5	mV
		T_J=-40°C ~125°C	2.2	3.7	5.2	mV
Fast Trip during Start-up	$V_{SNS,FST2}$	V_{TMR} = 0V. V_{GATE} = 5V. V_D = 5V, V_{SNS}↑, measure when I_{GATE}> 100mA	6	9	12	mV
PROG – Programing Pin to Set Current Limit (CL) and Fast Trip						
PROG Pin Current	I_{PROG}		7.9	10.1	12	µA
Prog Pin Voltage	$V_{PROG,LOW}$	Threshold on V_{PROG}, where the fast trip setting changes from 80mV to 120mV.			0.45	V
Prog Pin Voltage	$V_{PROG,MID}$	Threshold on V_{PROG}, where the current limit setting changes from 25mV to 40mV.	0.94	1.23	1.51	V
Prog Pin Voltage	$V_{PROG,High}$	Threshold on V_{PROG}, where the fast trip setting changes from 80mV to 120mV.	2.4			V
GATE – Gate Drive for Main Hot Swap FET						
Output Gate Voltage	$V_{VCC\text{-}GATE}$	V_{SNS} = 0 V			1	V
Sourcing Current during Normal Operation.	$I_{GATE,SRS,NORM}$	V_{TMR} = 0V. V_{GATE} = 8V. V_D = 0V, V_{SNS} = 0 V	210	340		µA
Sourcing Current during Start-up	$I_{GATE,SRS,START}$	V_{TMR} = 0V. V_{GATE} = 5V. V_D = 0V, V_{SNS} = 0 V	15	20	25	µA
Weak Pull Down Current	$I_{GATE,wkpd}$	V_{SNS} = 0V. V_{UVEN} = 0 V	8	11	14	mA
Fast Pull Down Current with 10mV Overdrive	$I_{GATE,FST}$		0.4	1	1.5	A
GATE2 – Gate Drive for Auxiliary Hot Swap FET						
Output Gate Voltage	$V_{VCC\text{-}GATE2}$	V_{SNS} = 0 V			1	V
Weak Pull Down Current	$I_{GATE2,wkpd}$	V_{GATE} = 0 V		11		mA
Sourcing Current	$I_{GATE2,SRC}$			50		µA
Fast Pull Down Current with 10 mV Overdrive	$I_{GATE2,FST}$		0.4	1	1.5	A
Threshold on V_{GATE} When GATE2 Turns On	$V_{GATE,TH}$	Raise V_{GATE}, measure when V_{GATE2} comes up	6.25	7.25	8	V
Hysteresis of Threshold on	$V_{GATE,TH,hyst}$	hysteresis		0.5		V

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
V_{GATE} When GATE2 Turns On						
D – Drain Sense						
Resistance from the Drain Pin to GND.	$R_{D,INT}$		32	34	36	kΩ
Voltage on Drain that Switches Between Two Current Limits	V_{D,CL_SW}	V_{TMR} = 0 V, V_{GATE} = 5 V, V_{SNS} = 20 mV, D↑, measure V when I_{GATE} > 100mA	1.49	1.53	1.57	V
Voltage on Drain that Switches the VTMR Threshold.	V_{D,TMR_SW}	V_{TMR} = 1 V, V_{GATE} = 5 V, V_{SNS} = 20 mV, D↑, measure V when I_{GATE} > 1mA	0.73	0.75	0.77	V
Hysteresis for $V_{D,TMR,SW}$	$V_{D,TMR\_SW,hyst}$	hysteresis		75		mV
SS (Soft-start)						
Pull Down Current When not In Inrush	$I_{SS,PD}$	V_{SS} = 5 V	100			mA
Resistance Between GATE and SS in the Start-up Phase	$R_{SS,GATE}$			150		Ω
Vref						
Reference Output	V_{Vref}	0 < I_{Vref} < 800 µA	4	4.9	5.5	V
V_{Vref} SC Current	I_{Vref}	Vref ON, V_{Vref} shorted		2		mA
Neg48						
Leakage Current	$I_{lkg,Neg48}$	V_{Neg48} = –50 mV, BGATE ON	-2		2	µA
		V_{Neg48} = –100 mV, BGATE ON	-7		7	µA
		V_{Neg48} = 150 V, BGATE off			30	µA
Forward Regulation Voltage of the OR-ing Controller. V_{FWD} = V_{EE} – $V_{NEG48Vx}$	V_{FWD}		10	25	40	mV
Forward Voltage where a Fast Pull Up is Activated.	$V_{FWD,FST}$	V_{GATEx} = 5 V. V_{VEE} – $V_{Neg48Vx}$ ↑ measure when I_{GATEx} = 100 µA	50	80	105	mV
Fast Reverse Trip Voltage.	V_{RV}		21	25	29	mV
BGATE						
Gate Output Voltage.	$V_{VCC-BGATE}$			0.65	1.1	V
Gate Sourcing Current in Regulation	$I_{BGATE,SRS}$	V_{VEE} – $V_{Neg48Vx}$ = 50 mV		30		µA
Gate Sinking Current in Regulation	$I_{BGATE,SINK}$	V_{VEE} – $V_{Neg48Vx}$ = 0		30		µA
Pull-up Resistance in Fast Sourcing Mode	$R_{GATE,SRC,FST}$	V_{VEE} –$V_{Neg48Vx}$ = 100 mV; Measure current at V_{GATEx} = 0 V. R = $V_{VCC/I}$		14		kΩ
Fast Gate Pull Down Current	$I_{BGATE,FST}$	V_{VEE} – V_{Neg48} = –40 mV	0.4	1	1.5	A
PGb (Power Good Bar)						
Threshold on GATE2 that Triggers PGb to Assert.	$V_{GATE2,PGb}$	Raise V_{GATE2} until PGb asserts	6.5	7.25	8	V
Pull Down Strength on PGb	$V_{PGb,PD}$	PGb sinking 1 mA			1.5	V
leakage Current on PGb Pin	$I_{PGb,LEAK}$				1	µA
OTSD (Over Temperature Shut Down)						
Shutdown Temperature Temp Rising	T_{SD}		135	155	175	°C
Shutdown temperature Hysteresis	$T_{SD,hyst}$			8		°C

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
VCC – Clamped Supply						
Insertion Delay	t_{ID}	V_{VCC}: 0 V → 10 V, measure delay before V_{GATE} ↑		32		ms
UVEN						
Deglitch on UVEN	$t_{UV,degl}$			4		μs
OV						
Deglitch on OV	$t_{OV,degl}$			4		μs
SNS						
Response Time to Large Over Current	$t_{SNS,FST,RESP}$	V_{SNS} steps from 0 mV to 60 mV. Measure time for GATE and GATE2 to come down.		300		ns
Neg48V						
Response Time to Large Reverse Current	$t_{Neg48V,FST,RESP}$	V_{NEG48V} steps from -40 mV to 15mV. Measure time for BGATE to come down.		300		ns
PGb						
Deglitch of PGb. (GATE2 = Unloaded, Raise GATE, Measure Delay Between GATE and PGb)	$t_{PGb,DEGL}$	Power Good ↑ (V_{GATE} 0V → 10V) Look for PGb ↓		1		ms
		Power Good ↓ (V_{GATE} 10V → 0V) Look for PGb ↑		32		ms

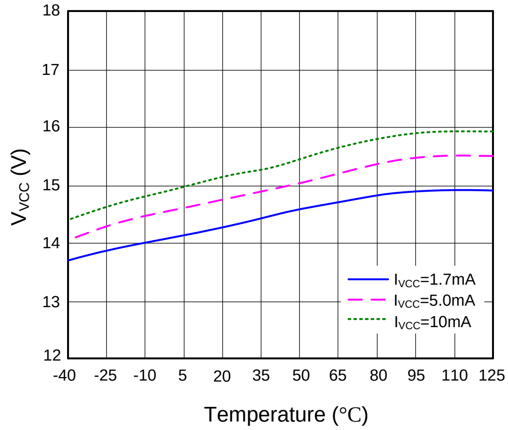
Note 1: Stresses beyond the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: θ_{JA} is measured in the natural convection at T_A = 25°C on a low effective double layer thermal conductivity test board of JEDEC 51-3 thermal measurement standard.

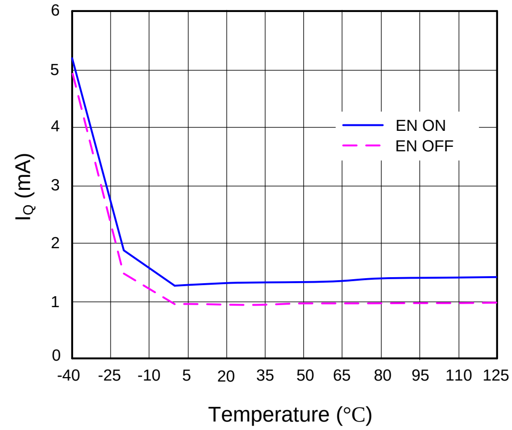
Note 3: The device is not guaranteed to function outside its operating conditions.

Typical Performance Characteristics

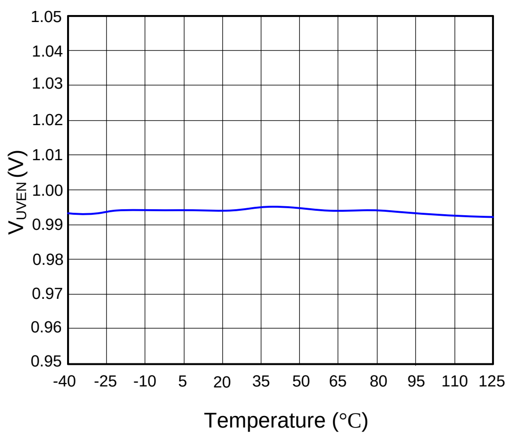
VCC Regulation Voltage vs. Temperature



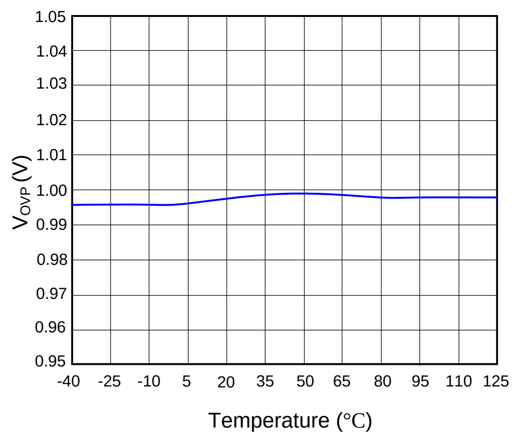
Quiescent Current vs. Temperature



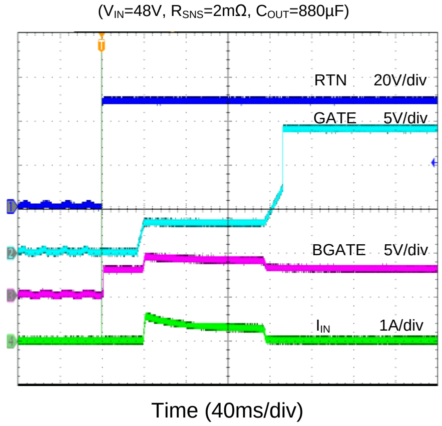
UVEN Threshold Voltage vs. Temperature



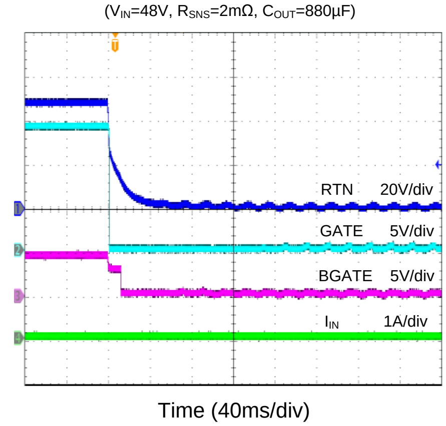
OVP Threshold Voltage vs. Temperature



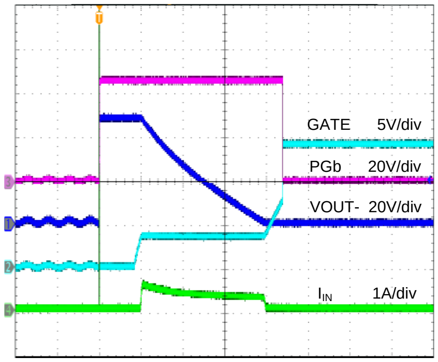
Startup
(V_{IN}=48V, R_{SNS}=2mΩ, C_{OUT}=880µF)



Shutdown
(V_{IN}=48V, R_{SNS}=2mΩ, C_{OUT}=880µF)

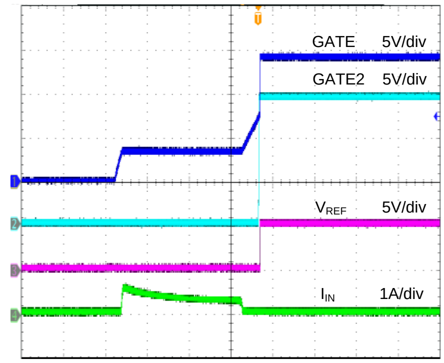


Startup
(V_{IN}=48V, R_{SNS}=2mΩ, C_{OUT}=880µF)



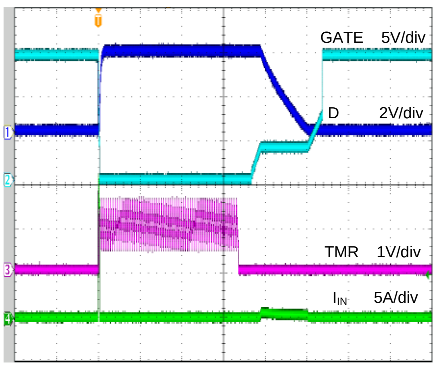
Time (40ms/div)

Startup
(V_{IN}=48V, R_{SNS}=2mΩ, C_{OUT}=880µF)



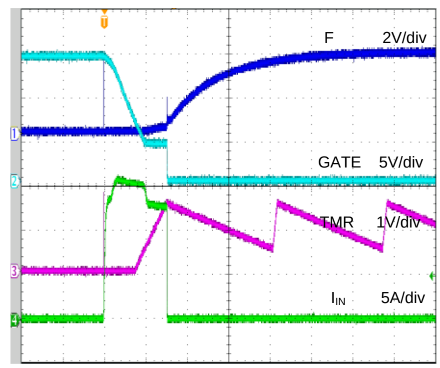
Time (40ms/div)

Current Limit and Remove Current Limit
(V_{IN}=48V, R_{SNS}=2mΩ, C_{TME}=10nF, C_{OUT}=880µF)



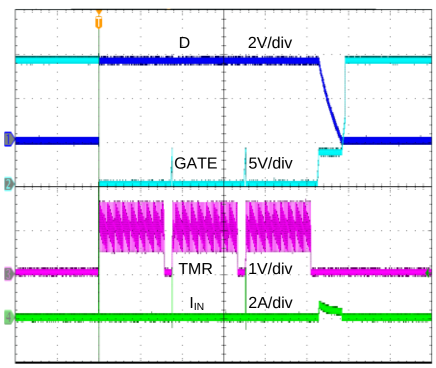
Time (100ms/div)

Current Limit (Zoomed In)
(V_{IN}=48V, R_{SNS}=2mΩ, C_{TME}=10nF, C_{OUT}=880µF)



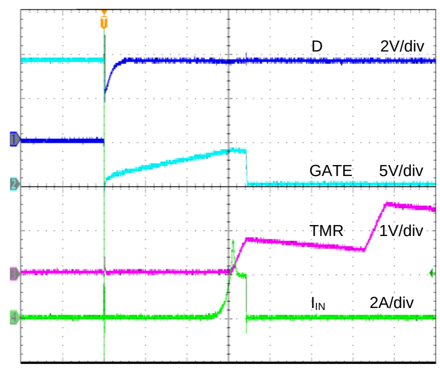
Time (2ms/div)

Hard-short and Remove Short



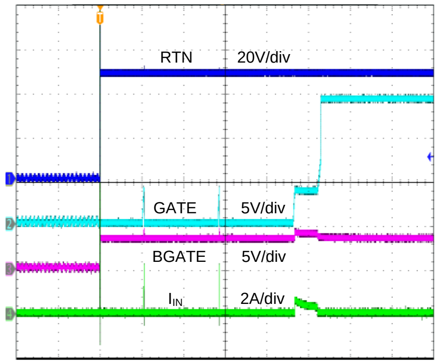
Time (200ms/div)

Hard-short (Zoomed In)



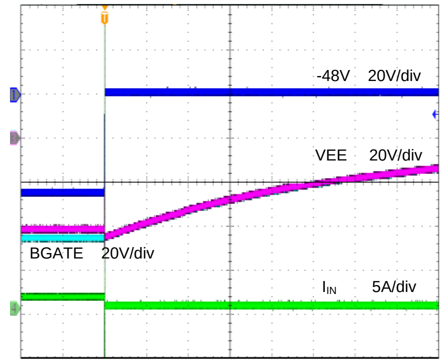
Time (400µs/div)

Start Into Short and Remove Short



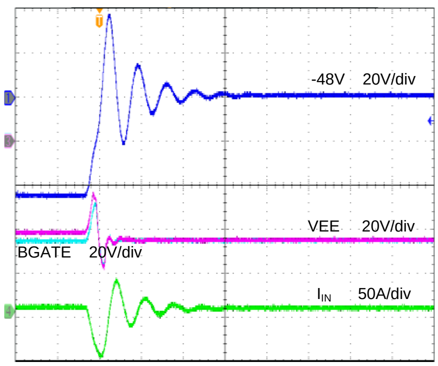
Time (200ms/div)

Short on V_{IN}
(scope GND = RTN)



Time (2ms/div)

Short on V_{IN} (Zoomed In)
(scope GND = RTN)



Time (1µs/div)

Overview

The SQ24901 is an integrated hot swap and Single OR-ing controller that enables high power telecom systems to comply with stringent transient requirements. The 200V absolute maximum rating makes it easier to survive lightning surge tests (IEC61000-4-5). The soft start cap disconnect allows soft start at start-up and disconnects the soft start cap during normal operation. This allows for the use of smaller hot swap FETs without hurting the transient response. GATE2 is a second hot swap FET driver, which only turns ON when the main hot swap FET is fully on. Thus the FETs driven by GATE2 don't need to have strong SOA. This saves space and BOM cost in high power applications that require multiple hot swap FETs. The 340-µA sourcing current allows fast recovery, which helps to avoid system resets during lightning surge tests. The dual current limit makes it easier to pass brown outs and input steps such as required by the ATIS 0600315.2013. Finally, the SQ24901 offers accurate under voltage and over voltage protection with programmable thresholds and hysteresis.

The SQ24901 integrates an OR-ing controller, making it ideal for –48 V systems that require reverse hook-up protection and reverse-current protection. The OR-ing controller protects the output when the input drops avoiding system resets. The OR-ing controller will turn off if any reverse current is detected.

Feature Description

1. Current Limit

The SQ24901 utilizes two current limit thresholds:

- I_{CL1} – also referred to as high current limit threshold, which is used when the V_{DS} of the hot swap FET is low.
- I_{CL2} – lower current limit threshold, which is used when the V_{DS} of the hot swap FET is high.

This dual level protection scheme ensures that the part has a higher chance of riding out voltage steps and other transients due to the higher current limit at low V_{DS}, while protecting the MOSFET during start into short and hard-short events, by setting a lower current limit threshold for conditions with high V_{DS}. The transition threshold is programmed with a resistor that is connected from the drain of the hot swap FET to the D pin of the SQ24901. The figure below illustrates an example with a I_{CL1} set to 25A and I_{CL2} set to 3A. Note that compared to a traditional SOA protection scheme this approach allows better utilization of the SOA in the 10V< V_{DS} <40V range, which is critical in riding through transients and voltage steps.

Note that in both cases the SQ24901 regulated the gate voltage to enforce the current limit. However, this regulation is not very fast and doesn't offer the best protection against hard-shorts on the output. To protect in this scenario a fast comparator is used, which quickly pulls down the gate in case of severe over current events (2x bigger than V_{CL1}).

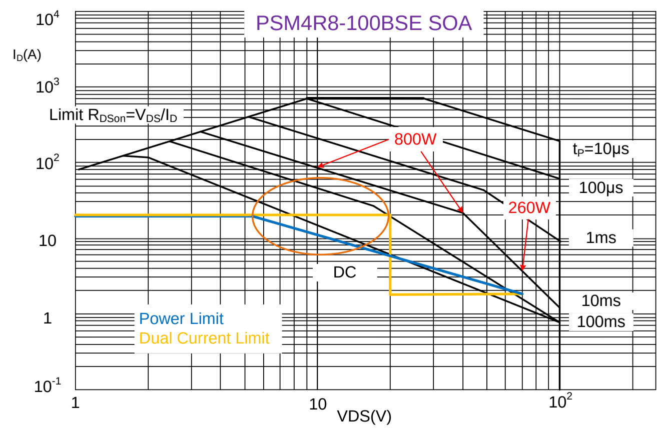


Figure 3. Dual Current Limit vs. FET Power Limit

1.1 Programming the CL Switch-Over Threshold

The V_{DS} threshold when the SQ24901 switches over from I_{CL1} to I_{CL2} ($V_{D,\ SW}$) can be computed using Equation 1. For example, if a 15V switch over is desired, R_D should be set to 300kΩ.

$$V_{D,SW} = \frac{1.53V \times (34k\Omega + R_D)}{34k\Omega} \quad (1)$$

1.2 Setting Up the PROG Pin

The PROG pin can be tied to VEE, left floating, or tied to VEE through a resistor to adjust $V_{SNS,\ CL1}$ and the ratio of fast trip to current limit. The options are set as follows:

- PROG = NC or Float: $V_{SNS,\ CL1}$ = 26 mV, $V_{SNS,FST}$ is 2× $V_{SNS,CL1}$
- R_{PROG} = 196 kΩ (1%): $V_{SNS,\ CL1}$ = 26 mV, $V_{SNS,FST}$ is 3×$V_{SNS,CL1}$
- R_{PROG} = 66.5 kΩ (1%): $V_{SNS,\ CL1}$ = 40 mV, $V_{SNS,FST}$ is 3×$V_{SNS,CL1}$
- PROG = VEE: $V_{SNS,\ CL1}$ = 40 mV, $V_{SNS,FST}$ is 2× $V_{SNS,CL1}$

1.3 Programming CL1

The current limit at low V_{DS} (I_{CL1}) of the SQ24901 can be computed using Equation 2 below.

$$I_{CL1} = \frac{V_{SNS,CL1}}{R_{SNS}} \quad (2)$$

To compute I_{CL1} for a 1-mΩ sense resistor use Equation 3 below.

$$I_{CL1} = \frac{V_{SNS,CL1}}{R_{SNS}} = \frac{26mV}{1m\Omega} = 26A \qquad (3)$$

1.4 Programming CL2

The current limit at high V_{DS} (I_{CL2}) of the SQ24901 can be computed using Equation 4 below.

$$I_{CL2} = \frac{V_{SNS,CL2}}{R_{SNS}} \qquad (4)$$

To compute I_{CL2} for a 1mΩ sense resistor use Equation 5 below.

$$I_{CL2} = \frac{V_{SNS,CL2}}{R_{SNS}} = \frac{3.7mV}{1m\Omega} = 3.7A \qquad (5)$$

2. Soft-start Disconnect

The inrush current into the output capacitor (C_{OUT}) can be limited by placing a capacitor between the SS (Soft Start) pin and the drain of the hot swap MOSFET. In that case the inrush current can be computed using equation below.

$$I_{INR} = \frac{C_{OUT} \times I_{GATE,SRS,START}}{C_{SS}} = \frac{660\mu F \times 20\mu A}{33nF} = 0.4A \qquad (6)$$

Note that with most hot swap the C_{SS} pin is tied simply to the gate pin, but this can interfere with performance during normal operation if transients or short circuits are encountered. In addition, the C_{SS} capacitor tends to pull up the gate during hot plug and cause shoot through current if it is always tied to the gate. For that reason, the SQ24901 has a disconnect switch between the gate pin and the SS pin as well as a discharge resistor. During the initial hot plug and during the insertion delay the switch between SS and GATE is open and SS is being discharged to GND through a resistor. Then during start-up SS and GATE are connected to limit the slew rate. Once in normal operation the SS pin is not tied to GATE and it is not shorted to GND, which prevents it from interfering with the operation during transients.

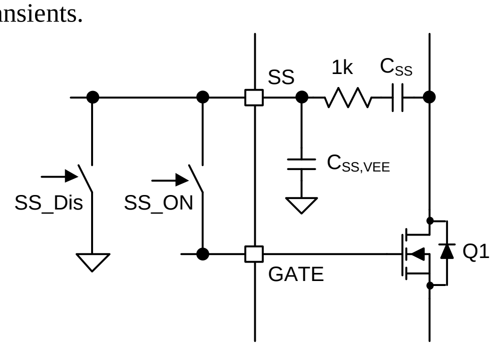


Figure 4. Implementation of SS Disconnect

3. Timer

Timer is a critical feature in the hot swap, which manages the stress level in the MOSFET. The timer will source and sink current into the timer capacitor as follows:

- Not in current limit: sink 2 µA
- If the part is in current limit and $V_{GATE} < V_{GATE,TH}$, the timer sources current as follows:
  – $V_D < V_{D,CL\_SW}$: source 10 µA
  – $V_D > V_{D,CL\_SW}$: source 50 µA

The SQ24901 times out and shuts down the hot swap as follows:

- If $V_D < V_{D,TMR\_SW}$ then the hot swap times out when V_{TMR} reaches 1.53 V
- If $V_D > V_{D,TMR\_SW}$ then the hot swap times out when V_{TMR} reaches 0.75 V

The above behavior maximizes the ability of the hot swap to ride out voltage steps, while ensuring that the FET remains safe even if the part can not ride out a voltage step.

A cool down period follows after the part times out. During this time the timer performs the following:

- Discharge C_{TMR} with a 2µA current source until 0.5 V
- Charge C_{TMR} with a 10-µA current source until it is back to 1.53 V.
- Repeat the above 64 times
- Discharge timer to 0 V.

The part attempts to restart after finishing the above. If the UVEN signal is toggled while the 64 cycles are in progress the part restarts immediately after the 64 cycles are completed.

The timer operates as follows when recovering from POR:

- If $V_{TMR} < 0.5$ V:
  – Proceed to regular startup
  – Do not discharge V_{TMR}
- If $V_{TMR} > 0.5$ V:
  – Go through 64 charge/discharge cycles
  – Discharge V_{TMR}
  – Proceed to startup

The Time Out (t_{TO}) can be computed using the equations below. Note that the time out depends on the V_{DS} of the MOSFET.

$$t_{TO} = \frac{C_{TMR} \times V_{TMR}}{I_{TMR,SRS}} \qquad (7)$$

$$t_{TO}(V_D < 0.75V) = \frac{C_{TMR} \times 1.53V}{10\mu A} \quad (8)$$

$$t_{TO}(0.75V < V_D < 1.53V) = \frac{C_{TMR} \times 0.75V}{10\mu A} \quad (9)$$

$$t_{TO}(V_D > 1.53V) = \frac{C_{TMR} \times 0.75V}{50\mu A} \quad (10)$$

4. Gate 2

The SQ24901 features a second hot swap Gate drive, which can be used to save BOM cost and size in applications that require multiple hot swap MOSFETs. The 2nd MOSFET is only turned ON when the main FET is enhanced. As a result, the 2nd MOSFET doesn't operate with large current and large voltage across it, thus reducing the SOA requirements. In many cases a 5×6 QFN FET can replace a D²PACK FET. The following figures show the operation during start-up and Hard Short event. It can be seen that the second FET is OFF during stressful operation and turns on during normal operation to improve steady state efficiency and reduce power losses.

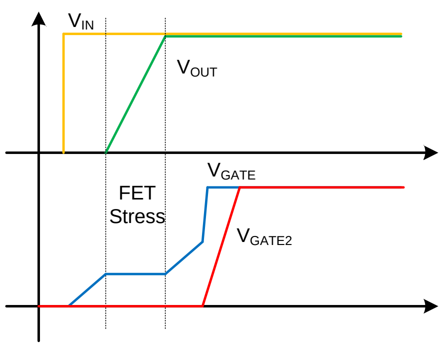


Figure 5. Gate 2 Operation During Start-up

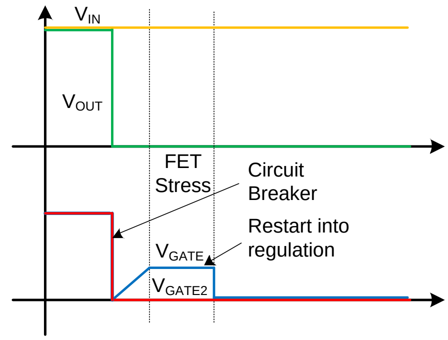


Figure 6. Gate2 Operation During Hard Short

5. OR-ing

The SQ24901 features integrated OR-ing that controls the external MOSFET in a way to emulate an ideal diode. The SQ24901 will regulate the forward drop across the OR-ing FET to 25 mV. This is accomplished by controlling the V_{GS} of the MOSFET. As the current decreases the V_{GS} is also decreased, which effectively increases the R_{DSON} of the MOSFET. This process is regulated with a low gain amplifier that is gate (OR-ing FET) pole compensated. The lower gain helps ensure stability over various operating conditions. The regulating amplifier ensures that there is no DC reverse current. However, the amplifier is not very fast and thus it is paired with a fast comparator. This comparator quickly turns off the FET if there is significant reverse current detected.

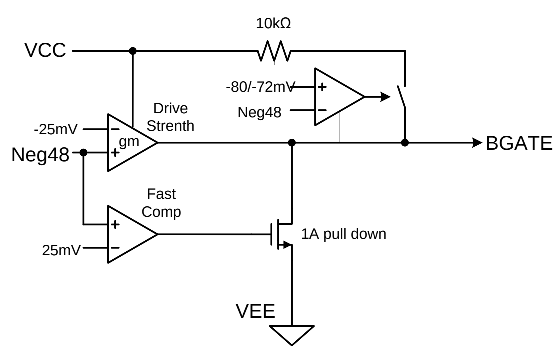


Figure 7. Simplified Diagram of OR-ing Block

Device Functional Modes

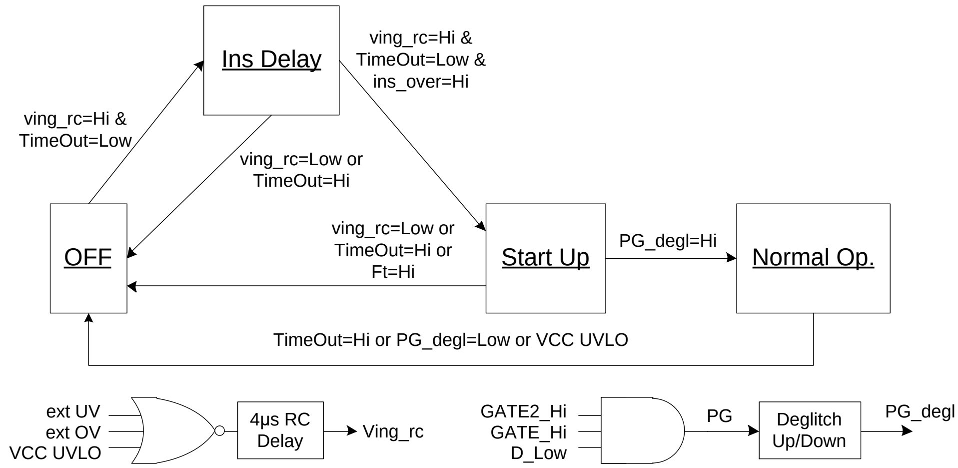


Figure 8. Simplified Hot Swap State Machine

The Figure above shows a simplified state machine of the hot swap controller. It has 4 distinct operating states and the controller switches between these states based on the following signals:

- Ving_rc: This means that both the input voltage is in the right range and the IC has power with Vcc. A 4-µs delay is added for deglitching. If the input voltage is above the OV threshold, input voltage is below the UV threshold, or VCC is below its internal UVLO, Ving_rc will be low.
- TimeOut: This signal comes from the timer block and will be asserted Hi if the IC has timed out due to an over-current condition. This signal is also Hi while the timer is going through the restart cycles. Once the cycles are completed this signal will go Low.
- ins_over: This signal states that the insertion delay has been completed and the hot swap is ready to start-up.
- FT: this is the fast trip signal coming from the fast trip comparator. It goes Hi if an extreme over current event is detected.
- PG: Internal Power good signal. This is high when the hot swap is fully on and the load can draw full power. For PG to be Hi, the GATE has to be Hi, GATE2 needs to be Hi, and the drain pin needs to be below 0.75 V.
- PG_degl: This is a deglitched version of the PG and is the signal used to move between states and controls the external PGb pin.

1. OFF State

In this state the hot swap FET is turned off and the controller is waiting to start-up. The controller can be in this state due to any of these scenarios:

- Input voltage is not in the valid range.
- The hot swap is in the cool down state and the timer is going through the retry cycle after a fault condition such as output Hard Short or over current.
- VCC is below its UVLO threshold and the IC doesn't have enough power to operate properly.

2. Insertion Delay State

In this state the hot swap FET is turned off and the controller is waiting for the insertion delay to finish. This allows the input supply to settle after a Hot Plug. If any of the following occur, the controller will be kicked back to the OFF state:

- Input voltage is not in the valid range.
- VCC is below its UVLO threshold and the IC doesn't have enough power to operate properly.

Once the insertion delay is finished, the controller will move to the Start-up state.

3. Start-up State

In this state the controller is turning on and charging the output cap. The operation is set as follows:

- The SS pin is internally connected to the GATE pin to allow for output dv/dt control.
- Lower gate sourcing current is applied to the GATE pin to allow for smaller SS caps.
- The lower current limit setting of $V_{SNS,CL2}$ and a lower fast trip setting of $V_{SNS,FST2}$ is used to

minimize the MOSFET stress in case of a fault condition.

If any of the following occur, the controller will be kicked back to the OFF state:

- Input voltage is not in the valid range.
- The timer times out due to over-current.
- VCC is below its UVLO threshold and the IC doesn't have enough power to operate properly.
- Fast trip is triggered.

Once the PG_degl signal goes Hi, the controller will move to the Normal Operation state.

4. Normal Operation State

In this state the hot swap is fully on and the operation is set as follows:

- The SS pin is disconnected from the GATE pin to improve transient response.
- The full gate sourcing current is used to improve transient response.
- The current limit and fast trip threshold are a function of the D pin to optimize the transient response while protecting the MOSFET.

If any of the following occur, the controller will be kicked back to the OFF state:

- PG_degl goes low.
- The timer times out due to over-current.
- VCC is below its UVLO threshold and the IC doesn't have enough power to operate properly.

Note that if the input voltage is outside the valid range or the fast trip is triggered, the hot swap FET will turn off, but the controller will not exit the Normal Operation state. In this case the PG signal would go low immediately. If this condition persists, the PG_degl will go low as well and the controller would move to the OFF state. This operation prevents the controller from re-starting the system during quick transients.

Application Information

The SQ24901 is a hot swap controller for –48-V applications and is used to manage inrush current and protect downstream circuitry and the upstream bus in case of fault conditions. The following key scenarios should be considered when designing a –48-V hot swap circuit:

- Start Up.
- Output of a hot swap is shorted to ground while the hot swap is on. This is often referred to as a Hot Short.
- Powering up a board when the output and ground are shorted. This is usually called a start-into-short.
- Input lightning surge. Here it is usually desired to avoid damage to downstream circuitry and to avoid system restarts.

These scenarios place a lot of stress on the hot swap MOSFET and the board designer should take special care to ensure that the MOSFET stays within it's Safe Operating Area (SOA) under all of these conditions. A detailed design example is provided below and the key equations are written out. Note that solving all of these equations by hand is cumbersome and can result in errors.

1. Design Requirements

The table below summarizes the design parameters that must be known before designing a hot swap circuit. When charging the output capacitor through the hot swap MOSFET, the FET's total energy dissipation equals the total energy stored in the output capacitor ($1/2CV^2$). Thus both the input voltage and output capacitance will determine the stress experienced by the MOSFET. The maximum load power will drive the current limit and sense resistor selection. In addition, the maximum load current, maximum ambient temperature, and the thermal properties of the PCB ($R_{\theta CA}$) will drive the selection of the MOSFET's R_{DSON} and the number of MOSFETs used. $R_{\theta CA}$ is a strong function of the layout and the amount of copper that is connected to the drain of the MOSFET. Air cooling will also reduce $R_{\theta CA}$ substantially. Finally, it's important to know what transients the circuit has to pass in order to size up the input protection accordingly.

Table 1. Design Requirements for a –38V to –60V, 400W Protection Circuit

Design Parameter	Example Value
Input Voltage Range	–38 V to –60 V
Maximum Load Power	400 W
Output Capacitance	660 µF
Location Of Output Capacitor	After EMI filter with ~5 µH of inductance.
Maximum Ambient Temperature	85°C
MOSFET $R_{\theta CA}$ (function of layout)	20°C/W
Pass "Hard-Short" on Output	Yes
Pass a "Start Into Short"	Yes
Is the Load Off until PG Asserted	Yes
Max Input Inductance	10 µH

Design Parameter	Example Value
Level of IEC61000-4-5 to Pass	2-kV Line to Line with 2-Ω series impedance
Pass Reverse Hook Up	Yes

2. Detailed Design Procedure

2.1 Selecting R_{SNS}

Before selecting R_{SNS}, first compute the maximum load current. For this example, the worst case load current happens at the minimum input voltage of 38 V. Thus the maximum current is 400 W/38 V = 10.5A. To provide some margin, set the target current limit to 12 A and compute R_{SNS} using equation below:

$$R_{SNS} = \frac{V_{SNS,CL1}}{I_{CL1}} = \frac{26mV}{12A} = 2.17m\Omega \quad (11)$$

Use next available R_{SNS} of 2 mΩ.

2.2 Selecting Soft Start Setting: C_{SS} and $C_{SS,\,VEE}$

First, compute the minimum inrush current where the timer will trip using equation below.

$$I_{INR,TMR} = \frac{V_{SNS,TMR2}}{R_{SNS}} = \frac{1.5mV}{2m\Omega} = 0.75A \quad (12)$$

To avoid running the timer the inrush current needs to be sufficiently low. Target 0.4 A of inrush current to allow margin, and compute the target C_{SS} using equation below.

$$C_{SS} = \frac{C_{OUT,MAX} \times I_{GATE,SRS,START}}{I_{INR,TGT}} = \frac{792\mu F \times 20\mu A}{0.4A} = 39.6nF$$

(13)

Next choose, the next available C_{SS} greater than 39.6 nF. For this example, 43 nF was used, which assumes a 33nF and 10nF cap in parallel. This results in an inrush current of 0.37 A at max C_{OUT} (792 µF) and inrush current of 0.31 A at typical C_{OUT} (660 µF). Also it is recommended to add a capacitor between the soft start pin and V_{EE} ($C_{SS,\,VEE}$) to improve immunity to input voltage noise during soft start. It's recommended to choose a capacitor that's 3x larger than C_{SS}. In this case a 150 nF capacitor was chosen. Finally, the start-up time at maximum input voltage can be computed using the equation below:

$$t_{START}(V_{INMAX}) = \frac{C_{SS} \times V_{IN,MAX}}{I_{GATE,SRS,START}} = \frac{43nF \times 60V}{20\mu A} = 129ms \quad (14)$$

2.3 Selecting V_{DS} Switch Over Threshold

The V_{DS} threshold where the current limit switches from CL1 to CL2 can be programmed using R_D. In general, a higher threshold improves ability to ride through voltage steps, brown outs, and other transients. However, a larger setting can also expose the MOSFET to more stress, because the larger current limit is now allowed at higher V_{DS} voltages. If there are no specific voltage step requirements, 20V is a good starting point. Use the equation below to compute the target R_D.

$$R_D = 34k\Omega \times (\frac{V_{DS,SW}}{1.53V} - 1) = 410k\Omega \quad (15)$$

2.4 Timer Selection

The timer determines how long the hot swap can be in current limit before timing out and can be programmed using C_{TMR}. In general, a longer time out (T_{TO}) improves ability to ride through voltage steps, brown outs, and other transients. However, a larger setting can also expose the MOSFET to more stress, because it takes longer for the FET to shut down during fault conditions. If there are no specific voltage step or transient requirements, 2 ms is a good starting point. Use the equation below to compute the target C_{TMR}. Choose the next available capacitor value of 15 nF, which results in a 2.25 ms time out.

$$C_{TMR} = \frac{t_{TO} \times I_{TMR,SRS}}{V_{TMR}} = \frac{2ms \times 10\mu A}{1.53V} = 13.1nF \quad (16)$$

2.5 MOSFET Selection and SOA Checks

When selecting MOSFETs for the –48 V application the three key parameters are: V_{DS} rating, R_{DSON}, and safe operating area (SOA). For this application the CSD19535KTT was selected to provide a 100V V_{DS} rating, low R_{DSON}, and sufficient SOA. After selecting the MOSFET, it is important to double check that it has sufficient SOA to handle the key stress scenarios: start-up, output Hot Short, and Start into Short. MOSFET's SOA is usually specified at a case temperature of 25°C and should be derated based on the maximum case temperature expected in the application. Compute the maximum case temperature using the equation below. Note that the R_{DSON} will vary with temperature and solving the equation below could be a repetitive process. The CSD19535KTT, has a maximum 3.4mΩ R_{DSON} at room temperature and is ~1.5x higher at 100°C. N stands for the number of MOSFETs used in parallel.

$$T_{C,MAX} = T_{A,MAX} + R_{\theta CA} \times (\frac{I_{LOAD,MAX}}{N})^2 \times R_{DSON}(T_J) \quad (17)$$

$$T_{C,MAX} = 85°C + 20°C/W \times (10.5A)^2 \times (3.4 \times 1.5m\Omega) = 96.3°C \quad (18)$$

Next the stress the MOSFET will experience during operation should be compared to the FETs capability. First, consider the power up. The inrush current with max C_{OUT} will be 0.37 A and the inrush will last for 129 ms. Note that the power dissipation of the FET will start at $V_{IN,\ MAX} \times I_{INR}$ and reduce to zero as the V_{DS} of the MOSFET is reduced. The SOA curve of a typical MOSFET assume the same power dissipation for a given time. A conservative approach is to assume an equivalent power profile where $P_{FET} = V_{IN,MAX} \times I_{INR}$ for $t = t_{start\text{-}up}/2$. In this instance, the SOA can be checked by looking at a 60 V, 0.4 A, 64.5ms pulse. Based on the SOA of the CSD19535KTT, it can handle 60 V, 1.8 A for 10 ms and it can handle 60 V, 1 A for 100 ms. The SOA at T_C = 25°C for 64.5ms can be extrapolated by approximating SOA vs time as a power function as shown in equations below:

$$I_{SOA}(t) = a \times t^m \quad (19)$$

$$m = \frac{In(I_{SOA}(t_1)/I_{SOA}(t_2))}{In(t_1/t_2)} = \frac{In(\frac{1.8A}{1A})}{In(\frac{10ms}{100ms})} = -0.25 \quad (20)$$

$$a = \frac{I_{SOA}(t_2)}{t_2^m} = \frac{1A}{(100ms)^{-0.25}} = 3.16A \times (ms)^{0.25} \quad (21)$$

$$I_{SOA}(64.5ms, 25°c) = 3.16A \times (ms)^{0.25} \times (64.5ms)^{-0.25} = 1.12A \quad (22)$$

Finally, the FET SOA needs to be derated based on the maximum case temperature as shown below. Note that the FET can handle 0.59 A, while it will have 0.37 A during start-up. Thus there is a lot of margin during this test condition.

$$I_{SOA}(64.5ms, T_{C,MAAX}) = 1.12A \times \frac{175°C - 96.3°C}{175°C - 25°C} = 0.59A \quad (23)$$

A similar approach should be taken to compute the FETs SOA capability during a Hot Short and start into short. As shown in the following figure, during a start into short the gate is coming up very slowly due to a large capacitance tied to the gate through the SS pin. Thus it is more stressful than a Hot Short and should be used for worst case SOA calculations. To compare the FET stress during start-up into short to the SOA curves the stress needs to be approximated as a square pulse as showing in the figure below. In this example, the stress is approximated with a 1.1 ms (Teq), 1.5 A, 60 V pulse. The FET can handle 6 A, 60 V for 1 ms and 1.8 A, 60 V for 10 ms. Using approximation and temp derating as shown earlier, the FET's capability can be computed as 3 A, 60 V, for 1.1 ms at 96°C. 3 A is significantly larger than 1.5 A implying good margin.

The final operating point to check is the operation with high current and V_{DS} just below the $V_{DS,SW}$ threshold. In this example, the time out would be 1.1ms (one half of the time out at V_d = 0 V), the current will be 12.5 A, and the voltage would be 20 V. Looking up the SOA curve, the FET can handle 30 A, 20 V for 1 ms and 10 A, 20 V for 10 ms. Repeating previously shown approximations and temp derating, the FET's capability is computed to be 16 A, 20 V, for 1.1 ms at 96°C. Again this is below the worst case operating point of 12.5 A and 20 V suggesting good margin.

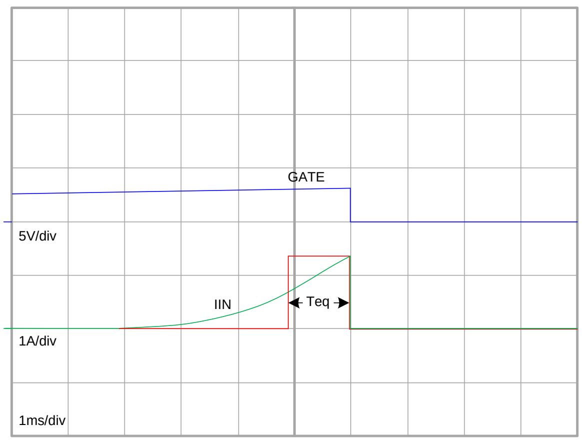


Figure 9. Teq During a Start Into a Short

2.6 Input Capacitor, Input TVS, and OR-ing FET Selection

This design example is sized for an application that needs to pass a 2 kV, 2Ω lightning strike per IEC61000-4-5. This equates to almost 1000 A of input current that needs to be clamped. In addition, the design needs to pass reverse hook up and thus the TVS needs to be bi directional. A ceramic transient voltage suppressor (2x B72540T6500S162) CT2220K50E2G was used to clamp this huge surge of current. According to it's datasheet it can clamp 500 A of current to 150 V. Note that the lightning strike can be positive or negative. The worst case voltage is dropped across the OR-ing FETs when the strike is positive (–48 V line goes above RTN). If the output of the OR-ing is –48 V and the input goes to +150 V that is a 200 V drop. Thus BSC320N20NS3 was chosen for the OR-ing FETs. This is a 200 V FET with a 32 mΩ R_{DSON} at room temperature. 2 of these were used in parallel to minimize power loss and manage thermal. Finally, a 0.1 µF input bypass cap is recommended.

2.7 EMI Filter Consideration

In this example it is assumed that the EMI filter is right after the hot swap and the bulk cap is after the EMI filter. The EMI filter adds significant inductance and needs to be accounted for. During a Hot Short, the inductor builds up significant current that needs to go somewhere after the FET opens. For that a freewheeling diode should be used along with a snubber. For this example, a 150V, SMA diode was used: STPS1150A. The snubber consisted of a 10-Ω resistor in series with a 1-µF ceramic capacitor. In addition, a 0.1-µF ceramic cap was tied directly on the output.

2.8 Under Voltage and Over Voltage Settings

Both the threshold and hysteresis can be programmed for under voltage and over voltage protection. In general, the rising UV threshold should be set sufficiently below the minimum input voltage and the falling OV threshold should be set sufficiently above the maximum input voltage to account for tolerances. For this example, a rising UV threshold of 37 V and a falling UV threshold of 35 V was chosen as the target. First, choose R_{UV1} based on the 2 V UV hysteresis as shown below.

$$R_{UV1} = \frac{V_{UV,hyst,tgt}}{I_{UV,hust}} = \frac{2V}{10\mu A} = 200k\Omega \qquad (24)$$

Once R_{UV1} is known R_{UV2} can be computed based on the target rising UV threshold as shown below.

$$R_{UV2} = \frac{R_{UV1}}{V_{UV,TGT,Rising} - 1V} = \frac{200k\Omega}{37V - 1V} = 5.56k\Omega \qquad (25)$$

The OV setting can be programmed in a similar fashion as shown in equations below.

$$R_{OV1} = \frac{V_{OV,hyst,tgt}}{i_{OV,hust}} = \frac{3V}{10\mu A} = 300k\Omega \qquad (26)$$

$$R_{OV2} = \frac{R_{OV1}}{V_{OV,TGT,Rising} - 1V} = \frac{300k\Omega}{65V - 1V} = 4.68k\Omega \qquad (27)$$

Optional filtering capacitors can be added to the UV and OV to improve immunity to noise and transients on the input bus. These should be tuned based on system requirements and input inductance. In this example place holders were added to the PCB, but the components were not populated.

2.9 Choosing R_{VCC} and C_{VCC}

The VCC is used as internal supply rail and is a shunt regulator. To ensure stability of internal loop a minimum of 0.1 µF is required for C_{VCC}. To ensure reasonable power on time it is recommended to keep C_{VCC} below 1 µF. R_{VCC} should be sized in such a way to ensure that sufficient current is supplied to the IC at minimum operating voltage corresponding to the falling UV threshold. To allow for some margin it is recommended that the current through R_{VCC} is at least 1.2x of $I_{Q,MAX}$ when RTN = Falling UV threshold and VCC = 10 V (minimum recommended operating voltage on VCC). For this example, R_{VCC} of 10 kΩ was used., which assumes two 20kΩ resistances in parallel.

2.10 Power Good Interface to Downstream DC/DC

It's critical to keep the downstream DC/DC off while the hot swap is charging the bulk capacitor. This can be accomplished through the PGb pin. Note that the VEE of the hot swap and the DC/DC are different and the Power Good can not be directly tied to the EN or UV of the DC/DC. The application circuit below provides a simple way to control the downstream converter with the PGb pin of the hot swap.

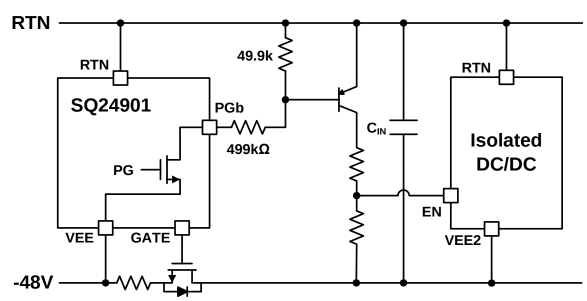


Figure 10. Interface to DC/DC

PCB Layout Guide

There are several things to keep in mind during layout of the SQ24901 circuit:

1. The VEE and SNS pin need to have a Kelvin Sense connection to the sense resistor.

2. The VEE trace carries current and needs to be thick and short in order to minimize IR drop and to avoid introducing current sensing error.

3. Connect the Neg48V filtering caps, UVEN resistor divider, OV resistor divider, and TMR cap to the "VEE" to insure maximum accuracy.

4. The filtering caps on Neg48V and SNS should be placed as close to the IC as possible.

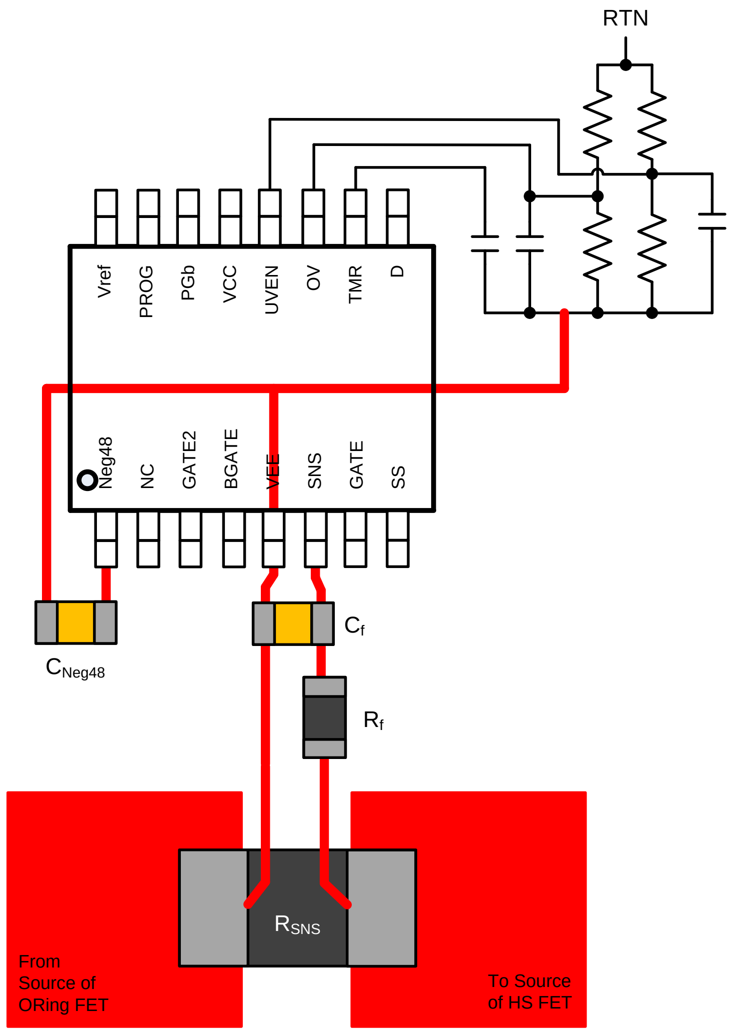
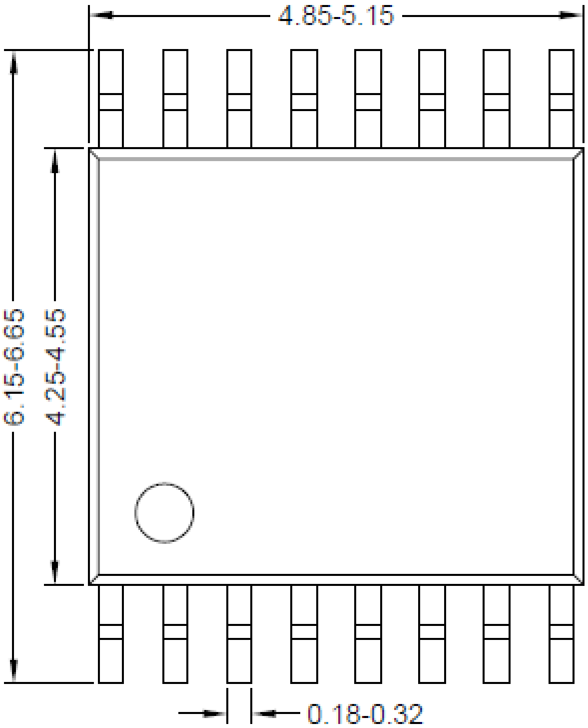
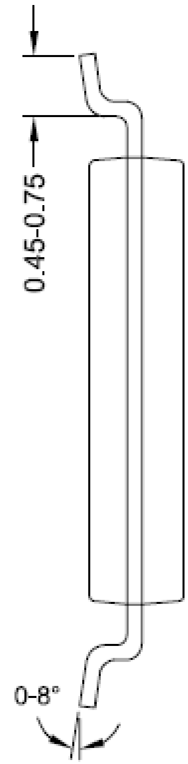


Figure 11. PCB Layout Suggestion

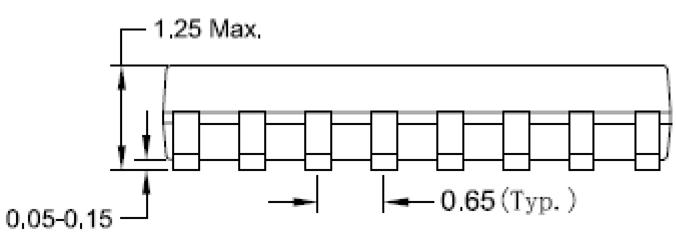
TSSOP16 Package Outline Drawing

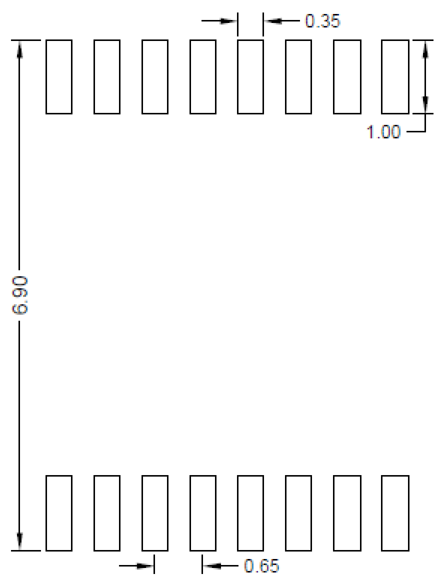


Top view



Side view A





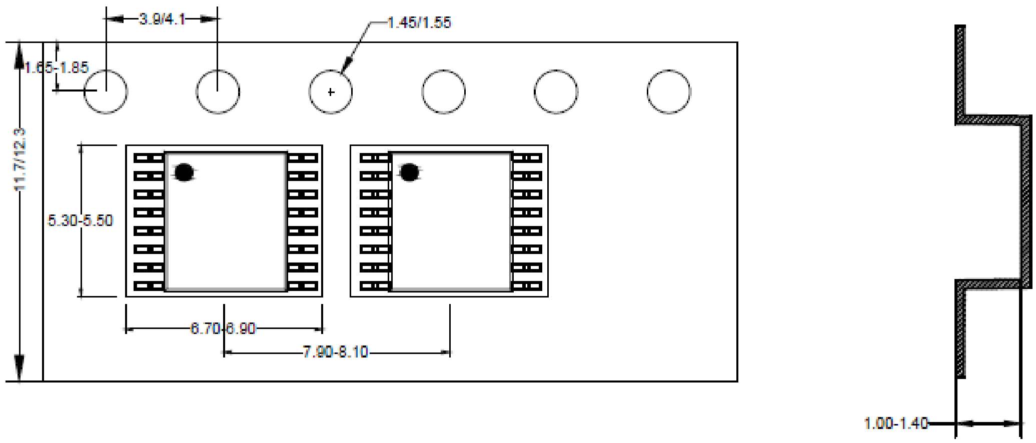
Side view B

Recommended PCB Layout

Notes: **All dimension in millimeter and exclude mold flash & metal burr.**

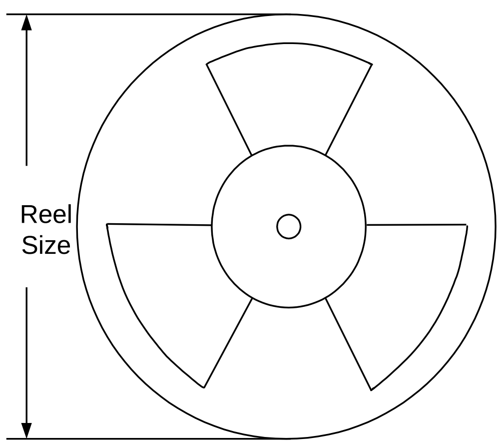
Taping & Reel Specification

1. TSSOP16 Taping orientation



Feeding direction →

2. Carrier Tape & Reel specification for packages



Package types	Tape width (mm)	Pocket pitch(mm)	Reel size (Inch)	Trailer * length(mm)	Leader * length (mm)	Qty per reel (pcs)
TSSOP16	12	8	13"	400	400	3000

3. Others: NA

Revision History

The revision history provided is for informational purpose only and is believed to be accurate, however, not warranted. Please make sure that you have the latest revision.

Date	Revision	Change
Jan.13, 2021	Revision 0.9	Initial Release

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