SY67626

26V 6.5A Three-phase BLDC Motor Driver

General Description

The SY67626 is designed for three-phase brushless DC (BLDC) motor driver. The SY67626 integrates three half-bridges, which have low on-state resistance. The SY67626 includes several protections, such as over current protection, short circuit protection, under voltage protection and thermal shutdown. Low-power shutdown mode and standby mode are also provided.

Ordering Information

SY67626 □(□□□)

Package Code

Optional Spec Code

Ordering Number	Package Type	Note
SY67626RPQ	QFN5×5-40	

Features

- Power Supply Voltage Range from 5V to 26V
- Integrated Three Half-Bridges Motor Driver
- Maximum 6.5A Peak Current
- Shutdown Mode
- Standby Mode
- Over Current Protection
- Under Voltage Protection
- Short Circuit Protection
- Thermal Shutdown
- Fault Output

Applications

- 3-Phase BLDC Motor Driver

Typical Application

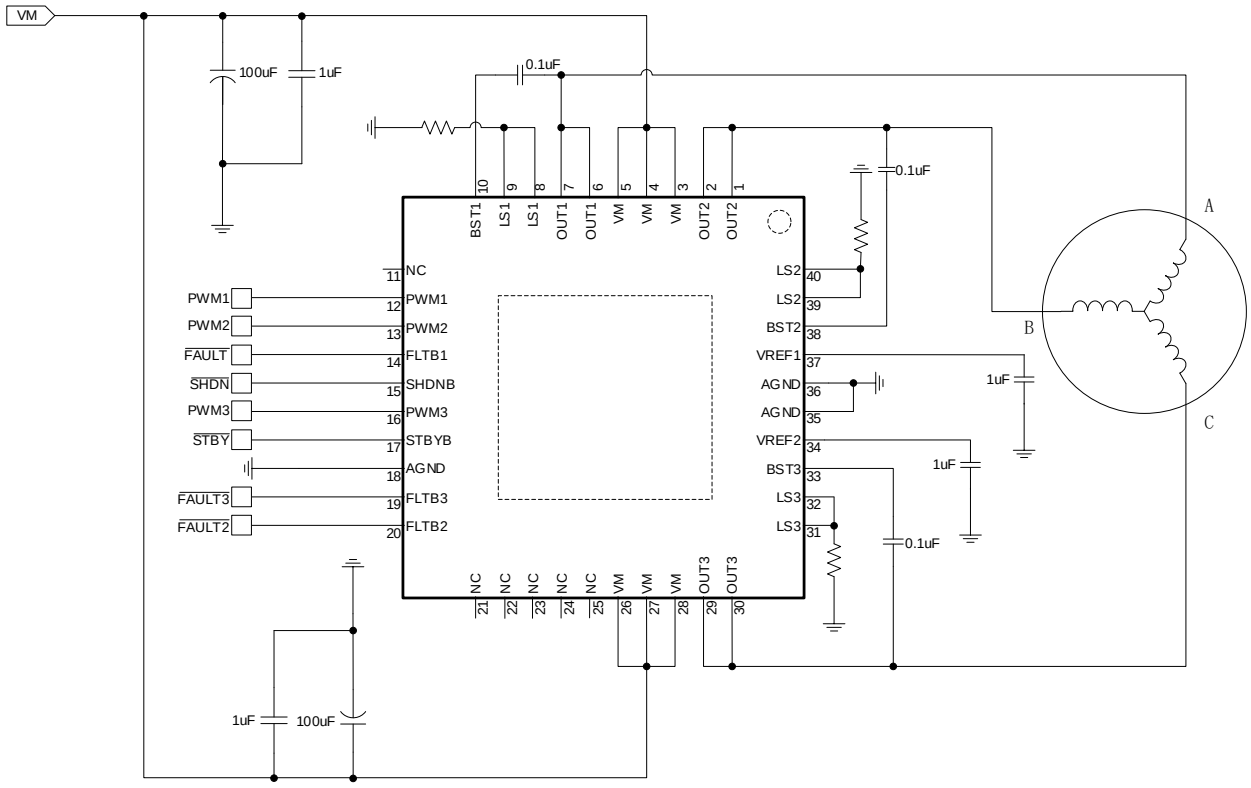
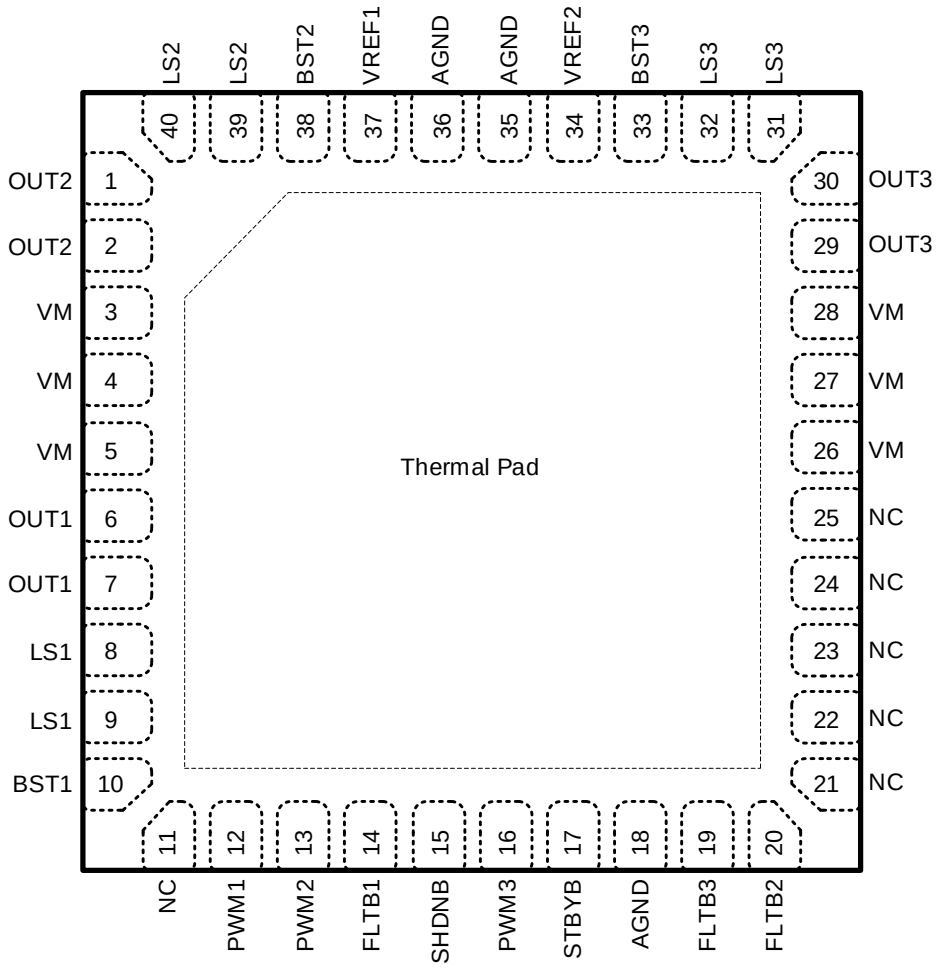


Figure 1. Typical Application Schematic

Pinout (Top View)



(QFN5×5-40)

Top Mark: EEF*xyz* (device code: **EEF**, ***x=year code, y=week code, z= lot number code)***

Pin Name	Pin No.	Pin Description
OUT2	1,2	Half bridge 2 output.
VM	3,4,5	Power supply pin. Decouple this pin to AGND pin with at least 1uF ceramic cap.
OUT1	6,7	Half bridge 1 output.
LS1	8,9	Half bridge 1 low side power MOSFET source connection.
BST1	10	Half bridge 1 high side gate driver bootstrap supply. Connect an at least 0.1uF capacitor between BST1 and OUT1.
NC	11	No connection.
PWM1	12	Half bridge 1 driver logic input. PWM1=high, half bridge 1 high side MOSFET turns on; PWM1=low, half bridge 1 low side MOSFET turns on.
PWM2	13	Half bridge 2 driver logic input. PWM2=high, half bridge 2 high side MOSFET turns on; PWM2=low, half bridge 2 low side MOSFET turns on.
FLTB1	14	Fault output, open drain output. When over current protection or thermal shutdown happens, FLTB1 is pulled logic low.
SHDNB	15	Shutdown input. SHDNB=low, the IC enters into shutdown mode.

PWM3	16	Half bridge 3 driver logic input. PWM3=high, half bridge 3 high side MOSFET turns on; PWM3=low, half bridge 3 low side MOSFET turns on.
STBYB	17	Standby input. Default low, if STBYB=high, the output is determined by PWMx; If STBYB=low, the outputs are high Z.
AGND	18	Analog ground.
FLTB3	19	Fault monitor 3, open drain output.
FLTB2	20	Fault monitor 2, open drain output.
NC	21,22,23,24,25	No connection.
VM	26,27,28	Power supply pin. Decouple this pin to AGND pin with at least 1uF ceramic cap.
OUT3	29,30	Half bridge 3 output.
LS3	31,32	Half bridge 3 low side power MOSFET source connection.
BST3	33	Half bridge 3 high side gate driver bootstrap supply. Connect an at least 0.1uF capacitor between BST3 and OUT3.
VREF2	34	Gate driver supply bypass. VREF2 powers gate driver for OUT1、OUT2 and OUT3. Connect an at least 1uF capacitor between VREF2 and AGND.
AGND	35,36	Analog ground.
VREF1	37	The VREF1 supplies the analog circuits. Connect an at least 1uF capacitor between VREF1 and AGND.
BST2	38	Half bridge 2 high side gate driver bootstrap supply. Connect an at least 0.1uF capacitor between BST2 and OUT2.
LS2	39,40	Half bridge 2 low side power MOSFET source connection.
Thermal Pad	-	The exposed pad must be connected to AGND through soldering PCB for better thermal spreading.

Block Diagram

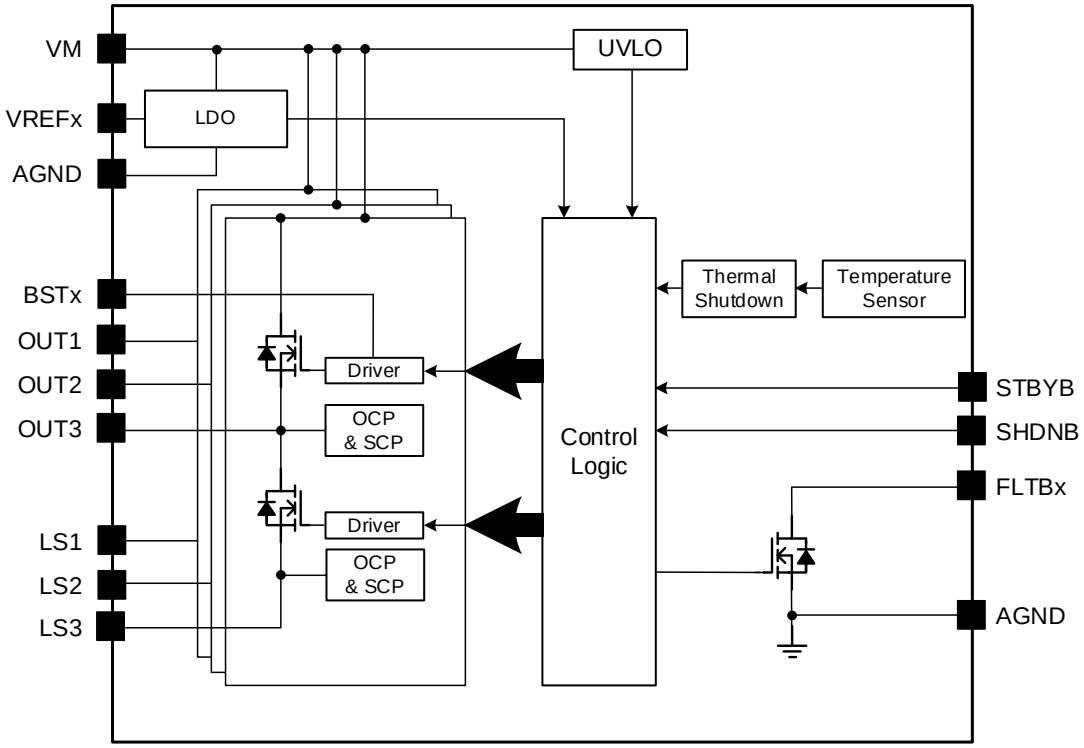


Figure 2. Block Diagram

Absolute Maximum Ratings (Note 1)

VM ---------- -0.3V to 28V
OUTx ---------- -0.3V to VM+0.3V
BSTx to OUTx ---------- -0.3V to 4V
LSx ---------- -0.3V to 1V
FLTB1, FLTB2, FLTB3 ---------- -0.3V to 7V
PWMx, STBYB, SHDNB ---------- -0.3V to 7V
VREF1, VREF2 ---------- -0.3V to 4V
Junction Temperature (T_J) ---------- -40°C to +150°C
Storage Temperature ---------- -55°C to +150°C
Package Thermal Resistance (Note 2)
θ_{JA} ---------- 27.5°C/W
θ_{JC} ---------- 18.8°C/W

Recommended Operating Conditions

VM ---------- 5V to 26V
OUTx ---------- -0.1V to VM+0.1V
BSTx to OUTx ---------- -0.1V to 3.3V
LSx ---------- -0.1V to 0.2V
FLTB1, FLTB2, FLTB3 ---------- -0.1V to 5.5V
PWMx, STBYB, SHDNB ---------- -0.1V to 5.5V
VREF1, VREF2 ---------- -0.1V to 3.3V
Junction Temperature Range ---------- -40°C to 125°C

Electrical Characteristics

(T_A = 25°C, VM=12V, V_{SHDNB}=5V, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Power Supplies						
VM Operating Supply Current	I_{VM}	OUTx Open, PWMx=0		2.3		mA
VM Shutdown Current	I_{VMSTD}	V_{SHDNB}=0V		32		uA
VM Under Voltage Lockout Voltage	V_{UVLO_RISE}	VM Rising		4.4	4.8	V
	V_{UVLO_FALL}	VM Falling	3.7	4		V
VREF1, VREF2						
LDO Output Voltage	V_{VREF}	I_{Load}=30mA		3.25		V
H-Bridge MOSFETs						
High Side MOSFETs On Resistance	R_{dson_H}	VM=5V		70		mΩ
Low Side MOSFETs On Resistance	R_{dson_L}	VM=5V		70		mΩ
Off-State Leakage Current	I_{OFF}	V_{SHDNB}=V_{STBYB}=0V, V_{DS}=28V	-2		2	μA
BST						
BST Current	I_{BST}	High Side MOSFET On, V_{BST} –V_{OUT}=3.3V		65		μA
BST Under Voltage Lockout Voltage	V_{BST_UV}	V_{BST} Falling		1.9		V
Timing						
OUTx Switching Frequency	F_{OUT}	50% Duty			1	MHz
Minimum PWM Pulse Width	T_{MIN}			60		ns
PWMx to OUTx Delay Time Rising	T_{DR}	V_{PWMx}=0V to 5V		100		ns
PWMx to OUTx Delay Time Falling	T_{DF}	V_{PWMx}=5V to 0V		100		ns
Output Deadtime	T_D	I_{OUT}=±500mA		10		ns
OUTx Rise Time	T_r	V_{PWMx}=0V to 5V		15		ns
OUTx Fall Time	T_f	V_{PWMx}=5V to 0V		5		ns
Logic Input (PWMx, STBYB, SHDNB)						
Input High Voltage	V_H	V_{PWMx}, V_{SHDNB}, V_{STBYB} Rising		1.6	2.0	V
Input Low Voltage	V_L	V_{PWMx}, V_{SHDNB}, V_{STBYB} Falling	0.6	1		V
PWMx Input Bias Current	I_{PWMx}	V_{PWMx}=3.3V		27.5		μA
PWMx Pull Down Resistance	R_{PWMx}			120		kΩ
FLTB1, FLTB2, FLTB3 Output						
Open Drain Output Sink Current	I_{FO}	FLTBx is Low, V_{FLTBx}= 0.2V	5			mA
Protection						
Output Over Current Protection High	I_{OCPH}	V_{PWMx}=0V, Sinking		6.5		A
		V_{PWMx}=5V, Sourcing				
Output Over Current Protection Low	I_{OCPL}	V_{PWMx}=0V, Sinking		3.2		A
		V_{PWMx}=5V, Sourcing				
Over Current Deglitch Time	T_{OCP}	(Note 3)		100		ns
Over Current Retry Time	T_{retry}			30		μs
Short Circuit Deglitch Time	T_{SCP}	(Note 3)		50		ns
Thermal Shutdown Temperature	T_{SD}	(Note 3)		160		℃
Thermal Shutdown Hysteresis	T_{HYS}	(Note 3)		30		℃

Note 1: Stresses listed as the above "Absolute Maximum Ratings" may cause permanent damage to the device. These are for stress ratings. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may remain possibility to affect device reliability.

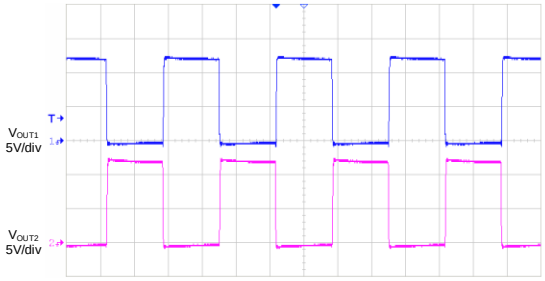
Note 2: θ_{JA} is measured in the natural convection at T_A = 25°C on a high effective 4-layer thermal conductivity test board with four thermals via.

Note 3: Guaranteed by design, not subject to test.

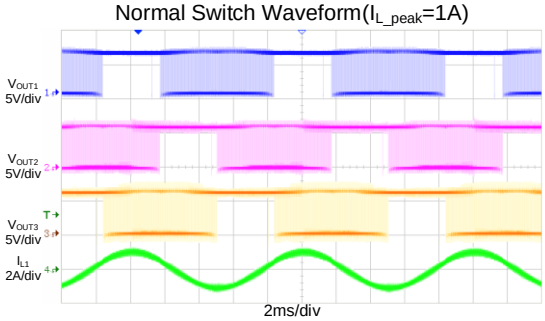
Typical Performance Characteristics

(VM=12V, V_{SHDNB}= 5V, T_A=25℃, unless otherwise specified)

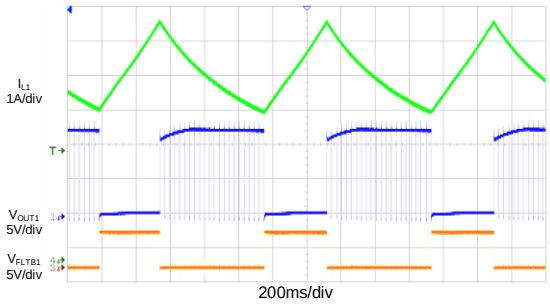
Normal Switch Waveform



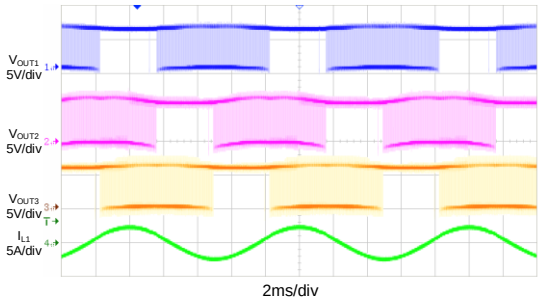
Normal Switch Waveform(I_{L_peak}=1A)



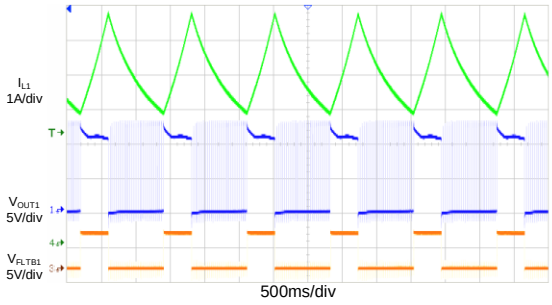
Low Side Output Over Current Protection



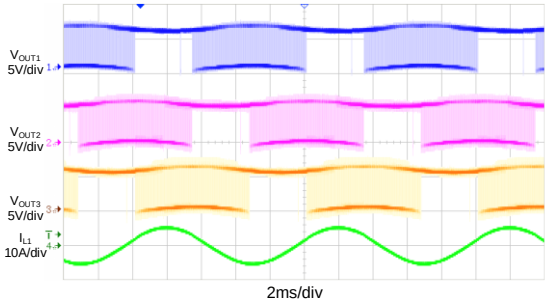
Normal Switch Waveform(I_{L_peak}=2.5A)



High Side Output Over Current Protection



Normal Switch Waveform(I_{L_peak}=5.5A)



Function Description

General Description

The SY67626 is designed for three-phase brushless DC (BLDC) motor driver. The SY67626 integrates three half-bridges, which have low on-state resistance. The SY67626 includes several protections, such as over current protection, short circuit protection, under voltage protection and thermal shutdown.

Standby Mode

When STBYB is low, all FETs are turned off. After the detection time, the FET with current in the body diode will be turned on and enter synchronous rectification mode. When the synchronous rectification mode is over, all FETs are disabled and OUT1/2/3 enter high impedance status, the IC is in standby mode. When STBYB is high, the IC is out of standby mode.

Shutdown Mode

When SHDNB is low and persists for longer than deglitch time, all FETs are turned off. After the detection time, the FET with current in the body diode will be turned on and enter synchronous rectification mode. When the synchronous rectification mode is over, all FETs are disabled, all circuitry in the device will be disabled, and all internal logic will be reset. When OUT1/2/3 enter high impedance status, the IC is in shutdown mode. When SHDNB is high, the IC is out of shutdown mode.

Protection Circuits

Over Current Protection (OCP)

A current limit circuit on each FET limits the current through the FET by controlling the gate drive. When the FET current is larger than the limit current (I_{OCPH}) and persists for longer than the OCP deglitch time (T_{OCP}), all FETs in three half-bridges will be disabled and OUT1/2/3 will enter high impedance status. The driver will be re-enabled after the OCP retry period (T_{retry}) has passed. If the current is still larger than the lower limit of over current protection (I_{OCPL}) during the deglitch time ($T_{deglitch}$), the cycle repeats. When the current falls below the lower limit of over current protection (I_{OCPL}) and persists for longer than deglitch time ($T_{deglitch}$), normal operation resumes.

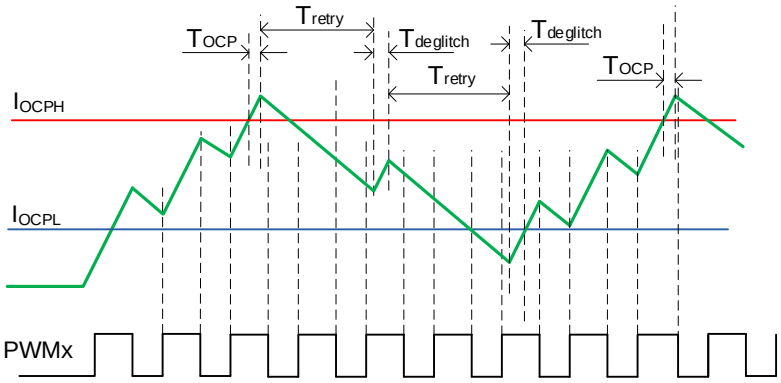


Figure 3. OCP Operation Waveform

Under Voltage Lockout (UVLO)

If at any time the VM voltage falls below the under-voltage lockout threshold voltage, all circuits in the device will be disabled, and all internal logic will be reset. Operation will resume when VM voltage rises above the UVLO threshold voltage.

Thermal Shutdown (TSD)

If the die temperature exceeds approximately 160°C, all FETs are turned off. After the detection time, the FET with current in the body diode will be turned on and enter synchronous rectification mode. When the synchronous rectification mode is over, all FETs are disabled until the temperature drops to safe working temperature.

Any tendency of the device to enter thermal shutdown is an indication of either excessive power dissipation, insufficient heatsinking, or too high ambient temperature.

Fault Output

The IC provides fault output pins, when TSD or OCP happens, the FLTB1 is pulled low.

When OCP or UVLO occurs, FLTB2 is pulled low and remains low until power up, exits from standby mode or shutdown mode. FLTB3 follows the same latch logic.

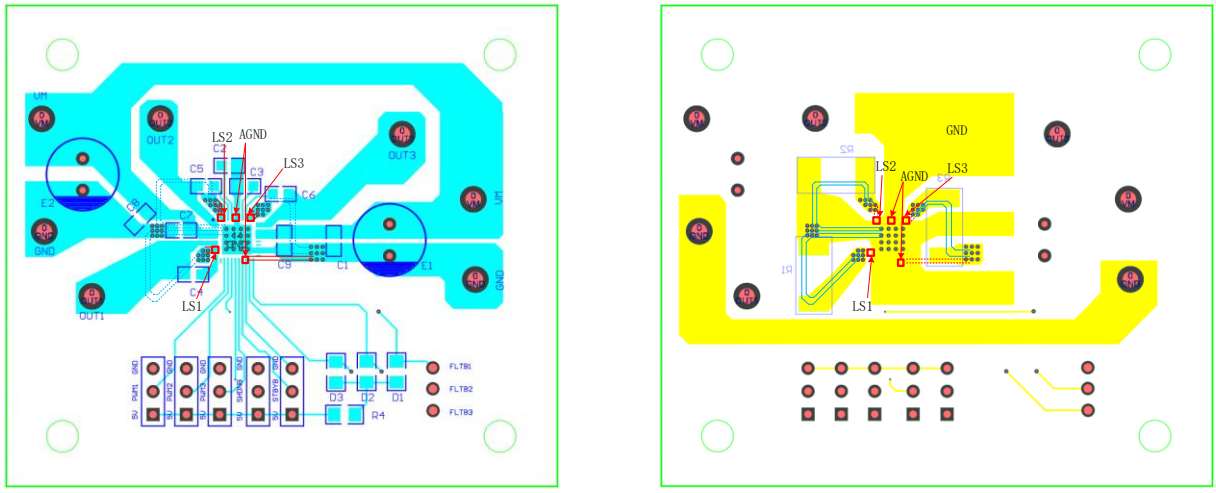
Table 1. Fault Reporting

OCP	TSD	UVLO	FLTB1	FLTB2	FLTB3
0	0	0	1	1	1
0	0	1	1	0	1
0	1	0	0	1	0
1	0	0	0	0	0

Layout Design

The layout design of the SY67626 is relatively simple.

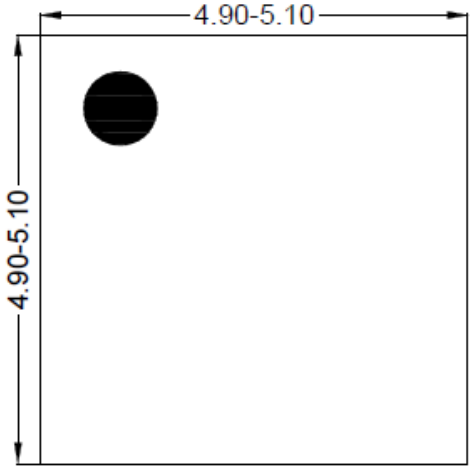
1) It is desirable to maximize the PCB copper area connecting to AGND pin to achieve the best thermal and noise performance. If the board space allowed, a ground plane is highly desirable.
2) The trace connecting the LS to GND pin must be minimized and NOT be adjacent to the logic input pins on the PCB layout to avoid the noise problem.



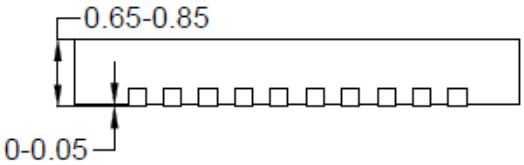
(a) (b)

Figure 4. PCB Layout Suggestion (a) Top Layer (b) Bottom Layer

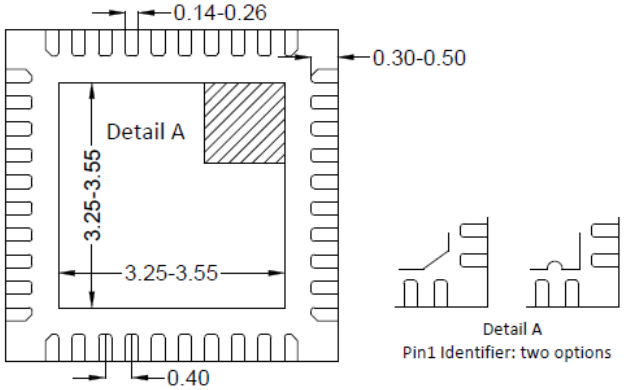
QFN5×5-40 Package Outline Drawing



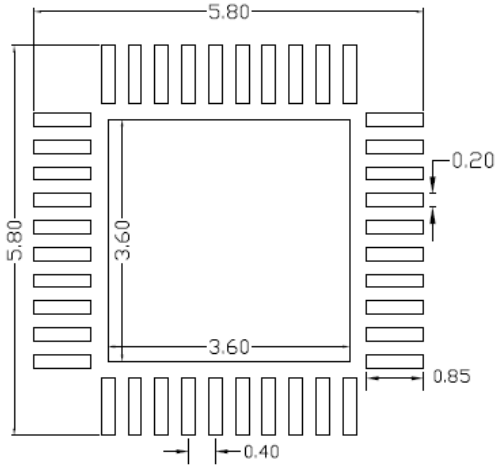
Top View



Side View



Bottom View

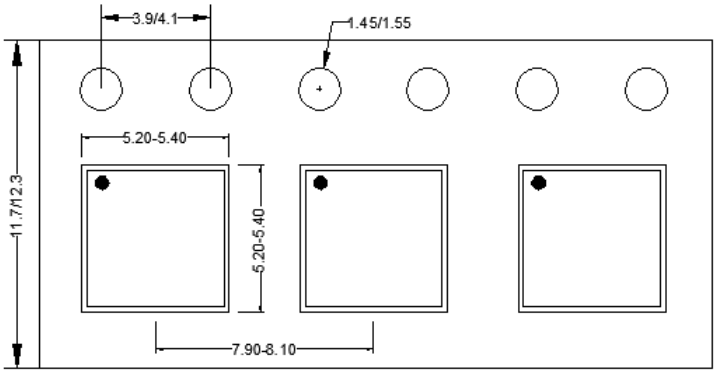


Recommended PCB Layout
(Reference only)

Notes: All dimension in millimeter and exclude mold flash & metal burr.

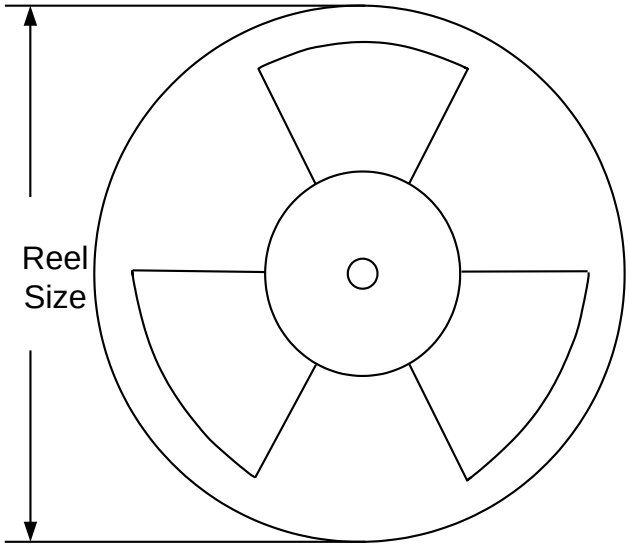
Taping & Reel Specification

1. QFN5×5 Taping Orientation



Feeding direction →

2. Carrier Tape & Reel specification for packages



Package Type	Tape Width (mm)	Pocket Pitch(mm)	Reel Size (Inch)	Trailer Length(mm)	Leader Length (mm)	Qty per Reel
QFN5×5	12	8	13"	400	400	5000

3. Others: NA

Revision History

The revision history provided is for informational purpose only and is believed to be accurate, however, not warranted. Please make sure that you have the latest revision.

Revision Number	Revision Date	Description
Rev 0.9	August 28, 2023	Initial Release
Rev 1.0	August 28, 2024	Production Release

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