SY67343

Three Phase Sensorless Sine Wave Motor Driver with Integrated Power MOSFETs

General Description

The SY67343 is designed for sensorless control of three-phase brushless DC (BLDC) motor, especially for low noise, low external component count and high efficiency applications. The SY67343 also integrates three half-H-bridges, which have low turn on resistance. A 180° modified SPWM is used to reduce the motor noise and torque ripple. The device can be easily configured through an I^2C interface to drive different motors.

The SY67343 supplies several protections and abnormal state detections to ensure reliable operation of the motor, such as over current protection, short circuit protection, under voltage lockout, thermal shutdown and abnormal motor states protection. A low-power sleep mode is also provided.

To be compatible with industry-standard devices, the SY67343 package is 24-pin TSSOP24E.

Features

- Power Supply Voltage Range from 5V to 40V
- Maximum Drive Current of 2A RMS, 3A Peak Current
- Sine Wave Driver
- Integrated 5V or 3.3V Buck Regulator
- I^2C Interface
- Speed Setting: PWM/ Analog/I^2C
- Forward/Reverse Control
- Sleep Mode
- Over Current Protection
- Motor Lock Protection
- Under Voltage Protection
- Thermal Shutdown
- TSSOP24E Package

Applications

- Appliance Fan
- HVAC

Ordering Information

SY67343 □(□□□)

Package Code

Optional Spec Code

Ordering Number	Package type	Note
SY67343HHP	TSSOP24E	

Typical Application

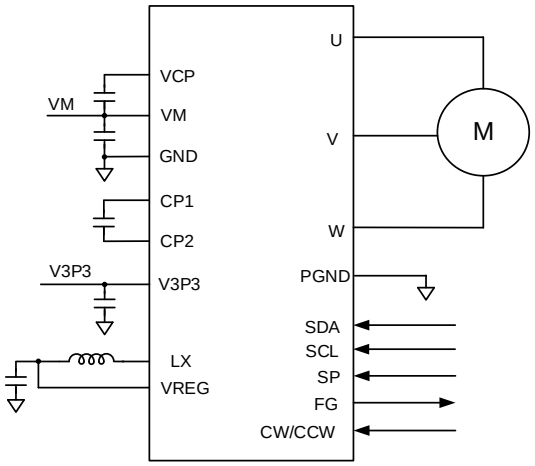
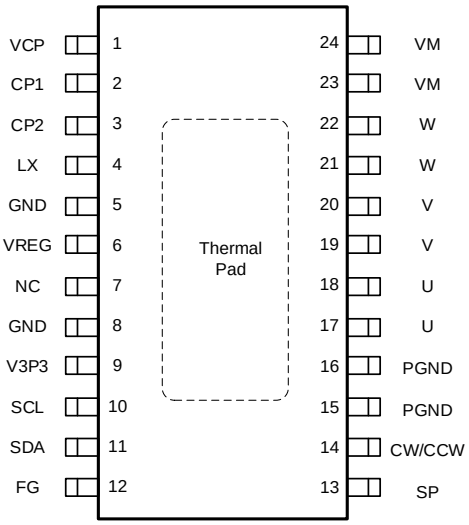


Figure 1. Typical Application Circuit

Pin out (Top View)



(TSSOP24E)

Top Mark: **FDY*xyz***, **(**Device code: FDY; ***x=year code, y=week code, z= lot number code***)

Pin No.	Pin Name	Pin Description
1	VCP	High side gate drive voltage supply. Connect a 100nF capacitor to VM.
2	CP1	Charger pump capacitor. Connect a 100nf capacitor between CP1 and CP2.
3	CP2	
4	LX	Internal regulator switching node. Connect a 47uH inductance at this PIN.
5	GND	Step down regulator ground.
6	VREG	Step down regulator output and feedback pin. Connect a 10uF/6.3V ceramic capacitor at this pin.
7	NC	Not connected
8	GND	Analog power ground.
9	V3P3	3.3V LDO output pin. Connect a 1uF/6.3V capacitor to GND.
10	SCL	I²C clock input pin.
11	SDA	I²C data signal pin.
12	FG	Motor electrical period output pin, open drain output, need a pull up resistor.
13	SP	Speed control signal input pin. This pin supports PWM or analog speed control signal input.
14	CW/CCW	Motor direction control pin.
15	PGND	Power ground.
16		
17	U	Motor U phase driver pin.
18		
19	V	Motor V phase driver pin.
20		
21	W	Motor W phase driver pin.
22		
23	VM	Motor power supply pin. Decouple this pin to GND pin with at least 10uF ceramic cap.
24		
-	Thermal Pad	The exposed pad must be connected to PGND through soldering PCB for better thermal spreading.

Block Diagram

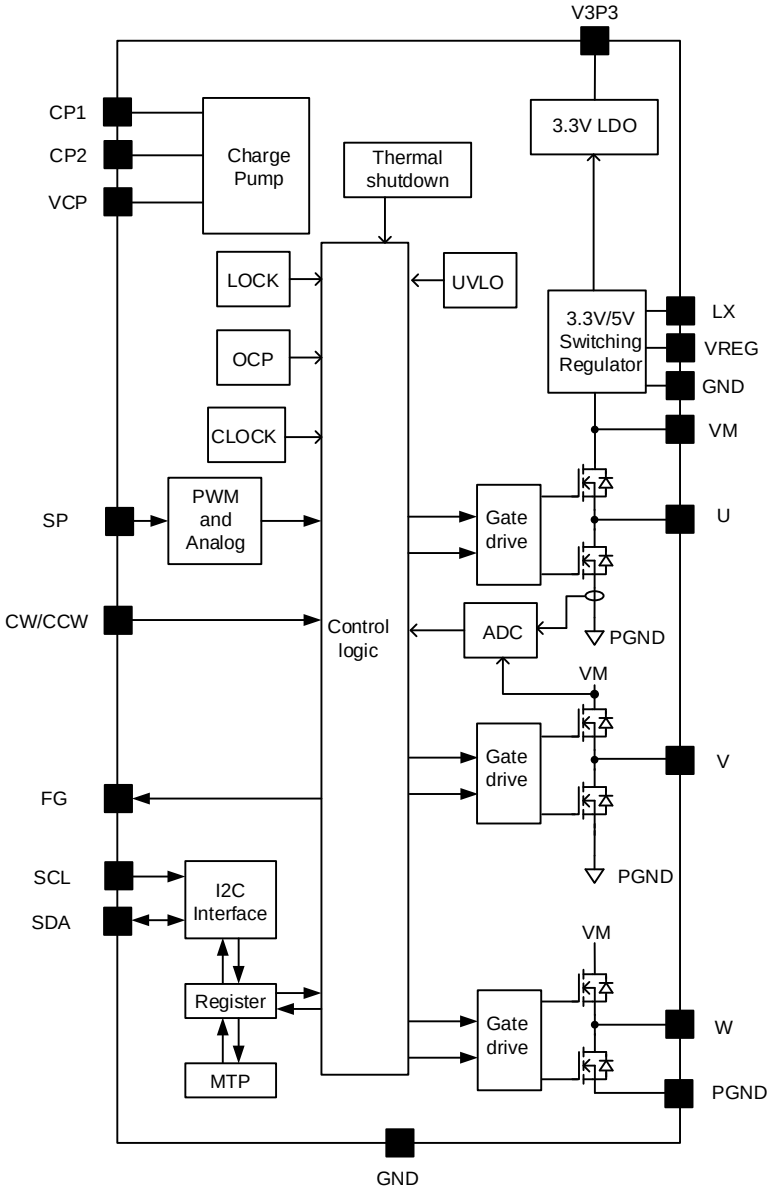


Figure 2. SY67343 Block Diagram

Absolute Maximum Ratings (Note 1)

VM ---------- -0.3 to 40V
U, V, W ---------- -0.7 to 40V
VCP, CP1, CP2---------- -0.3 to 40V
SP ---------- -0.3 to 5.5V
SCL, SDA, CW/CCW---------- -0.3 to 5.5V
LX ---------- -0.3 to 40V
VREG ---------- -0.3 to 6V
FG ---------- -0.3 to 5.5V
V3P3 ---------- -0.3 to 4V
Junction Temperature (T_J) ---------- -40°C to +150°C
Storage Temperature ---------- -55°C to +150°C
Package Thermal Resistance
θ_{JA} (Note 2) ---------- 36.1°C/W
θ_{JC} ---------- 17.4°C/W

Recommended Operating Conditions

VM ---------- 5 to 32V
U, V, W ---------- -0.5 to 32V
SP ---------- -0.1 to 5V
FG---------- -0.1 to 5V
SCL, SDA, CW/CCW---------- -0.1 to 5V
Step down regulator output current (I_{buck} @T_A=25°C, BKIPSET=10) ---------- < 100mA
V3P3 LDO output current (I_{3P3_LDO}) ---------- ---------- 0 to 5mA
Junction Temperature Range ---------- -40°C to 125°C
Ambient Temperature Range ---------- -40°C to 85°C

Electrical Characteristics

(T_A = 25°C, VM=24V, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Power Supplies						
VM Operating Supply Current	I_{VM}	VM=24V, Buck disable		4.2	6	mA
VM Sleep Mode Current	I_{VMSLP}	VM=24V, SP=0V, sleep mode		220	300	μA
VM Undervoltage Lockout Voltage	V_{UVLO_RISE}	VM Rising	4.1	4.5	4.9	V
	V_{UVLO_HYS}	VM Hysteresis		300		mV
Stepdown Regulator						
Step down Regulator Output Voltage	V_{REG}	L_{LX}=47μH,C_{VREG}=10μF, VregSel=0	4.75	5	5.25	V
		L_{LX}=47μH,C_{VREG}=10μF, VregSel=1	3.25	3.4	3.55	V
Maximum Load from V_{REG}	I_{REG_MAX}	T_A = 25°C , L_{LX}=47μH, C_{VREG}=10μF,BKIPSET=10		100		mA
3.3V LDO						
3.3V LDO Output Voltage	V_{3P3}	Iout=0 to 5mA	3.1	3.3	3.5	V
3.3V LDO Output Current	I_{3P3_LDO}	(Note4)			5	mA
H-Bridge MOSFETs						
High Side+ Low Side MOSFETs on Resistance	R_{dson}			200	240	mΩ
Off-State Leakage Current	I_{OFF}		-1		1	μA
Output Deadtime	T_D	(Note4)		100		ns
SPEED Control---Analog						
Analog Full Speed Voltage	V_{AFS}	(Note4)		V_{3P3}*0.9		V
Analog Zero Speed Voltage	V_{AZS}			0.2		V
Analog Voltage Resolution	V_{AVR}			10.8		mV
Analog Startup Voltage	V_{ASV}	Standby mode	0.4			V
Analog Startup Voltage	V_{ASV}	Sleep mode	2.2			V
SPEED Control---Digital						
Input High Voltage	V_{DSPH}		2.2			V
Input Low Voltage	V_{DSPL}				0.8	V
Input Frequency	F_{DSPF}	(Note4)	1		100	kHz
CW/CCW input						
Input High Voltage	V_{CWH}		2.2			V
Input Low Voltage	V_{CWL}				0.6	V
FG output						
FG Output Sink Current	I_{FG}		5			mA
SLEEP condition						
Analog Voltage to Enter Sleep Mode	V_{AENSLP}	Spctrmd=0(analog mode)			100	mV
Digital Voltage to Enter Sleep Mode	V_{DENSLP}	Spctrmd=1(digital mode)			0.8	V
Analog Voltage to Exit Sleep Mode	V_{AEXSLP}		2.2			V
Digital Voltage to Exit Sleep Mode	V_{DEXSLP}		2.2			V
Time to Exit from Sleep Mode	T_{EXSLP}	(Note4)		1		μs
Time to Enter Sleep Mode	T_{ENSLP}	(Note4)		10		ms

Lock detection						
Lock Release Time	T_{LCKR}	(Note4)		5		s
Lock Enter Time	T_{LCKEN}	(Note4)		0.3		s
Protection						
Output Over Current Limit	I_{OCP}		3.5	4.5		A
Thermal Shutdown Temperature	T_{SD}	(Note4)		150		℃
Thermal Shutdown Hysteresis	T_{HYS}	(Note4)		10		℃
I²C INTERFACE						
Input High Voltage	V_{I^2CH}		2.2			V
Input Low Voltage	V_{I^2CL}				0.6	V
SCL Clock Frequency	f_{SCL}	(Note4)	0		400	kHz
Bus Free Time Between Stop/Start	t_{BUF}	(Note4)	1.3			μs
Start Condition (Repeated) Hold Time	$t_{HD,STA}$	(Note4)	600			ns
Repeat START Set up Time	$t_{SU,STA}$	(Note4)	600			ns
Set up Time for STOP	$t_{SU,STO}$	(Note4)	600			ns
Data Set up Time	$t_{SU,DAT}$	(Note4)	100			ns
Data Hold Time	$t_{HD,DAT}$	(Note4)	0		900	ns
Data Output Fall Time	t_{Of}	(Note3,4)	$20+0.1C_B$		300	ns

Note 1: Stresses listed as the above "Absolute Maximum Ratings" may cause permanent damage to the device. These are for stress ratings. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may remain possibility to affect device reliability.

Note 2: θ_{JA} is measured in the natural convection at T_A = 25°C on a low effective single layer thermal conductivity test board of JEDEC 51-3 thermal measurement standard.

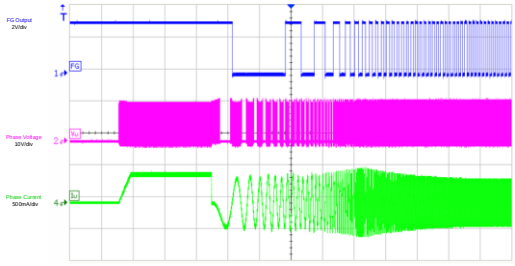
Note 3: C_B is total capacitance of one bus line in pF (C_B<=400pF).

Note 4: Guaranteed by design, not subject to test.

Operation Waveforms

Start-up Waveform

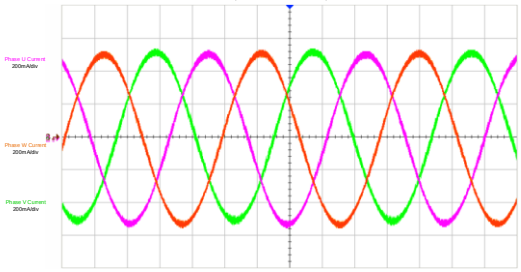
CH1:FG Output;CH2:Phase Voltage;CH4:Phase Current



500ms/div

Operation Current Waveform

CH2:Phase U Current;CH3:Phase V Current;CH4:Phase W Current



2ms/div

Functional Description

The SY67343 is designed for sensorless control of three-phase BLDC motor, especially for low noise, low external component count and high efficiency applications. A 180° modified SPWM is used to reduce the motor noise and torque ripple. The device can be easily configured through an I²C interface to drive different motors.

The device supplies several protection and abnormal state detect to ensure reliable operation of the motor. The abnormal rotor lock state is detected through different methods. Over current, under voltage lockout and thermal shutdown prevent the device and motor from being damaged.

A buck regulator steps down the input voltage efficiently to provide power for the internal circuits. The output can also be used to power the external circuit such as a microcontroller.

Flexible interfaces have designed in this device. In addition to the I²C interface, the system also provides discrete SP pin, CW/CCW pin and FG pin. The SP is the speed command input pin both for digital PWM input and analog input. CW/CCW pin controls the motor direction. FG pin is the speed output pin which shows the motor communication frequency. The user can adjust the motor speed by varying the supply voltage (VM) or by controlling the speed command. The speed command can be given through the PWM input or the analog input or the I²C command.

Motor Parameters

Three parameters of the motor need to be configured in the register to successfully control the motor: motor resistance, inductance, velocity constant. The motor resistance is programmed by writing the values for Rm[11:0] in the MotorPara register. The motor inductance is programmed by writing the values for Lm[11:0] in the MotorPara register. The motor velocity constant is programmed by writing the values for Kt[11:0] in the MotorPara register.

Motor Resistance

The resistance Rm[11:0] is the phase resistor of the motor. The Rm that the device supports is from 0 Ω to 32Ω which represent the digital value changes from 0 to 4095. The LSB of the digital value for the Rm is 1/128Ω.

Motor Inductance

The inductance Lm[11:0] is the phase inductance of the motor. The Lm that the device supports is from 0 mH to 32mH which represents the digital value changes from 0 to 4095. The LSB of the digital value for the Lm is 1/128 mH.

Motor Velocity Constant

The motor velocity constant Kt[11:0] is the peak value of the motor phase to phase Back Electro Motive Force (BEMF). The Kt that the device supports is from 0 mV/Hz to 2000mV/Hz which represents the digital value changes from 0 to 4095. The LSB of the digital value for the Kt is 1/2048V/Hz.

Start the Motor under Different Initial Conditions

This section introduces the startup of the motor under different initial conditions. There are three different states of the motor before the device attempts to exceed the startup process: stationary, spinning in the forward direction or spinning in the reverse direction. Several options are provided to make sure the motor can start up successfully.

Motor Initial State Detect

The motor initial state is essential for the startup process. Two phase to phase comparators are used to detect the motor initial state while it is coasting (motor phase are in high impedance state before the start). The zero crossings of the phase-to-phase BEMF voltage can be detect if the motor is spinning.

Start the Motor under the Stationary State

If the motor is stationary, two methods are available to get the initial position of the rotor: the Align method and the PSD (position state detect) method. The Align method forces the rotor to an align position by supplying a voltage with given position and amplitude for a certain time. This method could cause the rotor rotating through a small angle and oscillation during the align time. If the rotation and oscillation is not acceptable, the PSD method can be used. The PSD method detects the initial rotor position based on the inductance variation around the electrical cycle by injecting a sequence of high frequency voltage pulses.

Align

The device aligns a motor by injecting a DC voltage with the current flowing from phase U to phase V and phase W for a certain time. The amplitude and duration of the voltage should change with different applications. The motor with bigger inertia needs a bigger voltage and longer time. To avoid a sudden current change, current ramp is used during the alignment.

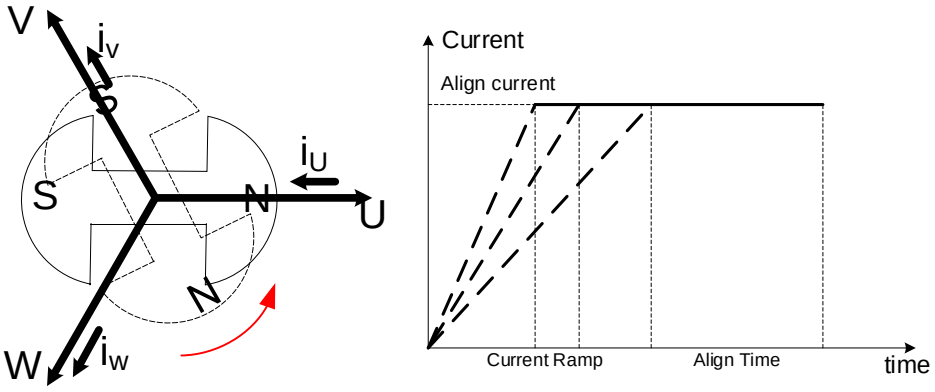


Figure 3. Align Voltage and Rotor Position Synchronization

PSD

The PSD method is used where the rotor reverse rotation and oscillation are not acceptable because this method does not need to align the rotor to a given position. The PSD obtains the rotor position by injecting six voltage pulses and detecting the bus current. The voltage pulses are generated by applying voltage across two motor phases as follows: UV, UW, VW, VU, WU and WV. The voltage lasts until the current reaches the threshold set inside the device. The device measures the time from when the voltage is applied until the current reaches the threshold. The PSD current threshold is determined by the PSD current threshold setting (PSDCurrThr[2:0]).

Start the Motor with the Detected Position

If the motor is stationary, the rotor position is obtained after Align or PSD process. The device begins to accelerate the motor from a certain position. The motor is accelerated by applying a rotating voltage vector given by open loop setting. The amplitude of the voltage is determined by the open loop current setting (OpenLCurr[2:0]). The rotating speed of the voltage vector is determined by the open loop start acceleration setting (StAccel1[2:0], StAccel2[2:0]). As the motor needs a minimum speed to generate sufficient BEMF for the communication logic, an open to close threshold speed need to be set in Op2ClsThr[4:0]. Figure 4 shows the open loop start up process of the motor.

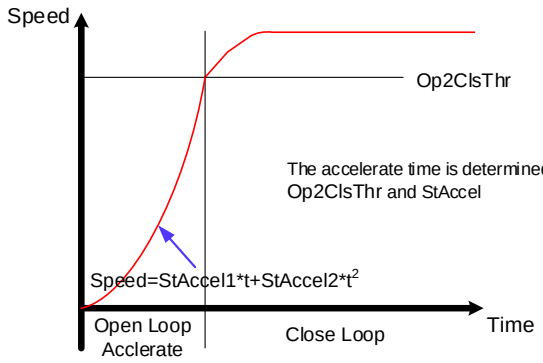


Figure 4. Open Loop Motor Start Up

The amplitude of the open loop voltage is given by Equation 1, where U_{st} is the open loop voltage amplitude, Kt is motor velocity constant configured by Kt[11:0], Rm is the motor resistance configured by Rm[11:0], I_{st} is the open loop current configured by OpenLCurr[2:0]. The motor with large inertia needs a big I_{st}

$$U_{st}=I_{st}\times Rm+Kt\times Speed \quad (1)$$

Start up When the Motor is spinning in the Forward Direction

If the motor is spinning forward, the initial state detect function can get the rotor communication period and the rotor position when the comparator output changes. So the motor can be started at the moment when the comparator changes. The method provides a quick startup of the motor in this situation.

Start up When the Motor is spinning in the Reverse Direction

If the motor is spinning in the reverse direction, two options are provided to start the motor: Brake or Reverse drive. The Reverse drive is enabled if RvsDrEn=1. The reverse drive voltage can be selected by setting the VolReverseSel[2:0]. The device applies a reverse rotated voltage to drive the motor reversely through the zero speed and continue accelerating the motor to close loop. If RvsDrEn=0, the device brakes the motor by turning on all the low-side MOSFETs. When initial state detect function detects the motor has stopped spinning, the device begins to start up the motor.

Figure 5 shows the startup of the motor under different conditions.

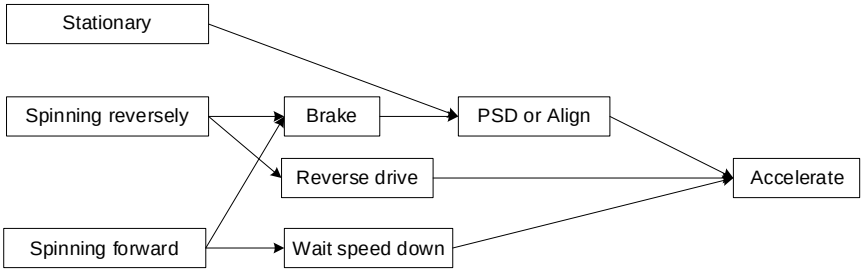


Figure 5. Startup of the Motor under Different Conditions

Closed Loop Control

In the closed loop operation, the BEMF information is essential to adjust the communication logic. In the sensorless control method, the device continually samples the motor current and periodically samples the bus voltage to estimate the BEMF.

Closed Loop Speed Control

The user can adjust the motor speed by VM or by controlling the speed command. The device supplies three approaches to control the speed command: the PWM input, the analog input or the I²C command.

Analog Mode Speed Control

The SP input pin can be set for analog input by configuring SpdCtrlMd to 0. If SP < V_{AZS}, the speed command is to stop the motor. If SP > V_{AFS}, the motor will run at the highest speed.

If V_{AZS} < SP <V_{AFS}, the speed command changes linearly according to the voltage on the SP pin.

And when the SP > V_{ASV}, the device start work, then the UVW PWM output will respond to the SP voltage.

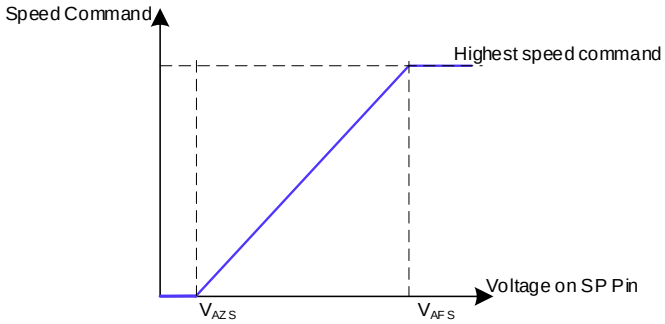


Figure 6. Analog Input and Speed Command

Digital PWM Input Mode Speed Control

When the SpdCtrlMd is configured to 1, the SP pin is set to a digital PWM input pin. The range of PWM duty cycle applied to the SP pin is 0 to 100%. The device can only recognize PWM of frequency F_{DSPF} to control the speed command. If the input signal keeps low for a certain time ($t_{EN\_SL\_SB}$), the speed command will be stopping the motor.

I²C Mode Speed Control

The speed can also be controlled through the I²C interface. When the OverRide bit is set to 1, the feature is enabled. The device will ignore the input of the SP pin if it is configured in I²C mode. The speed command of the I²C can be set from 0 to 255 by configuring the SpdCtrl[7:0].

Closed Loop Accelerate Limit

Sudden change of the speed command may cause noises and vibration of the motor. A maximum rate at which the speed commands changes is limited in this device. The value of the rate is decided by ClsLpAccel[2:0]. The input speed command and the speed command after rate limit are shown in Figure 7.

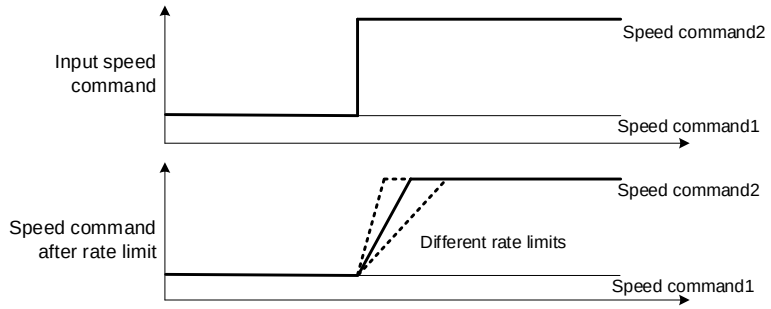


Figure 7. Rate Limit of the Speed Command

Closed Loop Angle Control of the Voltage

For a non-salient pole motor, the best efficiency will be achieved when the current and BEMF have the same phase position. The device adjusts the angle of the voltage every electrical cycle based on the zero crossing points of the BEMF and the sampled current. If the BEMF is leading the current, the voltage needs to be advanced with a corresponding angle in the next cycle. On the other hand, if the BEMF is lagging the current, the voltage needs to be delayed with a corresponding angle in the next cycle. Figure 8 shows the adjustment of the voltage angle with different phase position of the current and BEMF.

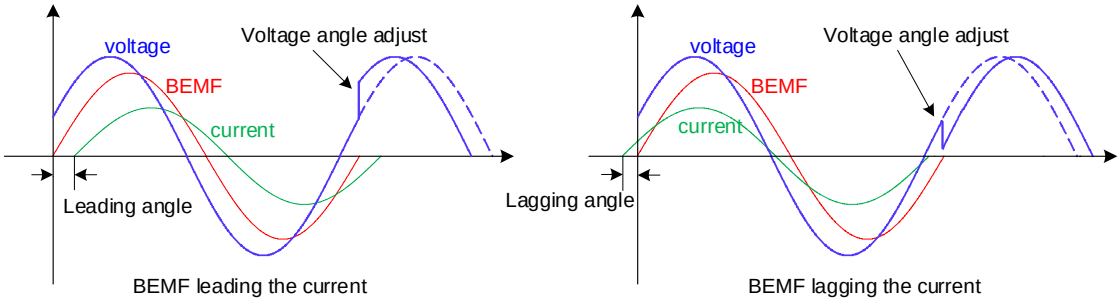


Figure 8. Adjust of the Voltage Angle

PWM Output Modulation

The SY67343 output PWM frequency is 20 kHz. The output voltage applied to the motor is a series of PWM signals modulated by a sine wave so that the output phase-to-phase voltage is sinusoidal. Figure 9 shows the sinusoidal modulating wave and the PWM output.

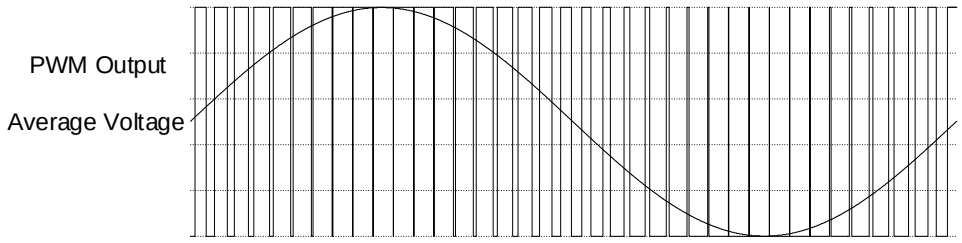


Figure 9. The Modulating Wave and the Output PWM

Motor Drive Direction Set

The motor drive direction is determined by the combination CW/CCW pin and the control register Direction. The logic of the drive direction is shown in Tab 1.

Tab 1. The Logic of Drive Direction

CW/CCW	Direction	Drive Direction
0	0	Forward (Drive Direction=1)
0	1	Reverse (Drive Direction=0)
1	0	Reverse (Drive Direction=0)
1	1	Forward (Drive Direction=1)

FG Output

The FG (frequency generator) output signal is a square wave based on the driving frequency. The default output signal toggles every electrical cycle. Many applications configure the pole pairs of the motor so that it provides two pulses for every mechanical rotation of the motor. The SY67343 device can accomplish this for 2-pole, 4- pole, 6-pole, and 8-pole motors up to 14-pole motors.

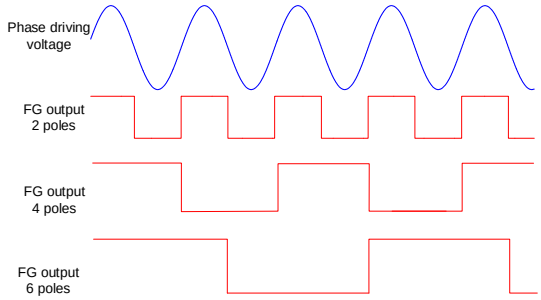


Figure 10. FG Output Signal

Step-Down Regulator

The SY67343 includes a step-down voltage regulator. The output voltage can be configured by register bit VregSel. When VregSel = 0, the output voltage is 5V, and when VregSel = 1, the output voltage is 3.3V.

The maximum peak current from Vreg can be selected by setting the BKIPSET[1:0], it can be used to power the external circuit such as a microcontroller.

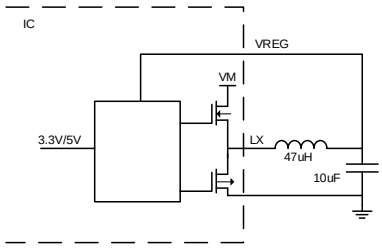


Figure 11. Buck Module

Abnormal State Detect

The device supplies several protection and abnormal state detect to ensure reliable operation of the motor. The abnormal rotor lock state is detected through different methods.

Lock Detect and Fault Handling

The device provides several different methods to detect whether the motor is locked by some external torque. Six different methods are used to make sure the detection is quick and reliable. If any of the lock conditions happens, the device will stop driving the motor and try to restart it after a certain time. The device also detects if there is a motor connected in addition to the lock detect. Figure 12 shows the detect logic of the device.

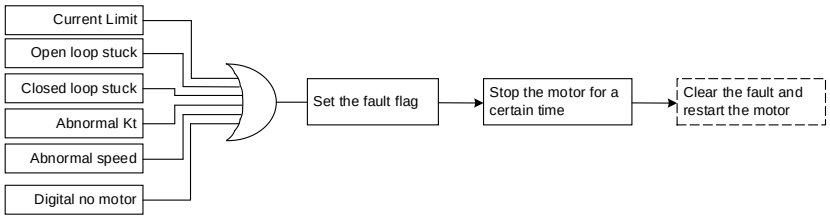


Figure 12. Lock Detect and Fault Handling

Current Limit

If a sudden lock happens when the motor is rotating, the current will be much big which could damage the system. The device provides a configurable current threshold which is set by CurrLimitThr[2:0] to detect the sudden lock. If the current is higher than the threshold, the device will stop the motor and a lock condition will be reported. The device will try to restart the motor after the time T_{LCKR}.

Open Loop Stuck

If the motor is successfully started up to the closed loop speed, the motor speed will be equal to the given closed loop speed. If the BEMF is not detected for one electrical period, the startup is failure and the device will stop the motor and report a lock condition. The device will try to restart the motor after T_{LCKR}.

Closed Loop Stuck

If a stuck happens when the motor operates in the closed loop state, the motor speed will suddenly become very low or even become 0. As the period of the BEMF is related to the motor speed, the zero crossing point of the BEMF will delay or even undetected. A closed loop stuck happens if the period of the BEMF is 1.5 longer than the previous period or the zero crossing point of the BEMF is not detected during that time.

Abnormal Kt

The integrated value of the BEMF in half of an electrical cycle is a constant regardless of the motor speed. The value is determined by the motor velocity Kt. The device calculates the velocity constant (Kt_est) and compares it with the Kt programmed by the user. If the Kt_est is smaller than 0.5×Kt or bigger than 2×Kt, a lock condition is reported.

Abnormal Speed

When the motor is normally running, the BEMF must be smaller than the amplitude of the output voltage. If the estimated BEMF is larger than the output voltage, the motor must get out of phase.

Digital No Motor

If the motor is not connected, no current will be detected. The device checks the U phase current through the ADC sample when the motor reaches the closed loop threshold, if the current is less than 40mA, the no motor fault is reported.

Diagnostics and Visibility

The motor information such as motor speed, lock information and others can also be monitored through the I²C serial interface.

Motor Status Read Back

The motor status register provides information on thermal shutdown (TSD), sleep state (Slp_Stdby), over current (OCP) and locked rotor (MtrLck).

Motor Electrical Speed Read Back

The motor electrical speed is calculated by the period of the zero-crossing point of the estimated BEMF. The value is automatically updated in register MotorSpeed. The electrical speed needs to be divided by the motor pole pairs to get the mechanical speed.

Motor Electrical Period Read Back

The motor electrical period is the time between two zero crossing points of the estimated BEMF. The value is automatically updated in register MotorPeriod.

Motor Velocity Read Back

The motor velocity is a constant for a certain motor. The motor velocity is automatically updated in register MotorKt.

Sleep or Standby Mode

The SY67343 also provide a sleep or standby mode. When the SY67343 enters Sleep Mode, three half-H-bridges gate drivers are disabled, the charge pump is stopped to conserve more energy, all internal logic and any register data not stored in MTP is reset, and all internal clocks are stopped.

Setting SleepDis=1 or sleep_stby=1 prevents the device to enter sleep condition. If the device has entered into sleep mode, setting SleepDis=1 or sleep_stby=1 will take it out of sleep mode.

For different speed command modes, bellow shows the condition to enter or exit from sleep mode.

Tab2. Enter/Exit Sleep Mode

Speed Command	Enter Sleep Mode	Exit from Sleep Mode
Analog	SP pin voltage < V_{AENSLP} for T_{ENSLP}	SP pin voltage > V_{AEXSLP} for T_{EXSLP}
PWM	SP pin voltage <V_{DEXSPL} for T_{ENSLP}	SP pin voltage >V_{DEXSPL} for T_{EXSLP}
I²C	SpdCtr[7:0] is set as 0 for T_{ENSLP}	SleepDis=1 or sleep_stby=1

Protections

The device is fully protected against overcurrent, undervoltage, thermal shutdown and mechanical voltage surge protection.

Overcurrent Protection (OCP)

An analog current limit circuit on each FET limits the current through the FET by limiting the gate drive. If this analog current limit persists for longer than the OCP deglitch time, all FETs in the three phase half-H-bridge will be disabled. The driver will be re-enabled after the OCP retry period (5s) has passed. If the fault condition is still present, the cycle repeats. If the fault is no longer present, normal operation resumes.

Over current conditions are detected independently on both high and low side devices; i.e., a short to ground, supply, or across the motor winding will all result in an overcurrent shutdown. If an analog current limit persists for longer than the OCP deglitch time, the SY67343 disables the output.

Undervoltage Lockout (UVLO)

If at any time the voltage on the VM pin falls below the undervoltage lockout threshold voltage, all circuitry in the device will be disabled, and all internal logic will be reset. Operation will resume when VM rises above the UVLO threshold.

Thermal Shutdown (TSD)

The device has thermal shutdown (TSD) to protect itself from over temperature. If the die temperature exceeds approximately 150°C, the device is disabled until the temperature drops to a safe level.

Any tendency of the device to enter thermal shutdown is an indication of either excessive power dissipation, insufficient heatsinking, or a too high ambient temperature.

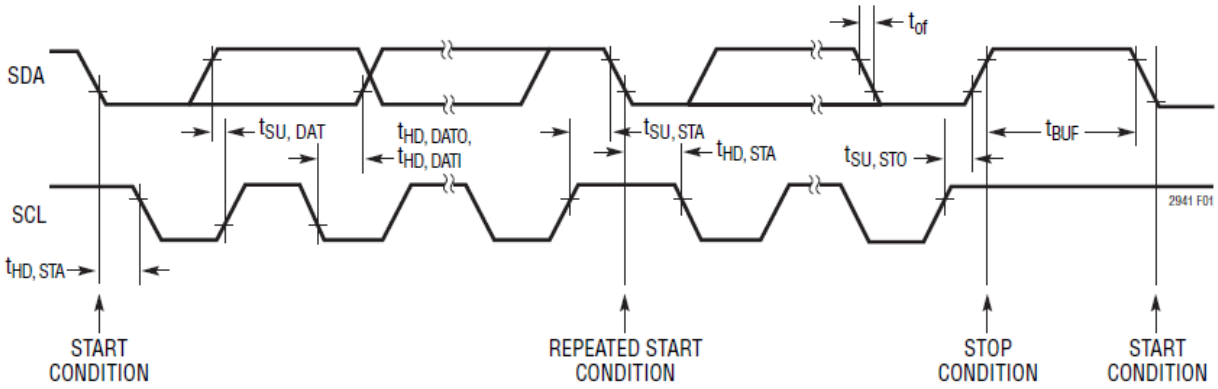
Mechanical Voltage Surge Protection

When the motor speed command suddenly drops or the drive signals turn from driving the motor state to a high impedance state, the mechanical energy stored in the rotor will return back to the power supply, which could lead to dc voltage surge and damage the system.

When the motor speed command suddenly drops, the BEMF generated by the motor is higher than the voltage applied to the motor. The energy returns to the power supply and the VM voltage surges. To avoid the energy returns back to the VM, there should be a minimal voltage supplied to the motor.

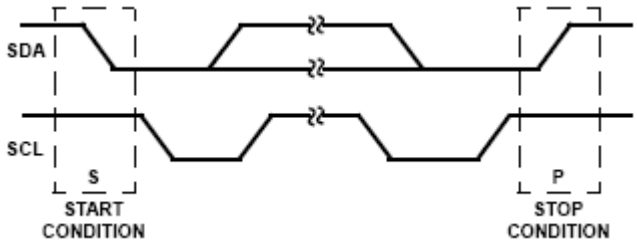
I²C Compatible Interface

The SY67343 features an I²C interface that allows the HOST processor to program or to control the motor. The I²C interface supports clock speeds of up to 400 kHz_and uses standard I²C commands. The SY67343 always operates as a slave device, and is addressed using a 7-bit slave address followed by an 8th bit, which indicates whether the transaction is a read-operation or a write-operation.



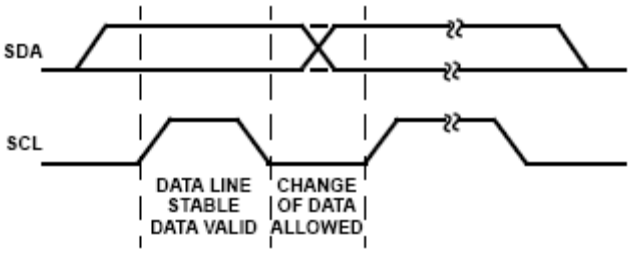
START and STOP Conditions:

The SY67343 is controlled via an I²C compatible interface. The START condition is a HIGH to LOW transition of the SDA line while SCL is HIGH. The STOP condition is a LOW to HIGH transition on the SDA line while SCL is HIGH. A STOP condition must be sent before each START condition. The I²C master always generates the START and STOP conditions.



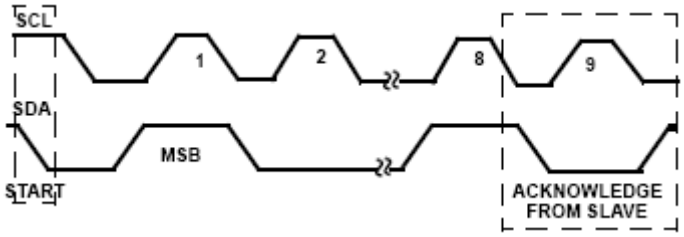
Data Validity:

The data on the SDA line must be stable during the HIGH period of the SCL, unless generating a START or STOP condition. The HIGH or LOW state of the data line can only change when the clock signal on the SCL line is LOW.



Acknowledge:

Each address and data transmission use 9-clock pulses. The ninth pulse is the acknowledge bit (ACK). After the START condition, the master sends 7-slave address bits and an R/$\overline{W}$ bit during the next 8-clock pulses. During the ninth clock pulse, the device that recognizes its own address holds the data line low to acknowledge. The acknowledge bit is also used by both the master and the slave to acknowledge receipt of register addresses and data.

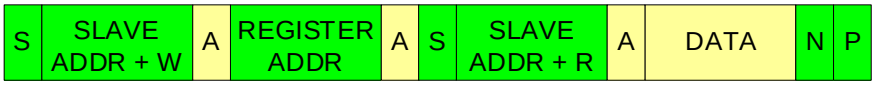


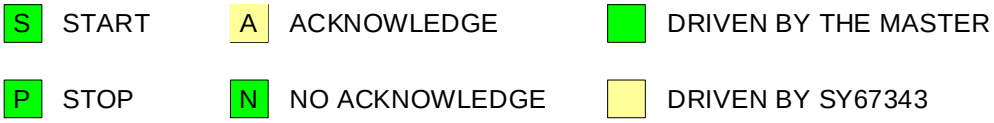
Data Transactions:

All transactions start with a control byte sent from the I²C master device. The control byte begins with a START condition, followed by 7-bits of slave address (0110100x) followed by the 8th bit, R/$\overline{W}$ bit. The R/$\overline{W}$ bit is 0 for a write or 1 for a read. If any slave devices on the I²C bus recognize their address, they will acknowledge by pulling the SDA line low for the last clock cycle in the control byte. If no slaves exist at that address or are not ready to communicate, the data line will be 1, indicating a Not Acknowledge condition. Once the control byte is sent, and the SY67343 acknowledges it, the 2nd byte sent by the master must be a register address byte. The register address byte tells the SY67343 which register the master will write or read. Once the SY67343 receives a register address byte it responds with an acknowledge signal.

Write To A Register

Read From A Register



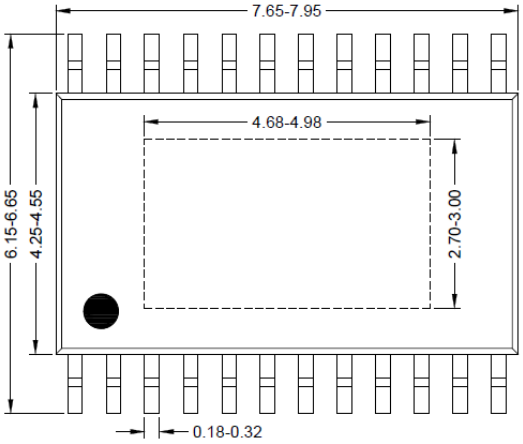


SY67343 Register Map

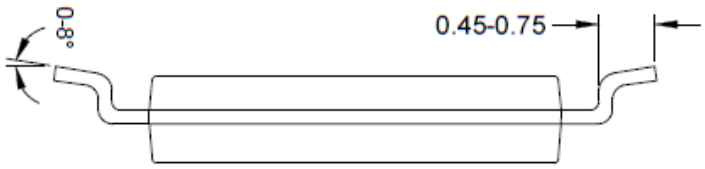
Register Name	Address	D7	D6	D5	D4	D3	D2	D1	D0
SpeedCtrl(1)	0x00	SpdCtrl[7:0]							
OverRide(1)	0x01	OverRide	Reserved						
DecCtrl(1)	0x02	enProgKey[7:0]							
EECtrl(1)	0x03	SleepDis	Sldata	eeRefresh	eeWrite	ParaInit	Reserved		
Status(2)	0x10	OCP	Slp_Stdby	TSD	MtrLck	UVLO	SHORT	BUCK	
MotorSpeed1(2)	0x11	MotorSpeed[15:8]							
MotorSpeed2(2)	0x12	MotorSpeed[7:0]							
MotorPeriod1(2)	0x13	MotorPeriod[15:8]							
MotorPeriod2(2)	0x14	MotorPeriod[7:0]							
MotorKt1(2)	0x15	MotorKt[15:8]							
MotorKt2(2)	0x16	MotorKt[7:0]							
SupplyVoltage(2)	0x17	SupplyVoltage[7:0]							
FaultCode(2)	0x18			Lock5	Lock4	Lock3	Lock2	Lock1	Lock0
MotorPara1	0x20	Rm[11:4]							
MotorPara2	0x21	Rm[3:0]				Lm[11:8]			
MotorPara3	0x22	Lm[7:0]							
MotorPara4	0x23	Kt[11:4]							
MotorPara5	0x24	Kt[3:0]				Direction	EnLdidt[2:0]		
SysOpt0(3)	0x25	SpdStartBrake[2:0]			SampleCnt[1:0]		SigFltTime0[2:0]		
SysOpt1(3)	0x26	ISDThr[2:0]			IPDAdvcAgl[1:0]		AVSMEn	RvsDrEn	AVSMMd
SysOpt2(3)	0x27			LockEn[5:0]					
SysOpt3(3)	0x28	OpenLCurr[2:0]			VMBias[1:0]		StAccel1[2:0]		
SysOpt4(3)	0x29	Op2ClsThr[4:0]					AlignTime[2:0]		
SysOpt5(3)	0x2A	IPDClk[1:0]		VolReverseSel[2:0]			ClsLpAccel[2:0]		
SysOpt6(3)	0x2B	IPDCurrThr[2:0]			SpdCtrlMd	VregSel	CurrLimitThr[2:0]		
SysOpt7(3)	0x2C	OpStuckThr[1:0]		SpdFlt[1:0]		SpdStartWait[3:0]			
SysOpt8(3)	0x2D	OpLCurrRt:[2:0]			StAccel2[2:0]			AccType	IPDCurrZero
SysOpt9(3)	0x2E					IPD_PWM[1:0]		IPD_SLEW[1:0]	
SysOpt10(3)	0x2F	FGCycle[2:0]			SpdupTime[1:0]		BuckPtcEn	BrkDoneThr [1:0]	
SysOpt11(3)	0x30	MaxPwmDuty[7:0]							
SysOpt12(3)	0x31	AngAdvCtrl[7:0]							
SysOpt13(3)	0x32	BKIPSET[1:0]		RestartTimeSel	Buck_Dis	CurrSamThr[1:0]		sleep_stby	sda_timeout_en

Note: (1) R/W;(2) Read Only;(3) MTP

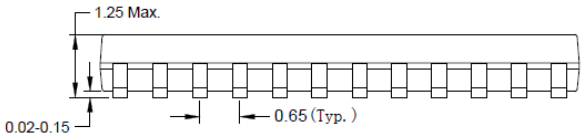
TSSOP24E Package Outline Drawing



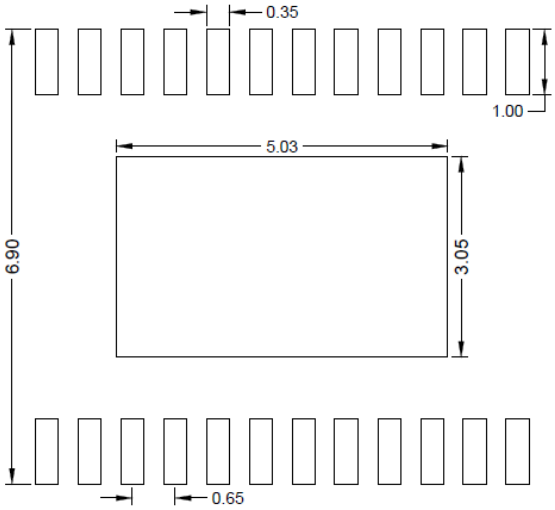
Top View



Side View



Front View

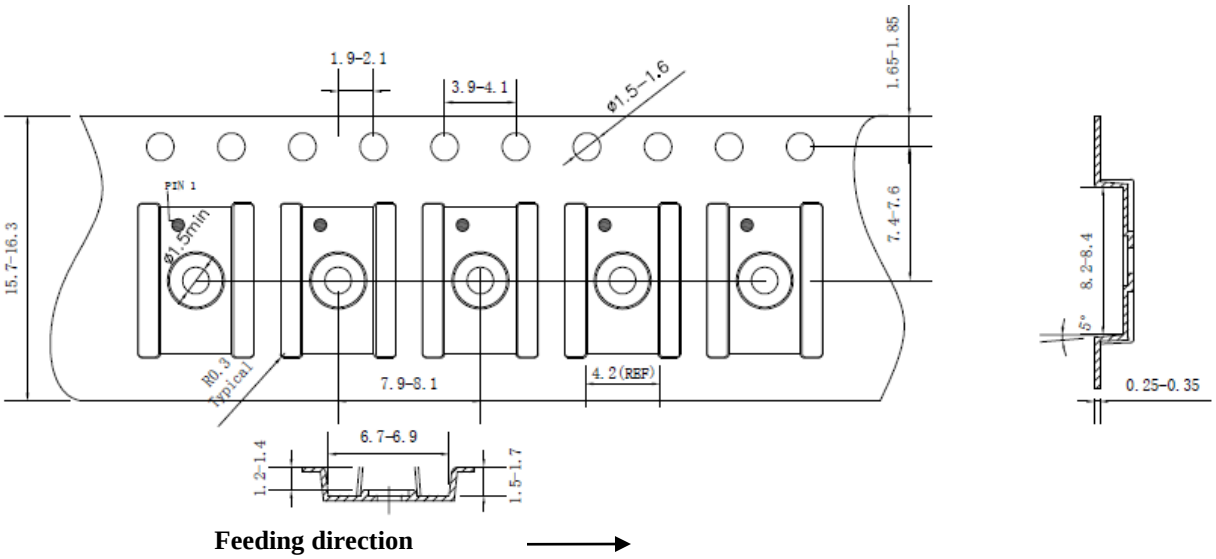


Recommended PCB Layout
(Reference only)

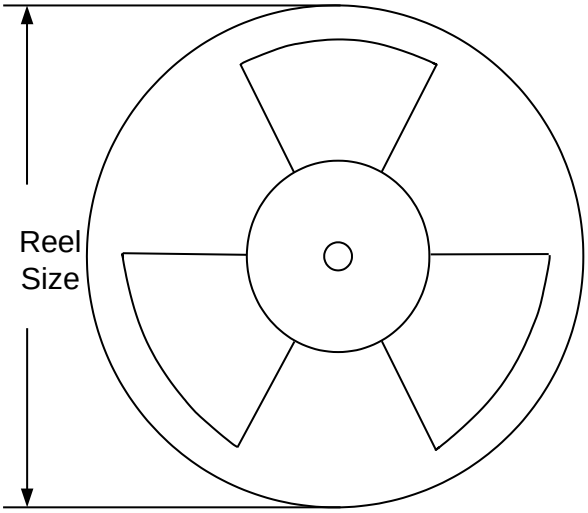
Notes: **All dimension in millimeter and exclude mold flash & metal burr.**

Taping & Reel Specification

1. Taping Orientation



2. Carrier Tape & Reel Specification for Packages



Package Types	Tape Width (mm)	Pocket Pitch(mm)	Reel Size (Inch)	Trailer Length(mm)	Leader Length (mm)	Qty per Reel
TSSOP24E	16	12	13"	400	400	3000

3. Others: NA

Revision History

The revision history provided is for informational purpose only and is believed to be accurate, however, not warranted. Please make sure that you have the latest revision.

Revision Number	Revision Date	Description
0.9	October 26, 2023	Initial Release
1.0	October 26, 2024	Production Release

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