SYT31S05DWD

Ultra-Low Capacitance TVS Protection

General Description

SYT31S05DWD is an ultra-low capacitance transient voltage suppressor (TVS) designed to provide electrostatic discharge (ESD) protection for high-speed data interfaces. With typical capacitance of 0.45pF only, SYT31S05DWD is designed to protect parasitic-sensitive systems against over-voltage and over-current transient events. It complies with IEC61000-4-2 (ESD) (±30kV air, ±30kV contact discharge), IEC61000-4-5 (Surge) (15A, 8/20μs), etc.

SYT31S05DWD can protect one high-speed data line. The combined features of ultra-low capacitance, ultra-small size and high ESD robustness make SYT31S05DWD ideal for high-speed data ports and high-frequency lines (e.g., USB3.x& DVI) applications. The low clamping voltage of the SYT31S05DWD guarantees a minimum stress on the protected IC.

Features

- Transient Protection for High-speed Data Lines
  - IEC61000-4-2(ESD) ±30kV (Air)±30kV (Contact)
  - IEC61000-4-5(Surge) 15A (8/20μs)
- For 5V and below Operating Voltage
- Ultra-small Package：DFN1.0×0.6-2
- Protects One High-speed Data Line
- Ultra Low Capacitance: 0.45pF（Typical）
- Low Clamping Voltage

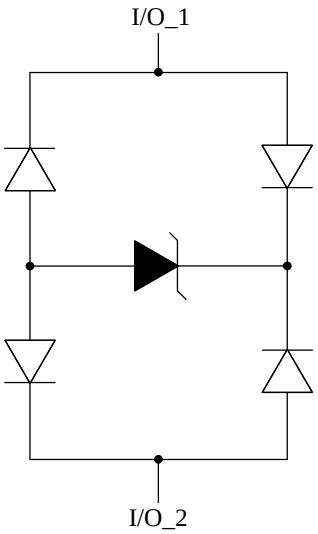
Applications

- Desktops, Servers and Notebooks
- USB3.x, USB Type-C
- USB2.0

Mechanical Characteristics

- DFN1.0×0.6-2 Package
- Marking: Device Code, Date Code.
- Packaging: Tape and Reel

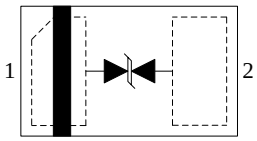
Circuit Diagram



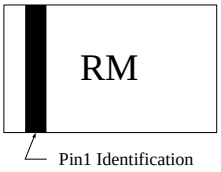
Ordering Information

Part Number	Package Type	Top Mark
SYT31S05DWD	DFN1.0*0.6-2	RM

Pinout (Top View)



Marking Codes



Note 1: "R" is device code, fixed.
Note 2: "M" is date code.

Pin Descriptions

Device Pins	Name	Description
1	Input/Output	IO1
2	Input/Output	IO2

Absolute Maximum Rating				
Parameter	**Symbol**	**Min**	**Max**	**Unit**
ESD per IEC 61000-4-2 (Air) ESD per IEC 61000-4-2 (Contact)	V_{ESD}	-30 -30	30 30	kV
Operating Temperature	T_{OPT}	-40	+125	℃
Storage Temperature	T_{STG}	-55	+150	℃

Electrical Characteristics (T_A = 25℃)						
Parameter	**Symbol**	**Test Condition**	**Min**	**Typ**	**Max**	**Unit**
Nominal Reverse Working Voltage	V_{RWM}		-5.0		5.0	V
Reverse Leakage Current @ V_{RWM}	I_R	V_{RWM} = 5V, T_A = 25°C		0.01	0.1	μA
Reverse Triggering Voltage @ I_{t1}	V_{tl}	I_{tl}= 1mA	5.5		10.5	V
Clamping Voltage @ I_{PP}	V_C[1]	I_{PP} = 16A, t_p = 10/100ns		6		V
Clamping Voltage @ I_{PP}	V_C[1]	I_{PP} = 15A, t_p = 8/20us		7.5		V
Dynamic Resistance	R_{DYN}[1,2]	t_p = 10/100ns		0.22		Ω
Parasitic Capacitance	C_{ESD}[1]	V_R = 1V, f = 1MHz		0.45	0.6	pF

Note 1: Guaranteed by design and not subject to production test.

Note 2: R_{DYN} calculated based on I_{PP}=8A to I_{PP}=16A, t_p = 10/100ns.

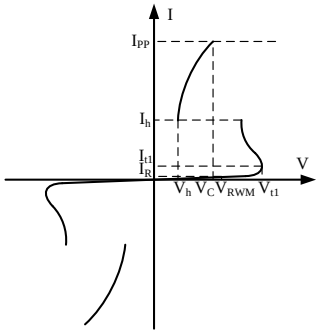
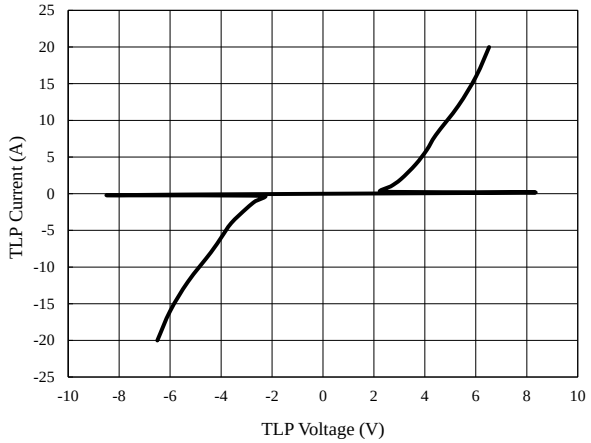


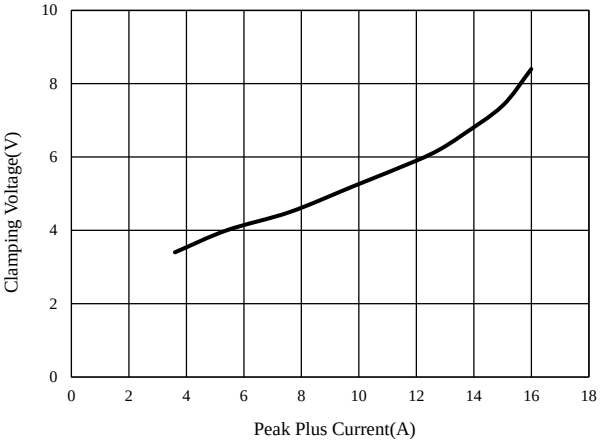
Figure 1. Bi-Directional TVS

Typical Characteristics

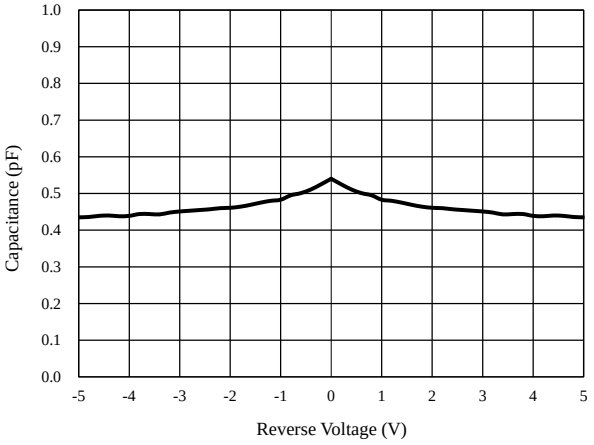
TLP Testing of I/O to I/O



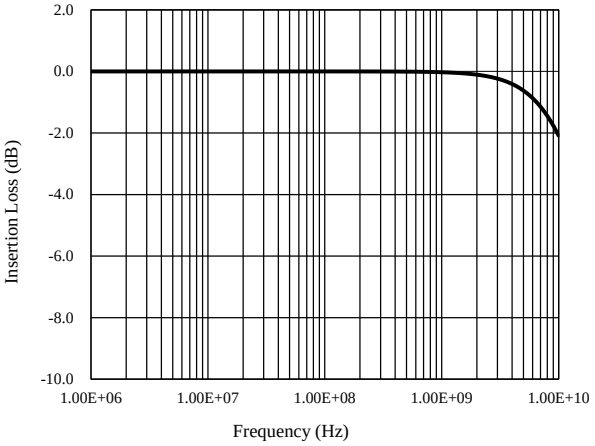
Clamping Voltage vs. Peak Pulse Current (8/20μs)



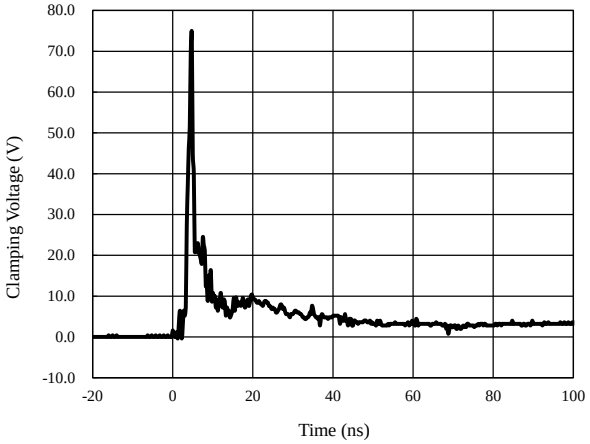
Capacitance vs. Voltage of I/O to I/O



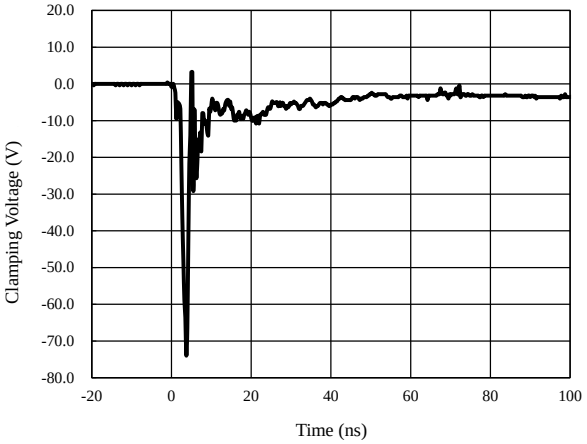
Insertion Loss S21 of I/O to I/O



ESD Clamping of I/O to I/O (+8kV Contact per IEC 61000-4-2)



ESD Clamping of I/O to I/O (-8kV Contact per IEC 61000-4-2)



Application Information

Pin Connection in PCB

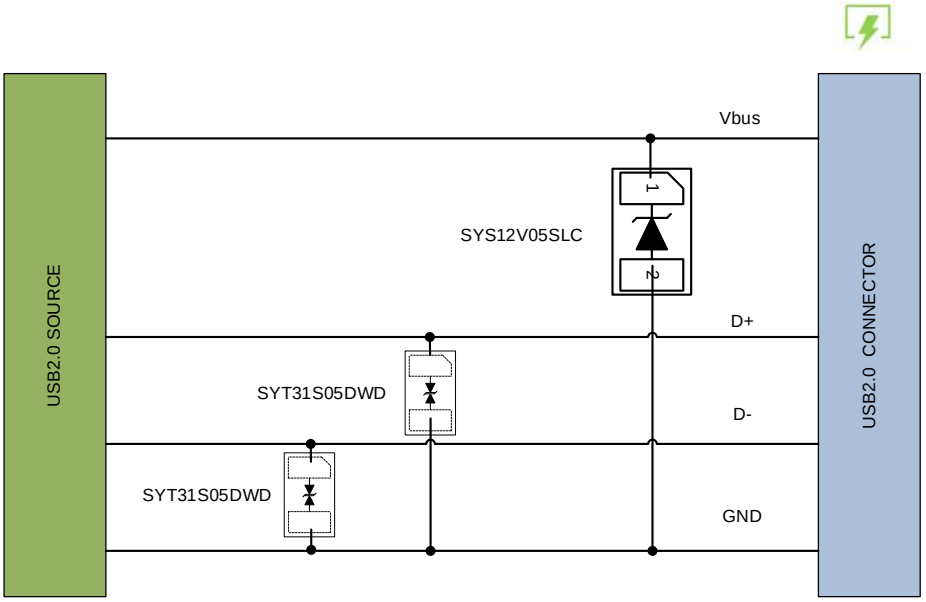


Figure 2. SYT31S05DWD Application for USB2.0

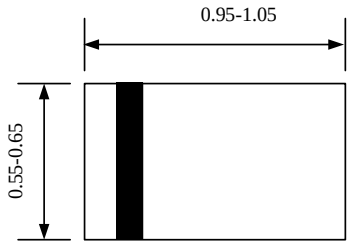
SYT31S05DWD provides ESD &surge protection for high speed lines (USB2.0, USB3.x.etc). Figure2 is the typical application for the USB2.0. A SYT31S05DWD can protect one high speed line, connect one pin to the high speed line, other pin to the ground. SYT31S05DWD has low clamping voltage 6V @ TLP current 16A, which provides a good ESD protection performance, besides SYT31S05DWD surge IPP is 15A, and surge clamping voltage only 7.5V, SYT31S05DWD can provide a higher than 30V surge protection level and good surge protection performance.

PCB Layout Guidelines

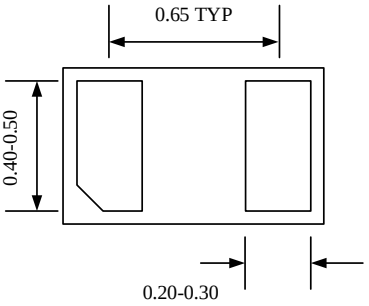
For optimum ESD protection and the whole circuit performance, the following PCB layout guidelines are recommended:

- SYT31S05DWD GND pin to the PCB GND rail path should be as short as possible. It could reduce the ESD transient return path to GND.
- The vias connecting SYT31S05DWD GND pins to the PCB GND should be wide.
- Place SYT31S05DWD as close to the connector port as possible. It could reduce the parasitic inductance and restrict ESD coupling into adjacent traces.
- Avoid running critical signals near board edges.

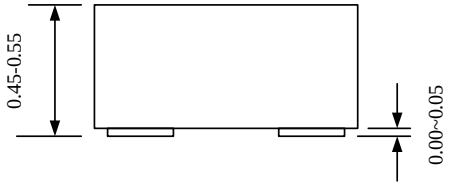
DFN1.0×0.6-2 Package Outline



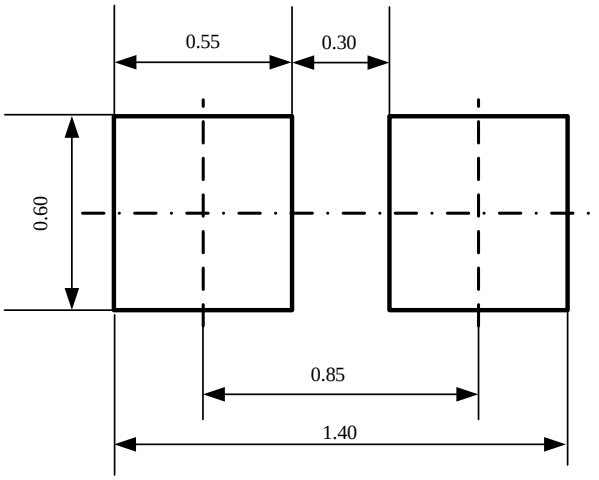
TOP VIEW



BOTTOM VIEW



SIDE VIEW

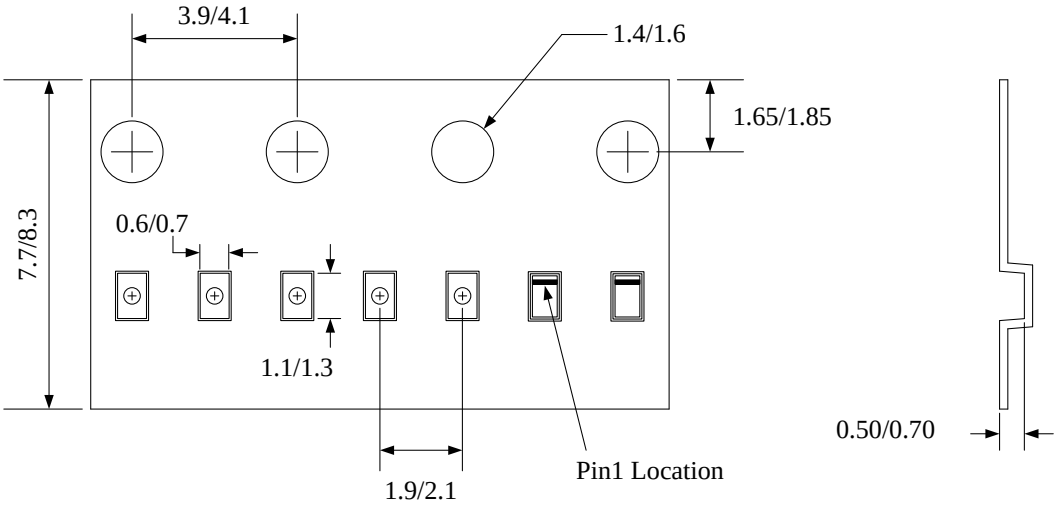


Recommended PCB Layout
(Reference only)

Note: All dimension in millimeter and exclude mold flash & metal burr.

Tape and Reel Specification

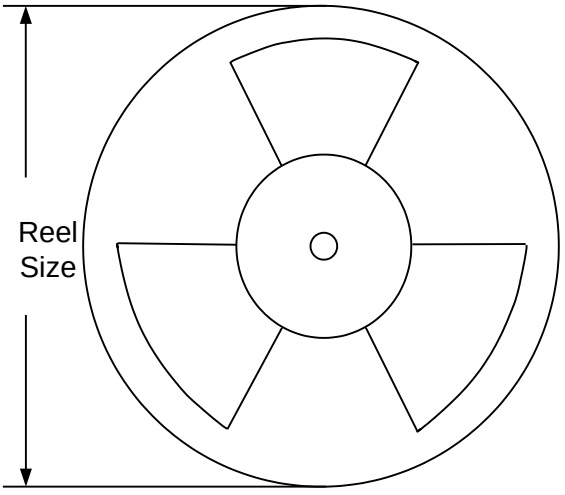
DFN1.0×0.6-2 Taping Orientation



Dimensions In mm

Feeding direction ⟶

Carrier Tape & Reel Specification for Packages



Package Types	Tape Width (mm)	Pocket Pitch(mm)	Reel Size (Inch)	Qty per Reel (pcs)
DFN1.0×0.6-2	8	2	7"	10000

Revision History

The revision history provided is for informational purpose only and is believed to be accurate, however, not warranted. Please make sure that you have the latest revision.

Revision Number	Revision Date	Description	Pages changed
0.9	Aug 29, 2023	Initial Release	
1.0	Aug 29, 2024	Production Release	
1.0A	Mar 11, 2025	Update Carrier Tape & Reel Specification for Packages	6

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