SQ33239

ZVS Flyback SR Controller

General Description

SQ33239 is a Flyback synchronous rectifier (SR) controller compatible with quasi-resonant (QR) mode converters, used to achieve zero voltage switching (ZVS) operation. The device is designed to complement primary side PWM converters operating in the QR mode.

Using a proprietary architecture, SQ33239 enables Flyback ZVS turn on, which can greatly improve the efficiency and increase the power density, while using adaptive gate voltage control to ensure system reliability.

SQ33239 uses DRAIN sense (DSEN) voltage falling slope rate detection to avoid SR MOSFET false turn on caused by parasitic ringing in discontinuous conduction mode (DCM) or QR mode.

The SQ33239 is available in a CPC8 package.

Features

- Proprietary Operation Mode for Flyback ZVS
- Adaptive Gate Voltage Control
- DSEN Falling Slope Rate Detecting to Prevent SR False Triggering
- 130V DSEN Pin to Directly Sense DRAIN Voltage of SR MOSET
- Power Saving Mode to Improve Light Load Efficiency
- Dual Power Supply Channel for 3.3V to 21V Output Systems
- Compact Package: CPC8

Applications

- Auxiliary Power Supplies
- AC/DC Adapters

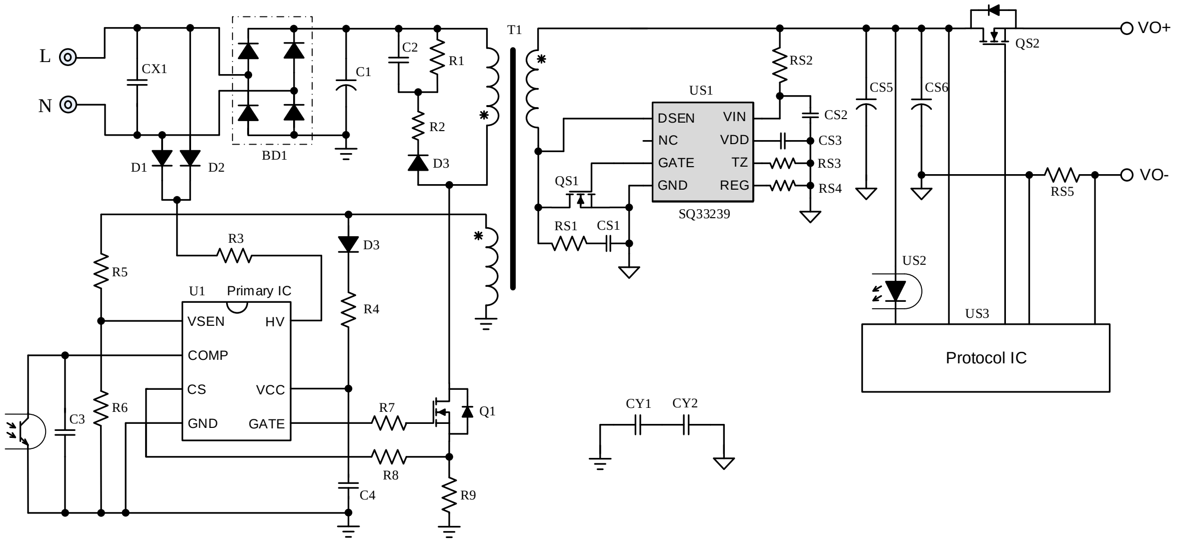


Fig. 1 Typical Application Circuit (SR MOSFET Location: Low Side)

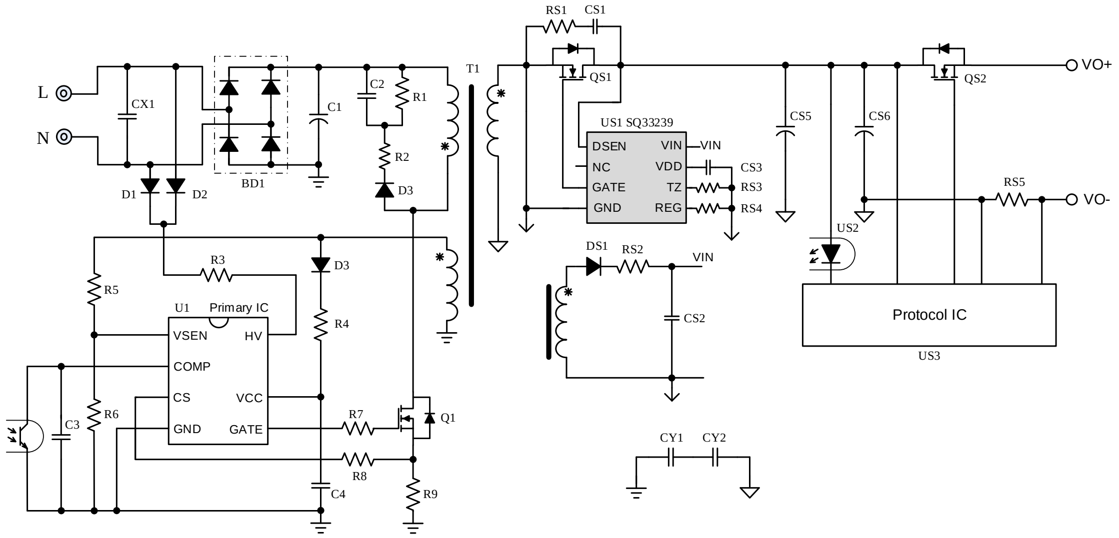


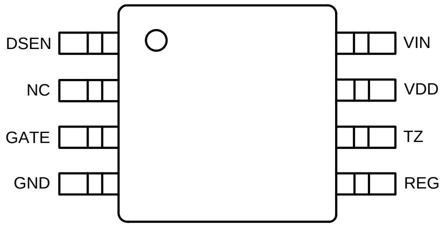
Fig. 2 Typical Application Circuit (SR MOSFET location: High Side)

Ordering Information

Ordering Part Number	Package type	Top Mark
SQ33239FPP	CPC8 RoHS-Compliant and Halogen-Free	**AACQ*xyz***

x = year code, y = week code, z = lot number code

Pinout (top view)



Pin Description

Pin No	Pin Name	Pin Description
1	DSEN	DRAIN sense input, also used as power supply source.
2	NC	Not connected.
3	GATE	External MOSFET gate drive pin.
4	GND	Ground pin.
5	REG	Connect a resistor between this pin and GND to set the falling slope reference time threshold.
6	TZ	Connect a resistor to program the ZVS coefficient.
7	VDD	Output of internal LDO, power supply for control logic and gate drive circuitry. Connect a 0.47μF or larger ceramic capacitor between VDD and GND pins.
8	VIN	Input of low voltage power supply.

Block Diagram

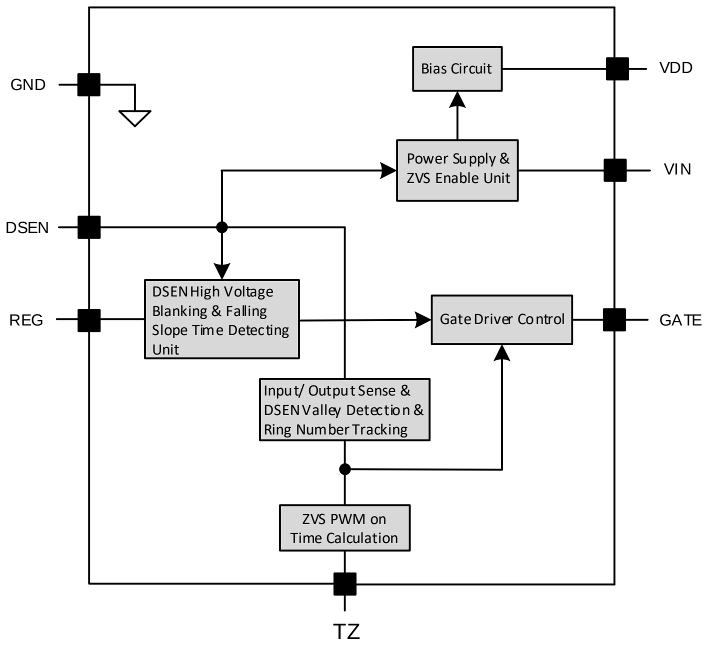


Fig.3 Block Diagram

Absolute Maximum Ratings

Parameter (Note 1)	Min	Max	Unit
DSEN	-1	130	V
VIN	-0.3	30	
VDD	-0.3	15	
GATE	-0.3	VDD+0.3V	
TZ, REG	-0.3	4	
Junction Temperature, Operating	-45	150	°C
Lead Temperature (Soldering, 10 sec.)		260	
Storage Temperature Range	-65	150	

Thermal Information

Parameter (Note 2)	Min	Max	Unit
θ_{JA} Junction-to-ambient Thermal Resistance		145	°C/W
θ_{JC} Junction-to-case Thermal Resistance		47	
P_D Power Dissipation T_A = 25°C		0.9	W

Recommended Operating Conditions

Parameter (Note 3)	Min	Max	Unit
VIN	3.3	21	V
VDD	3	10	
Junction Temperature	-40	125	°C
Ambient Temperature	-40	85	

Electrical Characteristics

(V_{VDD}=9V, T_J=-40 to 125℃, unless otherwise specified (Note 4))

Parameter		Symbol	Test Conditions	Min	Typ	Max	Unit
VDD Pin	VDD ON Threshold	V_{VDD_ON}		3	3.35	3.7	V
	UVLO Hysteresis	V_{VDD_HYS}		100	200	300	mV
	VDD Regulation Voltage when VIN Pin is Active to Supply IC	$V_{VDD\_REG\_VIN}$		8.4	9.4	10.2	V
	VDD Regulation Voltage when DSEN Pin is Active to Supply IC	$V_{VDD\_REG\_DSEN}$		4.5	5.1	5.6	V
	Operating Current (Note5)	I_{VDD_OP}	V_{DD}=9V, C_{GATE}=2.2nF, F_{SW}=200kHz		5.35	6.4	mA
			V_{DD}=5V, C_{GATE}=2.2nF, F_{SW}=200kHz		3.5	4.2	mA
	Maximum VDD Pin Capacitor Charging Current	$I_{VDD\_CHARGE\_MAX}$	VIN pin is active to charge VDD capacitor	16	35		mA
			DSEN pin is active to charge VDD capacitor	30	50		mA
	Quiescent Current	I_Q	Under Sleep Mode		350	455	µA
VIN Pin	Threshold of Switching to VIN Supply Channel	V_{VIN_VINSPY}	V_{VIN} is rising	4.3	4.7	4.95	V
	Threshold of Switching to DSEN Supply Channel	$V_{VIN\_DSENSPY}$	V_{VIN} is falling	4.2	4.6	4.85	V
REG Pin	Resistor to Program DRAIN Falling Slope to Enable SR(Note5)	t_{REF}	R_{REG}=50kΩ		80		ns
			R_{REG}=300kΩ		155		ns
TZ Pin	ZVS Time Program Coefficient(Note5)	k_{TZ}			4.5		10^{-9}
DSEN Pin	Ratio of PVS to DSEN(Note5)	$K_{\_PVS\_RATIO}$			50		
	PVS Initial Enable Threshold(Note5)	$V_{PVS\_INITIAL\_EN}$			150		mV
	Turn on Threshold	V_{ON_TH}		-125	-90	-55	mV
	V_{DS} Regulation Voltage	V_{DS_REG}		-53	-35	-18	mV
	Turn off Threshold	V_{OFF_TH}		6	20	33	mV
	Force Turn off Threshold	$V_{DS\_FORCE\_TH}$		34	48	65	mV
	Force Turn off Debounce Time (Note5)	t_{DBC_FORCE}		50	71	92	ns
	Enter Sleep Mode Time Threshold	t_{SLP_TH}		51	67	87	µs
GATE Pin	GATE Pin Clamped Current before VDD ON(Note5)	I_{CLP}	Vgs=1V		200		mA
	Max. Source Current (Note5)	I_{SOURCE_MAX}	C_{LOAD}=2.2nF, Vgs from 1V to 6V		0.5		A

Parameter		Symbol	Test Conditions	Min	Typ	Max	Unit
GATE Pin	Max. Sink Current (Note5)	I_{SINK_MAX}	C_{LOAD}=2.2nF, Vgs from 6V to 1V		2		A
	Minimum ON Time	t_{ON_MIN}		540	700	860	ns
	Minimum OFF Time	t_{OFF_MIN}		400	520	640	ns
	Turn on Delay Time (Note5)	t_{ON_DLY}	C_{GATE}=2.2nF		35	50	ns
	Turn off Delay Time (Note5)	t_{OFF_DLY}	C_{GATE}=2.2nF		10	20	ns
OTP	Thermal Shutdown Temperature (Note5)	T_{SD}			165		°C
	Hysteresis to Resume Operating (Note5)	T_{OTP_HYS}			20		°C

Note 1: Stresses beyond the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

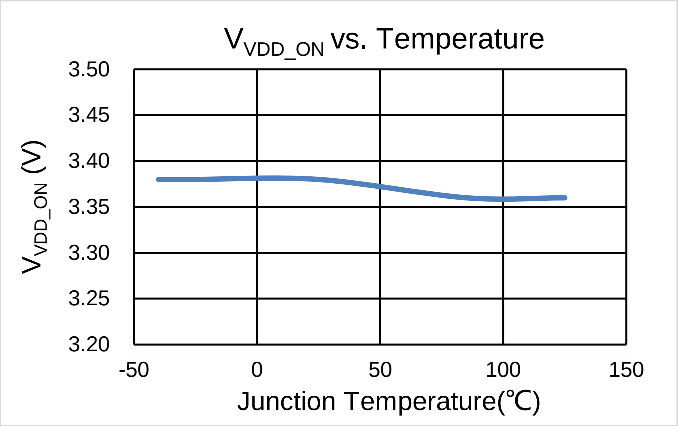
Note 2: θ_{JA} is measured in the natural convection at T_A = 25°C on a 2oz two-layer Silergy evaluation board. Case temperature θ_{JC} is measured at pin 4. [Use the actual condition provided by package engineering.]

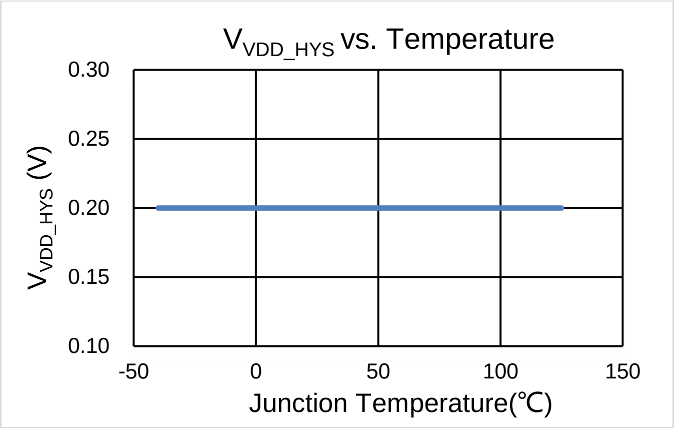
Note 3: The device is not guaranteed to function outside its operating conditions.

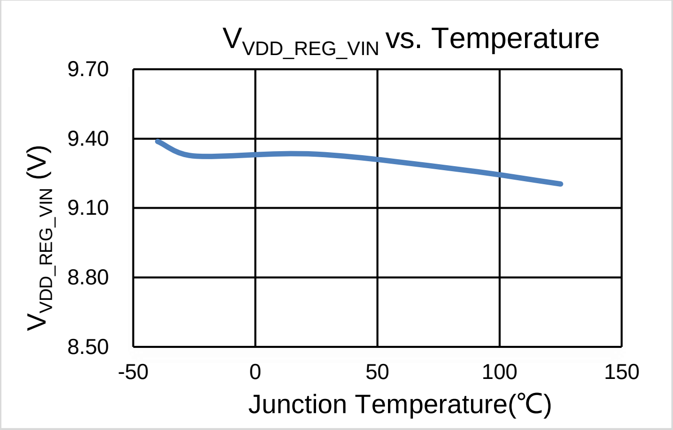
Note 4: Unless otherwise stated, limits are 100% production tested under pulsed load conditions such that $T_A \approx T_J = 25°C$. Limits over the operating temperature range (See recommended operating conditions) and relevant voltage range(s) are guaranteed by design, test, or statistical correlation.

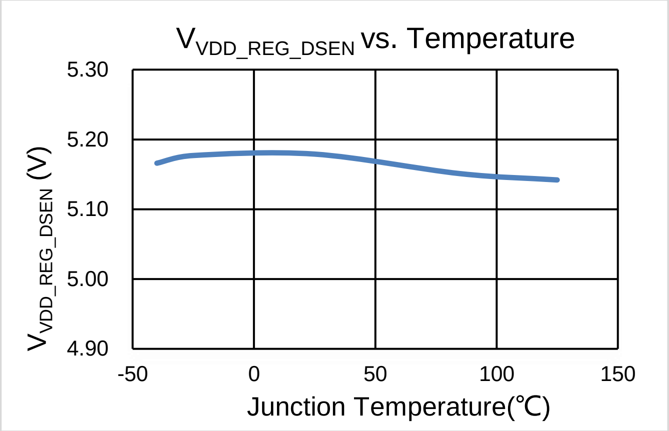
Note 5: Guaranteed by design or statistical correlation and not production tested. [Note 5 may be omitted if all EC parameters are tested in production.]

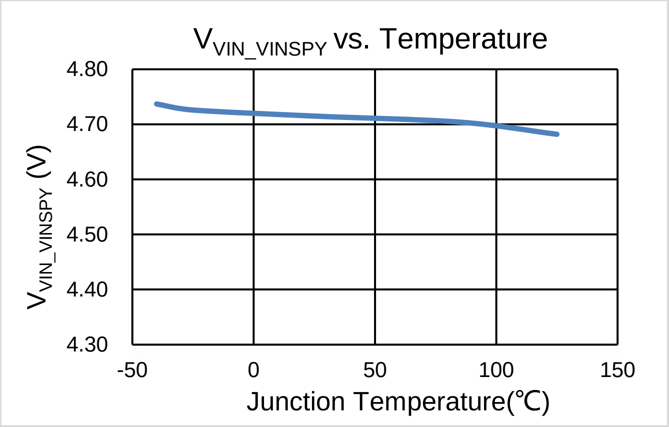
Typical Characteristics

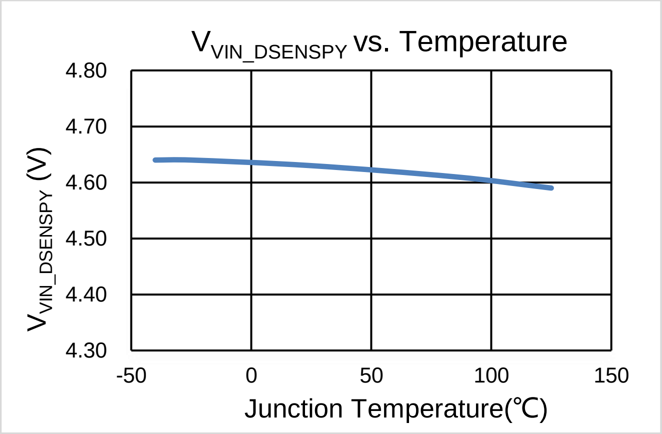


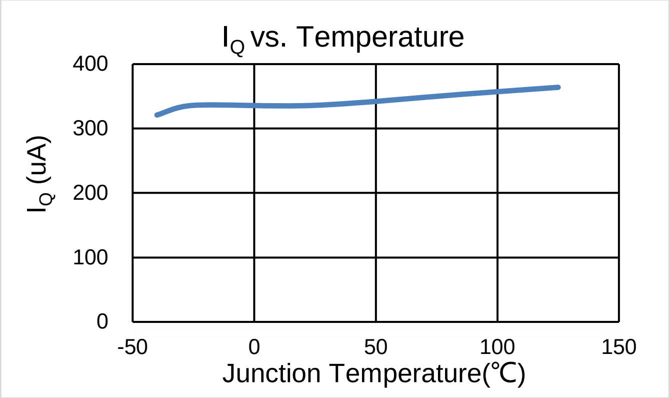


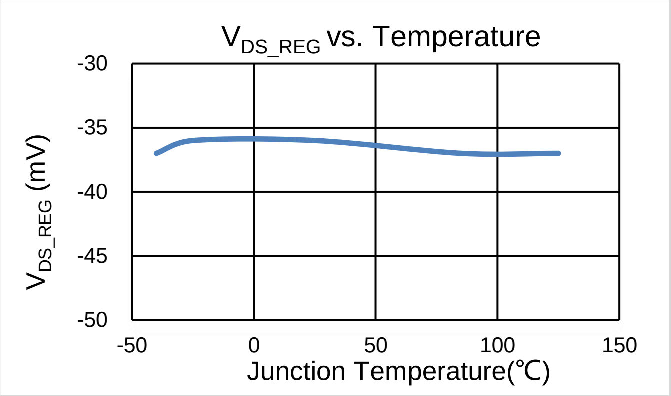


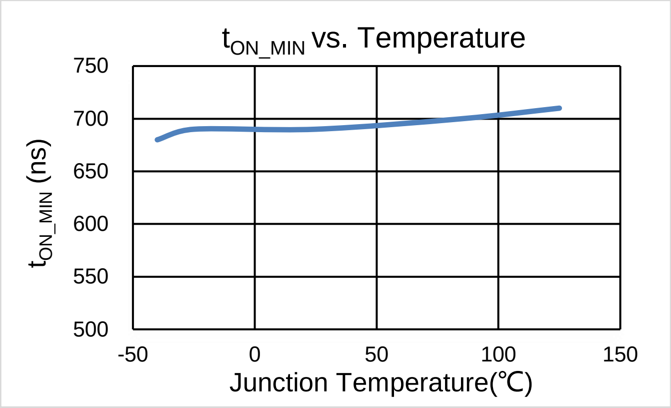


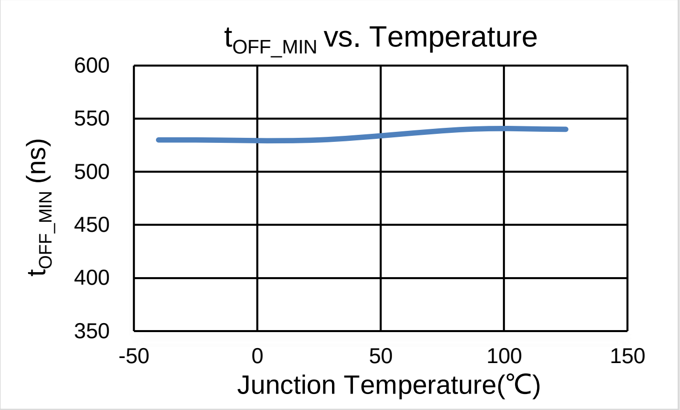





I_Q vs. Temperature
I_Q (uA)
400
300
200
100
0
-50
0
50
100
150
Junction Temperature(℃)


V_{DS_REG} vs. Temperature
V_{DS_REG} (mV)
-30
-35
-40
-45
-50
-50
0
50
100
150
Junction Temperature(℃)


t_{ON_MIN} vs. Temperature
t_{ON_MIN} (ns)
750
700
650
600
550
500
-50
0
50
100
150
Junction Temperature(℃)


t_{OFF_MIN} vs. Temperature
t_{OFF_MIN} (ns)
600
550
500
450
400
350
-50
0
50
100
150
Junction Temperature(℃)

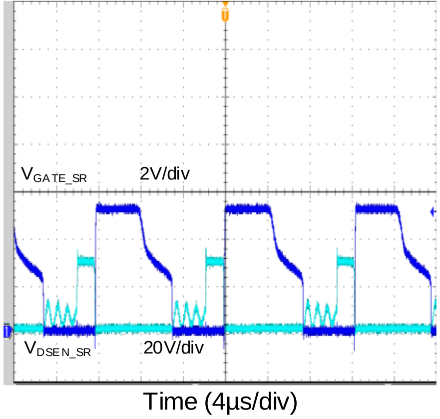
Typical Performance Characteristics

(Test condition: input voltage: 90Vac~264Vac; output spec: 5Vdc_3A, 20Vdc_3.25A; Ambient temperature: 25±5 ℃; Ambient humidity: 65±25 %.)

5Vdc_3A Output

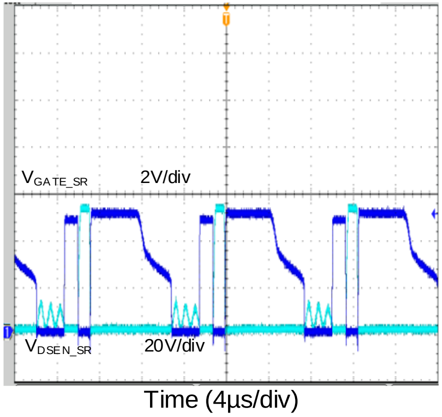
Steady States

(V_{IN}=115$V_{(AC)}$, full load)



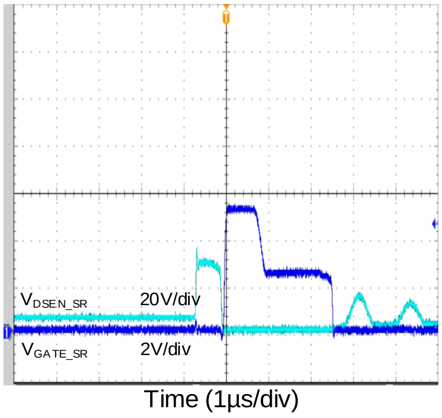
Steady States

(V_{IN}=230$V_{(AC)}$, full load)



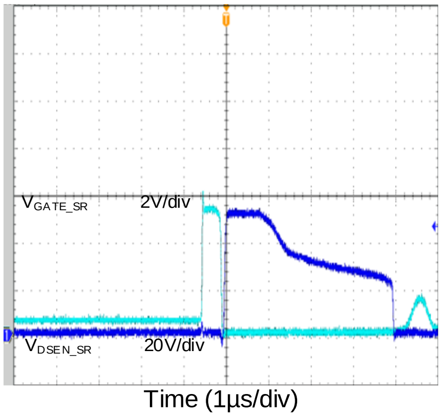
Steady States

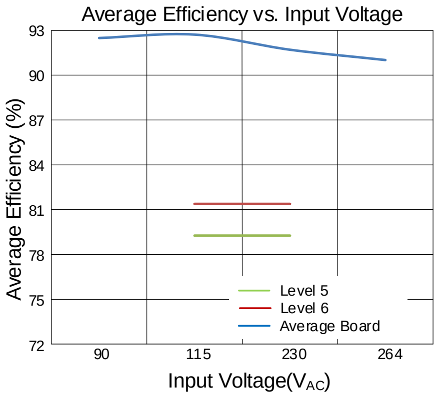
(V_{IN}=115$V_{(AC)}$, no load)



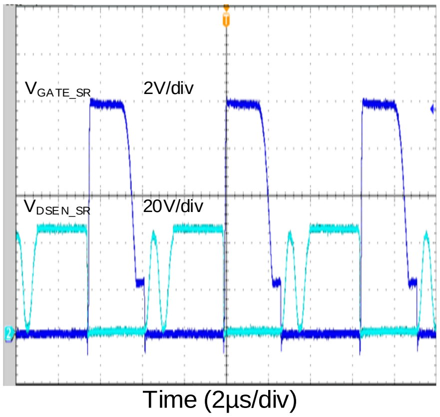
Steady States

(V_{IN}=230$V_{(AC)}$, no load)



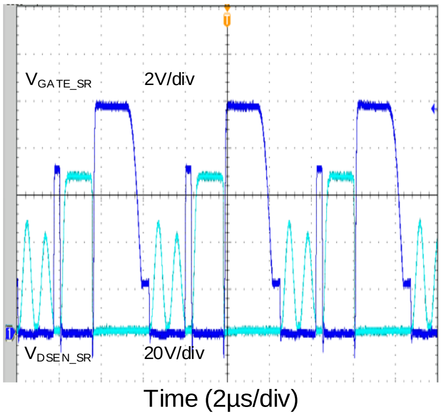


20Vdc_3.25A Output



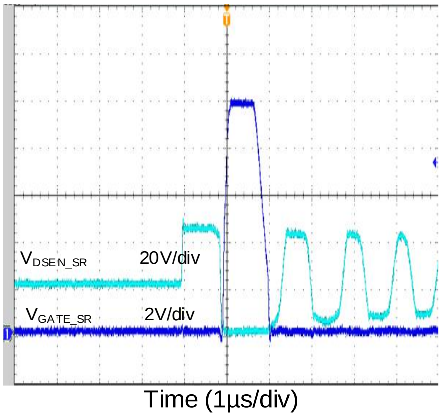
Steady States

(V_{IN}=115$V_{(AC)}$, full load)



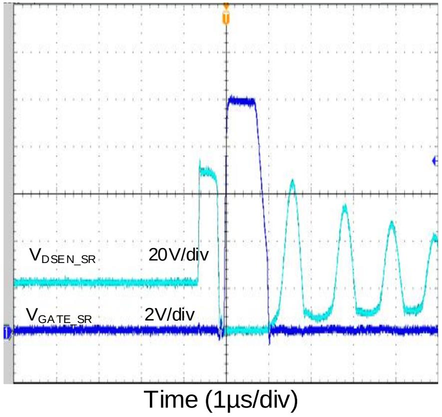
Steady States

(V_{IN}=230$V_{(AC)}$, full load)



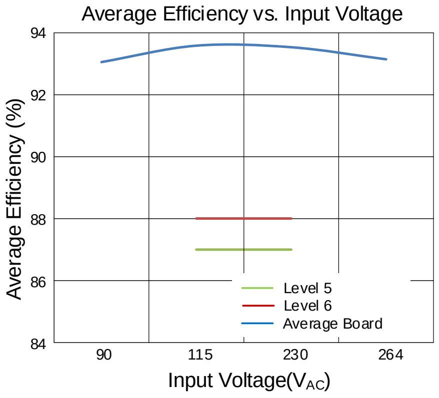
Steady States

(V_{IN}=115$V_{(AC)}$, no load)



Steady States

(V_{IN}=230$V_{(AC)}$, no load)



Detailed Description

Introduction

The SQ33239 is a Flyback SR controller compatible with QR mode converters for ZVS operation. The device is designed to complement primary side PWM converters operating in QR mode and valley lock mode, where the valley lock number is between 1 and 6.

Using a proprietary architecture, the SQ33239 supports Flyback ZVS turn on, which can greatly improve the solution efficiency and increase power density, while using adaptive gate voltage control to ensure system reliability.

The SQ33239 can achieve ZVS function by SR MOSFET turned on twice in a switching cycle. After the secondary side continuous current is completed, ZVS PWM is turned on at the last ring valley, generating negative current to achieve the primary side ZVS.

To ensure safe operation, SR control functions include turn on/off control, V_{DS} regulation and slope programming. The ZVS function helps the primary side MOSFET to turn on at a low DRAIN voltage to reduce the switching losses, thereby increasing system efficiency and power density.

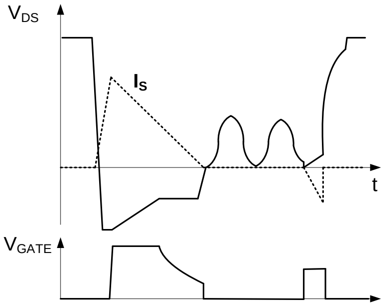


Fig. 4 SR Operation Diagram

SR Turn on

The traditional method of turning on the SR MOSFET is to use a set turn-on threshold V_{ON_TH}.

When the monitored DSEN voltage falls and reaches V_{ON_TH}, the SR MOSFET is turned on after a short delay.

While in DCM or QR operating modes, a resonant waveform may appear after the transformer secondary current decreases to zero. Sometimes, the amplitude of this resonant waveform can be large enough to cause the DSEN voltage to drop below the turn on threshold V_{ON_TH}, which may lead to the false turn on of the SR MOSFET. To address this issue, a circuit to detect the falling slope rate of V_{DSEN} is used.

When the primary MOSFET Q1 is turned off, the V_{DSEN} falling slope rate is very high, and the SR MOSFET will turn on. During the resonant phase, the V_{DSEN} falling slope rate is relatively low, and the SR MOSFET will not turn on.

The SQ33239 uses a resistor divider circuit (V_{PVS}) to sense the DSEN voltage, where V_{PVS} is 0.02 x V_{DSEN}.

Two thresholds are used to sense the V_{PVS} falling slope rate. $\triangle t$ is the time duration measured when V_{PVS} is falling between the high-level threshold V_{PVS_HTH} and the low-level threshold V_{DSEN_LTH} (0mV). $\triangle t$ is compared with a falling slope reference time t_{REF} using a counter.

A blanking period is used to prevent external noise (such as ESD noise) from falsely turning on the SR MOSFET.

If V_{PVS} is above V_{PVS_HTH}, lasts for t_{PVS_BLK} (200ns) and the falling slope time $\triangle t < t_{REF}$, the device considers this as a primary MOSFET turn off event, and will turn on the SR MOSFET after a short delay. In all other cases the SR MOSFET will not be turned on.

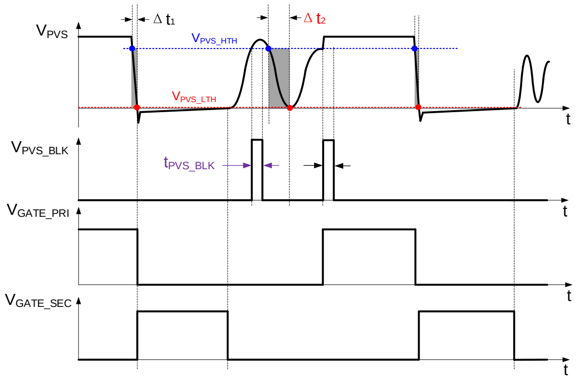


Fig. 5 SR MOSFET Turn on Time Diagram

V_{PVS_HTH} is a dynamically adjusted value, and it has a value of 0.85 x V_{DSEN}.

The falling slope ref time threshold t_{REF} is controlled by the REG resistor as shown below:

t_{REF} setting has 4 steps:		
Step	t_{REF}	R_{REG}
1	80ns	50kΩ
2	105ns	100kΩ
3	130ns	175kΩ
4	155ns	300kΩ

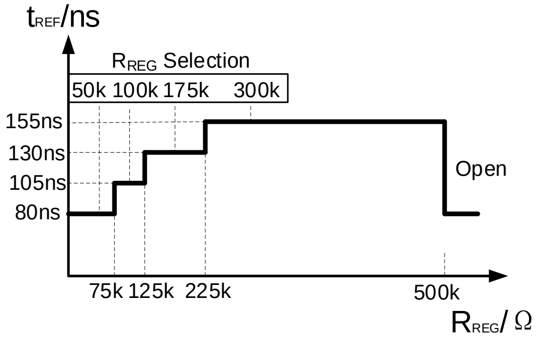


Fig. 6 t_{REF} Programming

SR Gate Control

In DCM mode, the current through the SR MOSFET will decrease before the primary MOSFET is turned on. The closed-loop V_{DS} regulation circuit will gradually reduce V_{GATE} once V_{DS} is above the V_{DS_REG} (-35mV) level. As the current through the SR MOSFET decreases, V_{GATE} drops close to the turn off threshold of the SR MOSFET. At this point, the product of the (I_D x R_{DSON}) can no longer be regulated to V_{DS_REG}, causing V_{DS} to increase beyond V_{OFF_TH}. After a short time delay (t_{OFF_DLY}), a large sink current will pull down the gate voltage to zero to turn OFF the SR MOSFET.

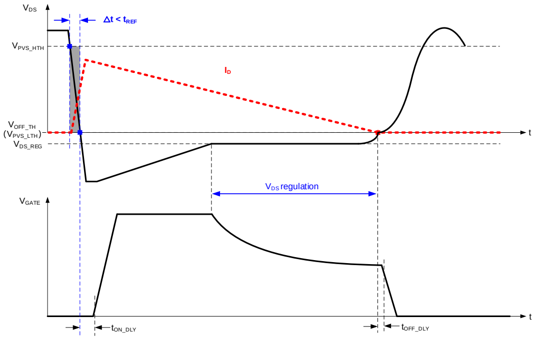


Fig. 7 SR MOSFET Control in DCM Mode

Dual Channel Power Supply

The device optimizes the overall efficiency by using two possible power sources during normal operation.

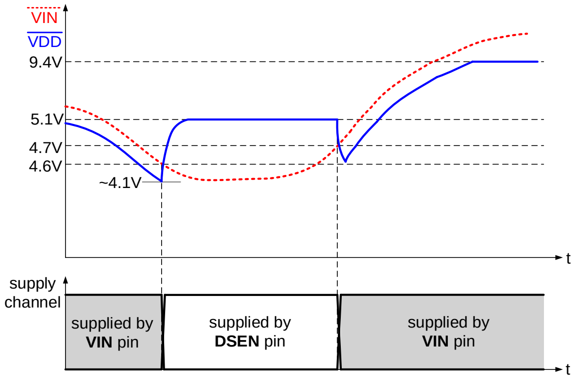


Fig. 8 Timing Diagram of Dual Channel Supply

Before VDD voltage reaches the V_{VDD_ON} threshold, the voltage is supplied by DSEN pin. When the voltage exceeds the V_{VIN_VINSPY} threshold, the VIN pin will be used instead.

As VIN increases, VDD will follow VIN (with about 0.5V voltage drop). When the voltage goes above 9.4V, the rail is regulated internally to this value.

When VIN is decreasing and crossing $V_{VIN\_DSENSPY}$, the device will switch to using the DSEN pin, and VDD will be regulated to 5.1V. The timing diagram is shown in Fig. 8.

Min ON Time & Min OFF Time

When the primary MOSFET is turned off, the DRAIN voltage of the secondary SR MOSFET will drop rapidly to about -700mV, due to the circuit parasitic resonance. To avoid false turn-off of the SR MOSFET, a blanking time t_{ON_MIN} is applied after the SR MOSFET is turned ON. During this blanking time, the GATE pin output is latched off.

After SR MOSFET is turned OFF, a ringing will appear on DRAIN voltage waveform. To avoid the internal logic circuit false trigger, a blanking time t_{OFF_MIN} used.

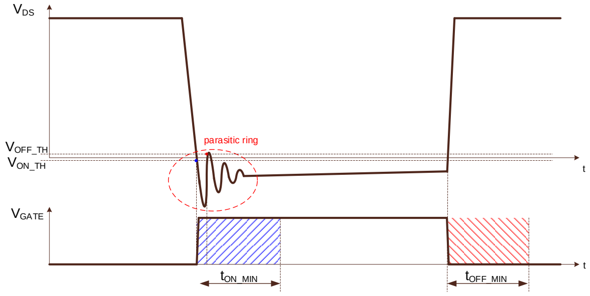


Fig. 9 Timing Diagram of Min ON/OFF Time

ZVS Operation

The key function of the SQ33239 is to achieve primary MOSFET ZVS turn on for high efficiency and high power density. The SQ33239 is compatible with primary side QR mode which has valley number lock operation mode to achieve this function.

The SQ33239 adopts a proprietary drive method to increase the resonant magnitude of switching node, which pulls primary DRAIN voltage (V_{DRAIN_PRI}) to approximately 50V to achieve primary side MOSFET ZVS conduction. The ZVS PWM is only activated in QR mode within 1~6 valleys. Beyond this range, ZVS is disabled.

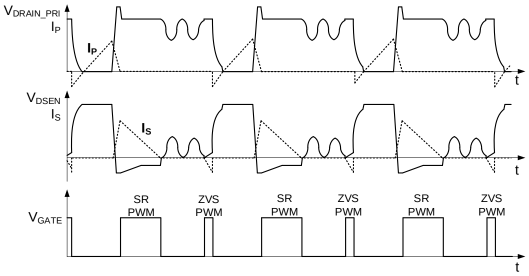


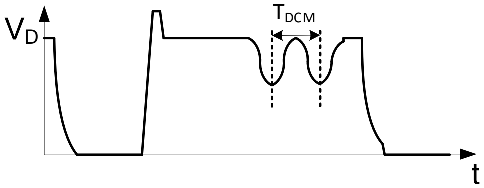
Fig. 10 ZVS Control Diagram

ZVS Coefficient TZ Resistor Setting

The ZVS performance is affected by transformer's magnetizing inductance (L_M) and the total equivalent capacitance (C_{SW}) of the switching node. For best efficiency, the resistor value connected between TZ and GND pins can be adjusted.

Method 1: Calculate the coefficient based on magnetizing inductance and equivalent switching node capacitance. The resistor sets ZVS PWM turn on time. The value can be calculated using the following equation:

$$R_{TZ}=\frac{\sqrt{C_{SW}\cdot L_M}}{4.5\cdot 10^{-9}}(k\Omega)$$



T_{DCM}: DCM resonance period time

Method 2: Calculate the coefficient based on DCM resonance time period.

$$R_{TZ}=\frac{T_{DCM}}{2\cdot\pi}\cdot\frac{1}{4.5\cdot 10^{-9}}(k\Omega)$$

The R_{TZ} should be adjusted slightly around the calculated value. The R_{TZ} value between 20kΩ and 80kΩ is recommended. ZVS is disabled for values <10kΩ or >100kΩ.

ZVS Enable

1. Power supply: when the VIN supply is active, ZVS will be enabled. When the DSEN supply is active, the ZVS will be disabled (the supply power loss is much higher when DSEN pin is used and the driving loss may be greater than ZVS effect).

2. Input voltage (V_{BULK}) condition: at low line input voltage, the efficiency is not significantly improved by using ZVS. To optimize operation, the input voltage range is limited to maximize ZVS effect. The input voltage range calculation is shown below, and it includes hysteresis for stable operation:

$$\text{ZVS enable: } V_{BULK}>N\cdot(0.333\cdot V_{OUT}+24)$$

$$\text{ZVS disable: } V_{BULK}<N\cdot(0.333\cdot V_{OUT}+21)$$

ZVS Protection

To guarantee operation of the ZVS function, the ZVS maximum on time is limited to 3us.

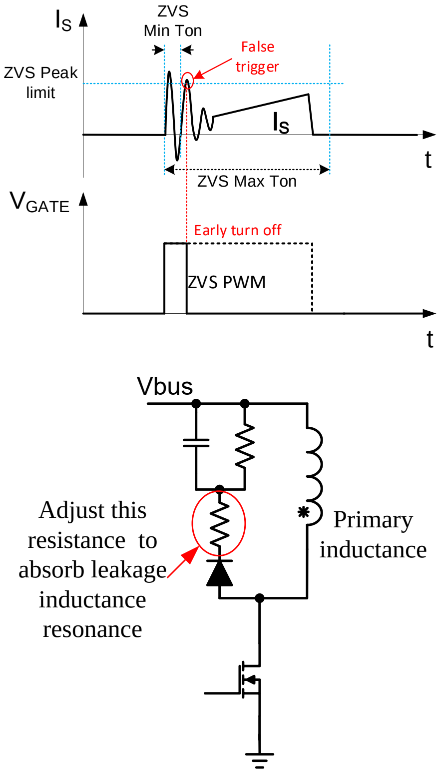


Fig. 11 ZVS Limit Protection

To prevent excessive ZVS current or primary side false turn on, the secondary current is limited during ZVS conduction. However, the primary leakage inductance resonance may false trigger the ZVS peak limit and cause the ZVS PWM early turned off. To avoid this situation, it is recommended to add a primary inductance resonance absorption resistor.

Power Saving Mode

Under light load conditions, the SQ33239 will enter power saving mode to improve light load efficiency.

During the switching cycle, a timer will start to count after SR MOSFET is turned off. If the timer counts to 67us before next SR turn on, the device will enter power saving mode to reduce the overall power consumption. The SQ33239 exits power saving mode on the next SR MOSFET turn on time.

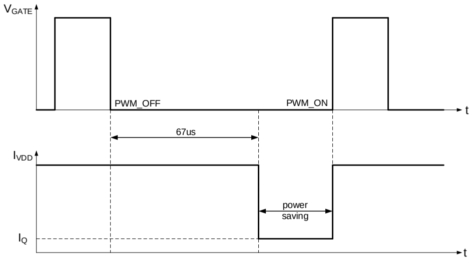


Fig. 12 Power Saving Mode Timing Diagram

Forced Turn off

To prevent the primary MOSFET and secondary MOSFET from turning on at the same time, the device uses a forced turn-off function, which has higher priority than t_{ON_MIN}. When the V_{DS} is above DSEN forced turn-off threshold $V_{DS\_FORCE\_TH}$, and lasting for debounce time t_{DBC_FORCE}, SR GATE will turn off immediately; When V_{DS} is below $V_{DS\_FORCE\_TH}$, SR GATE drive can be restored within t_{ON_MIN}.

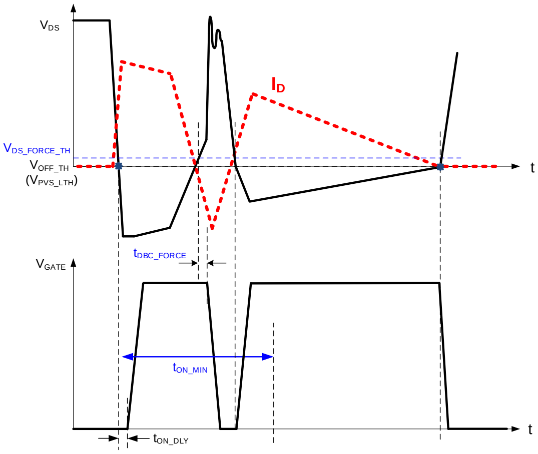


Fig.13 Timing Diagram of Forced Turn off

OTP

The internal die temperature is continuously monitored. If the die temperature rises above 165℃, the device stops switching the SR MOSFET and keep gate voltage to 0V. When the die temperature drops below 145℃, it resumes normal operation.

Typical Application Schematic

Typical application circuit information is displayed in a 65W PD Flyback design. The PD charger circuit includes synchronous rectifier controller (SQ33239).

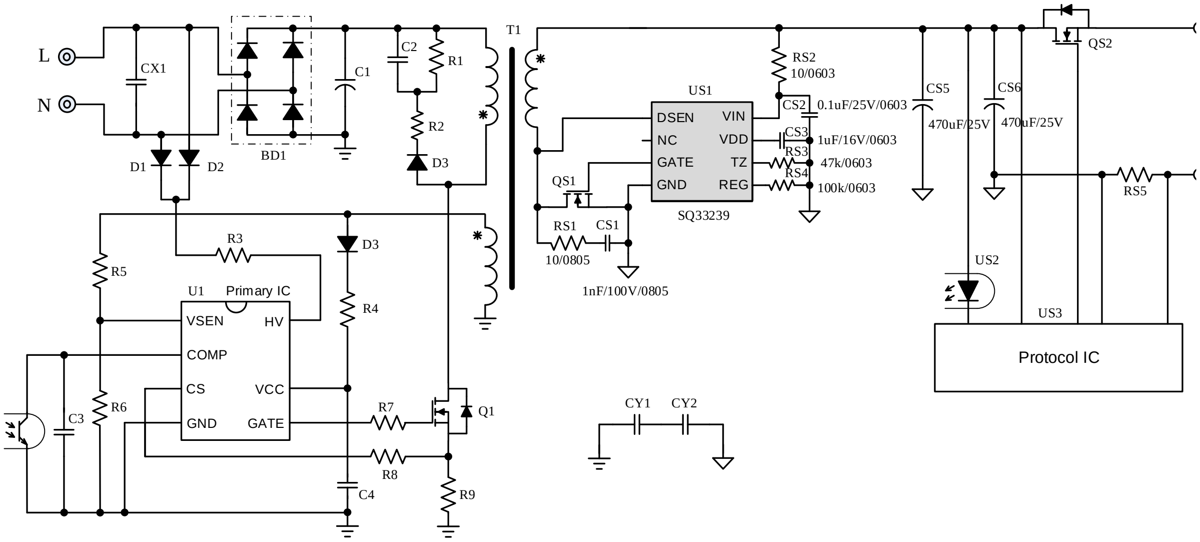


Fig. 14 65W PD Typical Application Circuit

Recommended BOM List

Designator	Description	Part Number	Manufacturer
RS1	10Ω/0805	0805W8F100JT5E	UNI-ROYAL
RS2	10Ω/0603	0603WAF100JT5E	UNI-ROYAL
RS3	47kΩ/0603	0603WAF4702T5E	UNI-ROYAL
RS4	100kΩ/0603	0603WAF1003T5E	UNI-ROYAL
CS1	1nF/100V/X7R, 0805	CC0805KRX7R0BB102	YAGEO
CS2	0.1uF/25V/X7R, 0603	CC0603KRX7R8BB104	YAGEO
CS3	1uF/16V/X7R, 0603	CC0603KRX7R0BB105	YAGEO
CS5, CS6	470uF/25V/Solid Cap	SPZ1EM471E14O00RAXXX	AISHI
US1	SQ33239/CPC8	SQ33239	Silergy

Design Procedure

SR MOSFET Selection

The MOSFET selection is based on optimizing the R_{DSON} versus gate charge losses.

Below a certain level, the R_{DSON} of the MOSFET doesn't directly reduce the conduction loss, because SQ33239 uses a loop that regulates the voltage drop in the forward direction to around 35mV across the drain-source terminals.

For optimal performance consider a minimum of 30% SR MSOFET conduction period at maximum load for optimal performance.

For example, for a 65W converter, the peak current of the SR MOSFET should be about 14A for 3.25A load current. To achieve a control time corresponding to 30% duty cycle, the R_{DSON} should be selected using the formula:

$$R_{DSON} \ge \frac{V_{DS\_REG}}{I_{PEAK\_SR} \times 0.3} = \frac{35mV}{4.2A} \approx 8.33m\Omega$$

For the MOSFET voltage rating, the maximum V_{DS} should be lower than breakdown derated voltage. For example, for the 65W converter example, the transformer turn ratio is 6.5 and the derating coefficient $K_{Derating}$ is 0.9.

The breakdown voltage of the MOSFET should be higher than the value calculated using the formula below:

$$V_{DS(BR)} \ge \frac{V_{DS\_MAX}}{K_{Derating}} = \frac{\frac{V_{BULK}}{N_{PS}} + \Delta V_{OUT}}{K_{Derating}} = \frac{\frac{373}{6.5}V + 20V}{0.9} = 86V$$

A 100V/8mΩ MOSFET is recommended for the above requirements.

Other considerations for selecting the right MOSFET are: overall efficiency, thermal performance and cost.

RC Snubber Selection

The RC snubber components RS1 and CS1 are used to damp the switching ringing caused by stray inductance (L_{Stray}) and equivalent capacitance (C_{EQ}) in the secondary switching loop.

The L_{Stray} can be tested using a LCR meter. The C_{EQ} can be calculated considering the switching ringing period, based on the formula:

$$C_{EQ} = \frac{T_r^2}{(2\pi)^2 \times L_{Stray}} = \frac{50ns^2}{(6.28)^2 * 100nH} = 634pF$$

Considering the Q of the circuit equal to 1, the snubber resistor RS1 can be calculated using the formula:

$$R_{RS1} = \frac{1}{Q}\sqrt{\frac{L_{stray}}{C_{EQ}}} = \sqrt{\frac{100nH}{634pF}} = 12.56\Omega$$

A value of 10Ω can be selected in this case.

CS1 will influence the spike of V_{DS} and thermal performance. The recommended value for CS1 is 1nF/100V.

External Components Selection

When used in low-side configuration, the SQ33239 uses two power inputs. VIN pin is one of the supply channels, and a reservoir capacitor, CS2, has to be connected close to this pin.

The recommended value and voltage rating for CS2 are:

0.1 µF/25V.

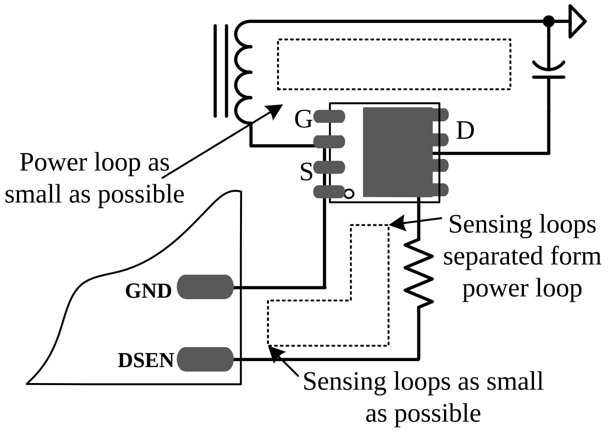
The recommended value for RS2 is 10Ω.

The recommended value and voltage rating for CS3 in most applications are:

1uF/16V.

Layout Guidelines

1. The sensing connection (DSEN/GND) should be made as close as possible to the MOSFET (drain/source).
2. Minimize the interference between the sensing and power loops as shown below:



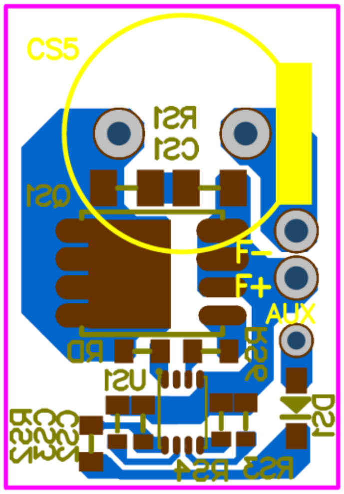
(a) Minimize the size of the switching loops: secondary power loop, secondary RC snubber circuit loop and IC power supply loop.

(b) To achieve better EMI and Efficiency performance, use a decoupling capacitor between the output connector and the SR MOSFET output.

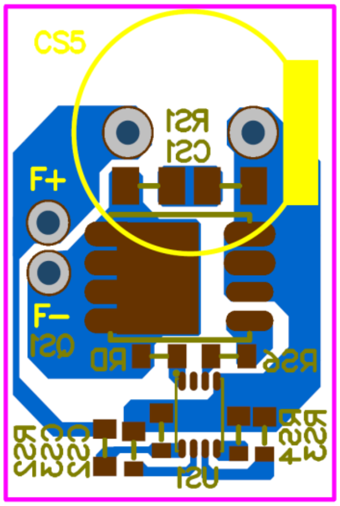
(c) GND pin should be connected to the Source of the SR MOSFET using a short trace.

(d) DSEN pin should be connected to the Drain of the SR MOSFET using a short connection.

(e) Due to the high resistance on REG and TZ pin, the layout size and length of each loop should be as small as possible. The layer directly under these two loops should be connected to the device GND to shield switching noise.



High Side SR Layout @Bottom View

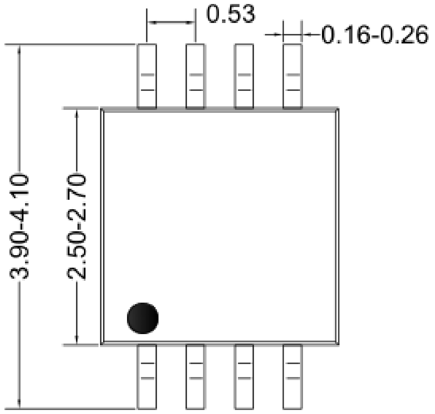


Low Side SR Layout @Bottom View

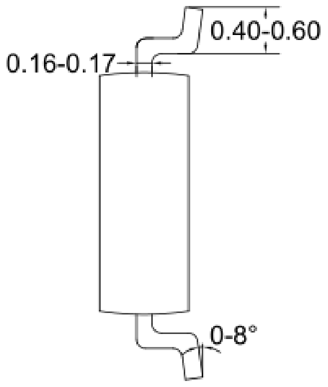
Design Notes:

1. To improve system ESD performance, a 10Ω~51Ω resistor should be used in series between VIN pin and output terminal, and at least 100nF cap should be used in parallel between VIN and GND pins.
2. To achieve optimal ZVS, select a SR MOSFET with low inductance packages like PDFN5*6 or SO-8 for the SR MOSFET, to avoid ZVS early turned off.
3. To achieve optimal ZVS, select a SR MOSFET with low Ciss and Coss capacitance. Ciss is recommended not exceed 6nF.

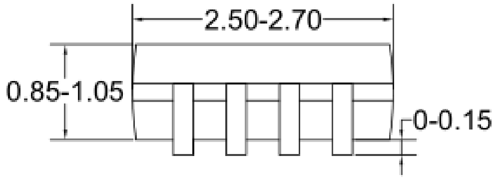
CPC8 Package Outline & PCB Layout Design



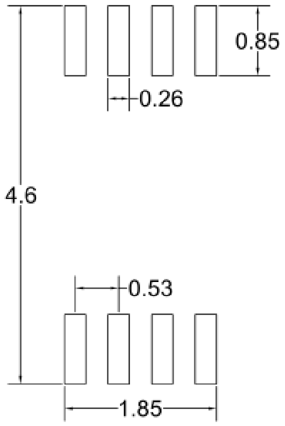
Top view



Side view



Front view

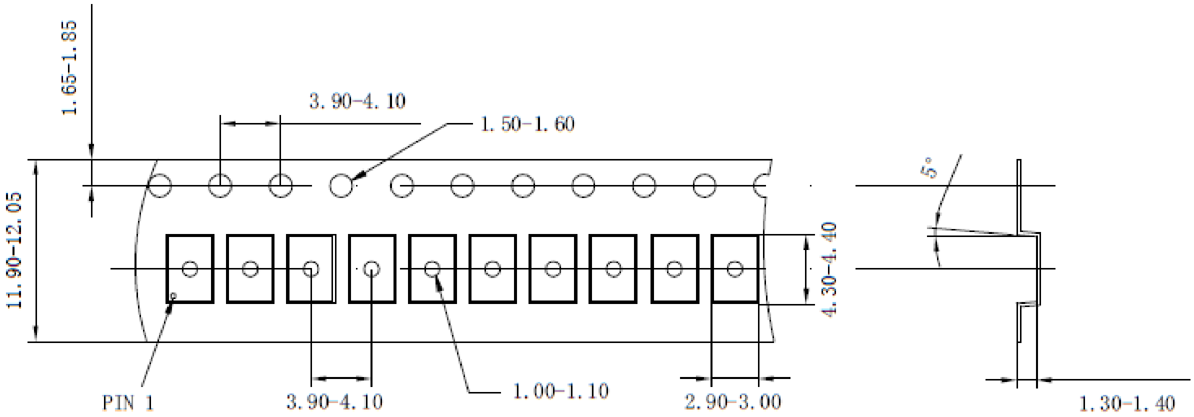


Recommended PCB Layout (Reference Only)

Notes: All dimension in MM and exclude mold flash & metal burr.

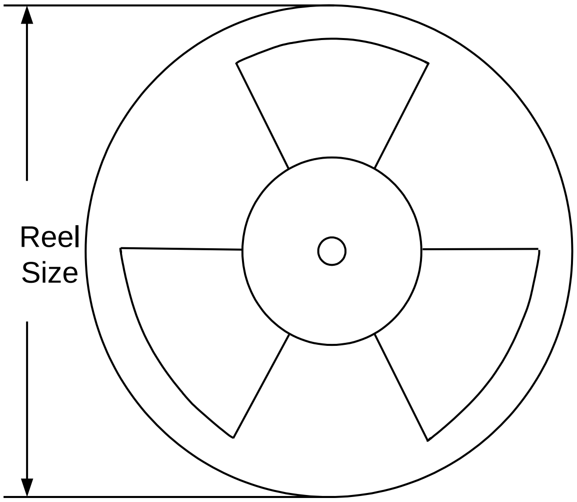
Taping & Reel Specification

1. Taping orientation for packages（CPC8）



Feeding direction →

2. Carrier Tape & Reel specification for packages



Package type	Tape width (mm)	Pocket pitch(mm)	Reel size (Inch)	Trailer length(mm)	Leader length (mm)	Qty per reel
CPC8	**12**	**4**	**13"**	**400**	**400**	**7500**

Revision History

The revision history provided is for informational purpose only and is believed to be accurate, however, not warranted. Please make sure that you have the latest revision.

Date	Revision	Change
June 25, 2024	Revision 1.0	Initial Release

IMPORTANT NOTICE

1. **Right to make changes.** Silergy and its subsidiaries (hereafter Silergy) reserve the right to change any information published in this document, including but not limited to circuitry, specification and/or product design, manufacturing or descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products are sold subject to Silergy's standard terms and conditions of sale.

2. **Applications.** Application examples that are described herein for any of these products are for illustrative purposes only. Silergy makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification. Buyers are responsible for the design and operation of their applications and products using Silergy products. Silergy or its subsidiaries assume no liability for any application assistance or designs of customer products. It is customer's sole responsibility to determine whether the Silergy product is suitable and fit for the customer's applications and products planned. To minimize the risks associated with customer's products and applications, customer should provide adequate design and operating safeguards. Customer represents and agrees that it has all the necessary expertise to create and implement safeguards which anticipate dangerous consequences of failures, monitor failures and their consequences, lessen the likelihood of failures that might cause harm and take appropriate remedial actions. Silergy assumes no liability related to any default, damage, costs or problem in the customer's applications or products, or the application or use by customer's third-party buyers. Customer will fully indemnify Silergy, its subsidiaries, and their representatives against any damages arising out of the use of any Silergy components in safety-critical applications. It is also buyers' sole responsibility to warrant and guarantee that any intellectual property rights of a third party are not infringed upon when integrating Silergy products into any application. Silergy assumes no responsibility for any said applications or for any use of any circuitry other than circuitry entirely embodied in a Silergy product.

3. **Limited warranty and liability.** Information furnished by Silergy in this document is believed to be accurate and reliable. However, Silergy makes no representation or warranty, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information. In no event shall Silergy be liable for any indirect, incidental, punitive, special or consequential damages, including but not limited to lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges, whether or not such damages are based on tort or negligence, warranty, breach of contract or any other legal theory. Notwithstanding any damages that customer might incur for any reason whatsoever, Silergy' aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the Standard Terms and Conditions of Sale of Silergy.

4. **Suitability for use.** Customer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of Silergy components in its applications, notwithstanding any applications-related information or support that may be provided by Silergy. Silergy products are not designed, authorized or warranted to be suitable for use in life support, life-critical or safety-critical systems or equipment, nor in applications where failure or malfunction of an Silergy product can reasonably be expected to result in personal injury, death or severe property or environmental damage. Silergy assumes no liability for inclusion and/or use of Silergy products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

5. **Terms and conditions of commercial sale**. Silergy products are sold subject to the standard terms and conditions of commercial sale, as published at http://www.silergy.com/stdterms, unless otherwise agreed in a valid written individual agreement specifically agreed to in writing by an authorized officer of Silergy. In case an individual agreement is concluded only the terms and conditions of the respective agreement shall apply. Silergy hereby expressly objects to and denies the application of any customer's general terms and conditions with regard to the purchase of Silergy products by the customer.

6. **No offer to sell or license**. Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights. Silergy makes no representation or warranty that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right. Information published by Silergy regarding third-party products or services does not constitute a license to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from Silergy under the patents or other intellectual property of Silergy.

For more information, please visit: www.silergy.com