

High Efficiency, 3.0A, 18V Input Synchronous Step Down Regulator

General Description

The SY8113B1 is a high efficiency, 1.4MHz synchronous step-down DC/DC regulator capable of delivering up to 3A load current. It can operate over a wide input voltage range from 4.5V to 18V and integrate main switch and synchronous switch with very low $R_{DS(ON)}$ to minimize the conduction loss.

The SY8113B1 adopts the instant PWM architecture to achieve fast transient responses for high step down applications. In addition, it operates at pseudo-constant frequency of 1.4MHz to minimize the size of the inductor and the capacitor.

Ordering Information

SY8113

└─ Temperature Code
└─ Package Code
└─ Optional Spec Code

Ordering Number	Package type	Note
SY8113B1ADC	TSOT23-6	----

Features

- Low $R_{DS(ON)}$ for Internal Switches (Top/Bottom): 80mΩ/40mΩ
- 4.5~18V Input Voltage Range
- 3A Output Current Capability
- 1.4MHz Switching Frequency Minimize the External Components
- Stable with 10μF C_{OUT} and 0.68μH Inductor
- Instant PWM Architecture to Achieve Fast Transient Responses
- Internal Soft-start Limits the Inrush Current
- Forced PWM Operation
- Cycle-by-cycle Peak/Valley Current Limitation
- Hic-cup Mode Output Short Circuit Protection
- Thermal Shutdown with Auto Recovery
- Output Auto Discharge Function
- Compact Package: TSOT23-6

Applications

- Set Top Box
- Portable TV
- DSL Modem
- LCD TV
- IP CAM
- Networking

Typical Application

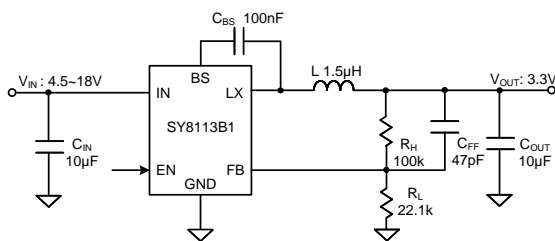


Figure1. Schematic Diagram

Inductor and C_{OUT} Selection Table

V_{OUT} [V]	L [μH]	C_{OUT} [μF]		
		4.7	10	22
1.2	0.68		✓	✓
	1.0		☆	✓
1.8	1.0		✓	✓
	1.5		☆	✓
3.3	1.5		☆	✓
5	2.2		✓	✓
	3.3		☆	✓

Note: '☆' means recommended for most applications.

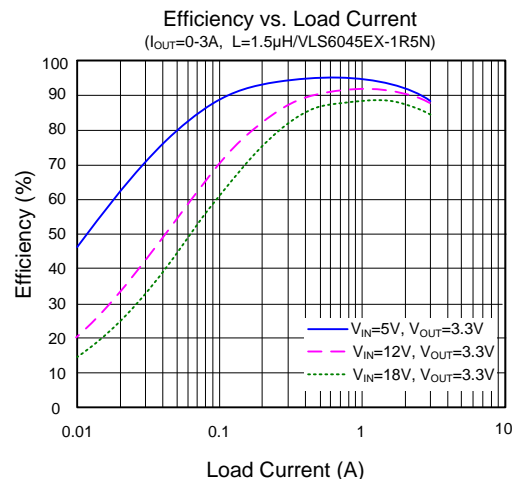
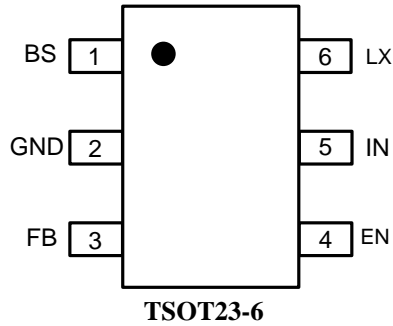


Figure2. Efficiency vs. Output Current

Pinout (top view)



Top mark: **L2xyz** (Device code: L2, x=year code, y=week code, z=lot number code)

Pin Name	Pin Number	Pin Description
BS	1	Boot-strap pin. Supply high side gate driver. Connect a 0.1 μ F ceramic capacitor between the BS and the LX pins.
GND	2	Power ground pin.
FB	3	Output feedback pin. Connect this pin to the center point of the output resistor divider (as shown in Figure 1) to program the output voltage: $V_{OUT}=0.6 \times (1+R_H/R_L)$.
EN	4	Enable control. Pull high to turn on. Do not leave this pin floating.
IN	5	Input pin. Decouple this pin to GND pin with at least a 10 μ F ceramic capacitor.
LX	6	Inductor pin. Connect this pin to the switching node of inductor.

Block Diagram

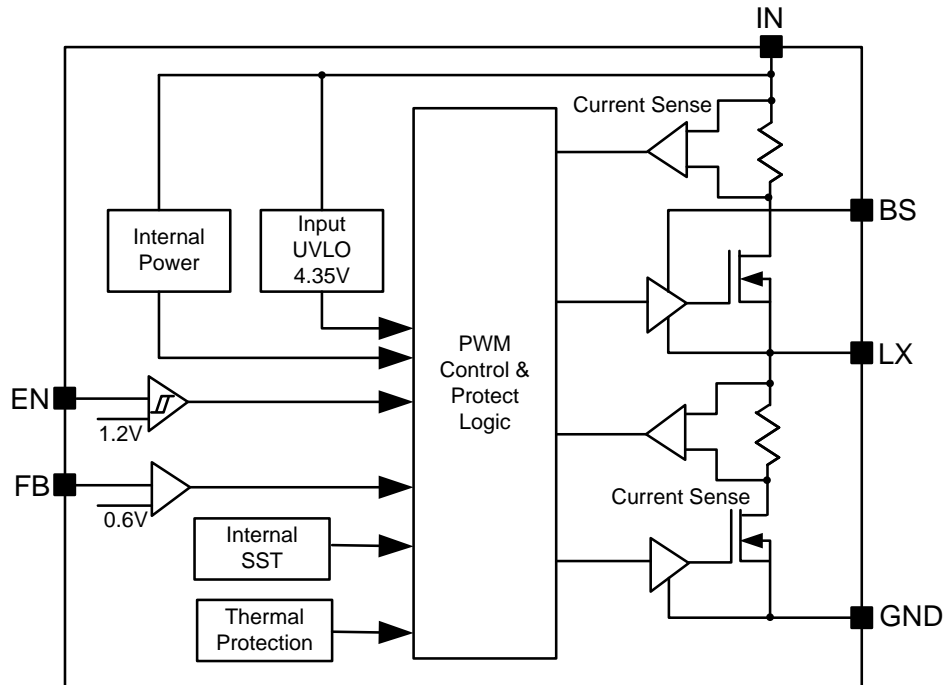


Figure3. Block Diagram

**Absolute Maximum Ratings** (Note 1)

Supply Input Voltage	-----	-0.3V to 19V
LX, EN Voltage	-----	-0.3V to $V_{IN} + 0.3V$
FB, BS-LX Voltage	-----	-0.3V to 4V
Power Dissipation, P_D @ $T_A = 25\text{ }^{\circ}\text{C}$ TSOT23-6,	-----	1.5W
Package Thermal Resistance (Note 2)		
θ_{JA}	-----	66 $^{\circ}\text{C/W}$
θ_{JC}	-----	15 $^{\circ}\text{C/W}$
Junction Temperature Range	-----	-40 $^{\circ}\text{C}$ to 150 $^{\circ}\text{C}$
Lead Temperature (Soldering, 10 sec.)	-----	260 $^{\circ}\text{C}$
Storage Temperature Range	-----	-65 $^{\circ}\text{C}$ to 150 $^{\circ}\text{C}$
Dynamic LX Voltage in 10ns Duration (Note3)	-----	IN+3V to GND-5V

Recommended Operating Conditions (Note 3)

Supply Input Voltage	-----	4.5V to 18V
Junction Temperature Range	-----	-40 $^{\circ}\text{C}$ to 125 $^{\circ}\text{C}$
Ambient Temperature Range	-----	-40 $^{\circ}\text{C}$ to 85 $^{\circ}\text{C}$



Electrical Characteristics

($V_{IN} = 12V$, $V_{OUT} = 3.3V$, $L = 1.5\mu H$, $C_{OUT} = 10\mu F$, $T_A = 25^\circ C$, $I_{OUT} = 1A$ unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Input Voltage Range	V_{IN}		4.5		18	V
Input UVLO Threshold	V_{UVLO}				4.35	V
Input UVLO Hysteresis	V_{HYS}			0.6		V
Shutdown Current	I_{SHDN}	EN=0		5	10	μA
Feedback Reference Voltage	V_{REF}		591	600	609	mV
FB Input Current	I_{FB}	$V_{FB}=3.3V$	-50		50	nA
Output Discharge Resistance	R_{DIS}			40		Ω
Top FET R_{ON}	$R_{DS(ON)1}$			80		m Ω
Bottom FET R_{ON}	$R_{DS(ON)2}$			40		m Ω
EN Rising Threshold	$V_{EN,R}$		1.08	1.2	1.32	V
EN Falling Threshold	$V_{EN,F}$		0.9	1.0	1.1	V
Min ON Time	$t_{ON,MIN}$			50		ns
Min OFF Time	$t_{OFF,MIN}$			200		ns
Turn On Delay	$t_{ON,DLY}$	from EN high to LX start switching		300		μs
Soft-start Time	t_{SS}	V_{OUT} from 0 to 100%		1		ms
Switching Frequency	f_{SW}	$V_{OUT}=3.3V$, CCM		1.4		MHz
Top FET Current Limit	$I_{LIM, TOP}$		4.5			A
Bottom FET Current Limit	$I_{LIM, BOT}$		3			A
Bottom FET Reverse Current Limit	$I_{LIM, RVS}$		1.3			A
Output Under Voltage Protection Threshold	V_{UVP}			33%		V_{REF}
Output UVP Delay	$t_{UVP, DLY}$			100		μs
UVP Hiccup On Time	$t_{UVP, ON}$			2		ms
UVP Hiccup Off Time	$t_{UVP, OFF}$			6		ms
Thermal Shutdown Temperature	T_{SD}			150		$^\circ C$
Thermal Shutdown Hysteresis	T_{HYS}			15		$^\circ C$

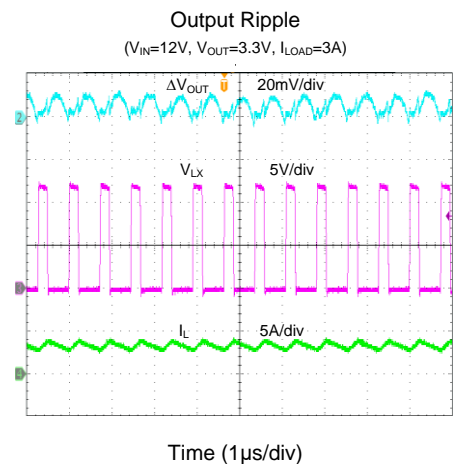
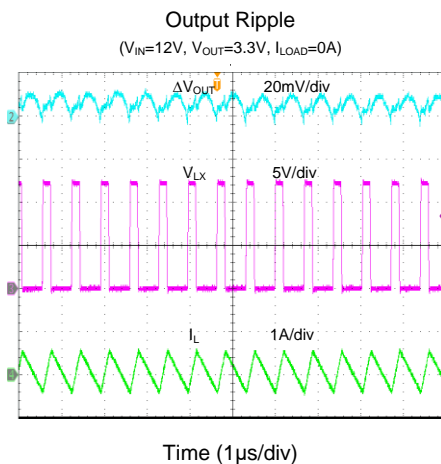
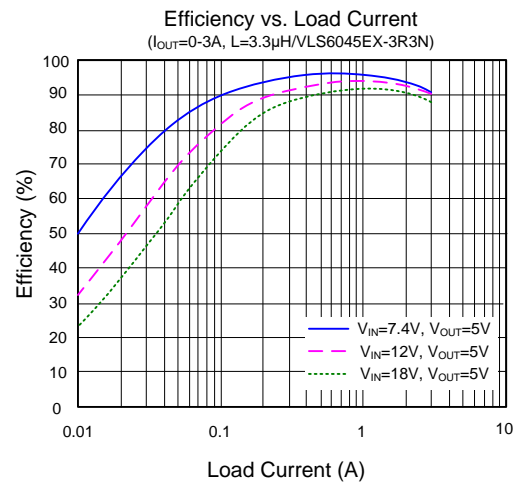
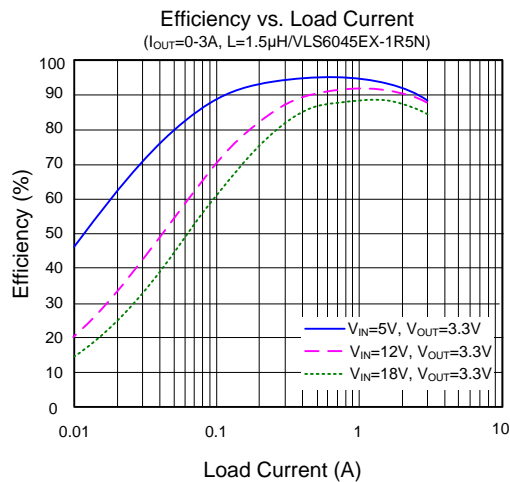
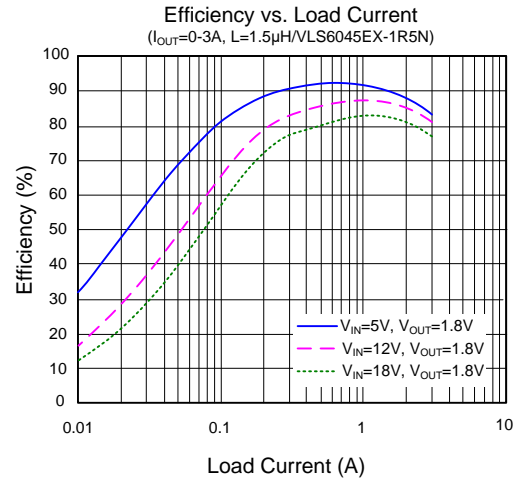
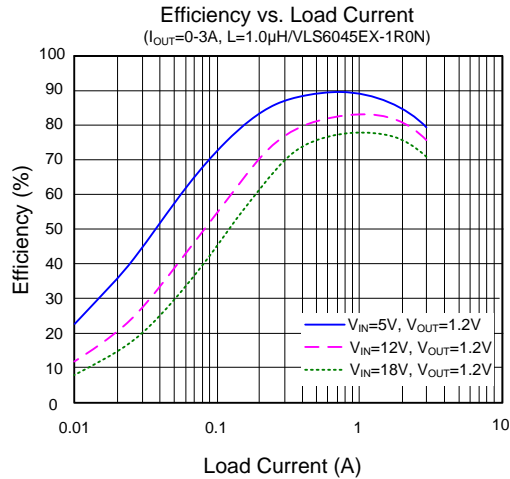
Note 1: Stresses beyond the “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: θ_{JA} is measured in the natural convection at $T_A = 25^\circ C$ on a 2-oz two-layer Silergy evaluation board. Paddle of TSOT23-6 package is the case position for SY8113B1 θ_{JC} measurement.

Note 3: The device is not guaranteed to function outside its operating conditions.

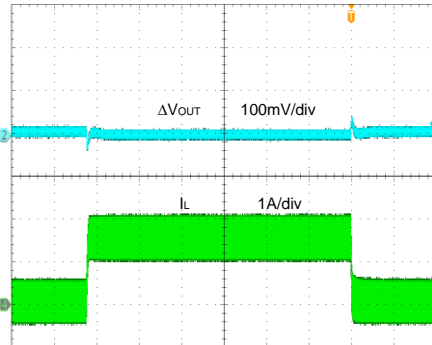
Typical Performance Characteristics

($T_A = 25^\circ\text{C}$, $V_{IN} = 12\text{V}$, $V_{OUT} = 3.3\text{V}$, $C_{OUT} = 10\mu\text{F}$, unless otherwise noted)



Load Transient

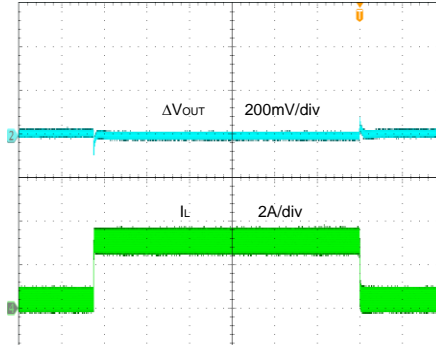
($V_{IN}=12V$, $V_{OUT}=3.3V$, $I_{LOAD}=0-1.5A$)



Time (800 μ s/div)

Load Transient

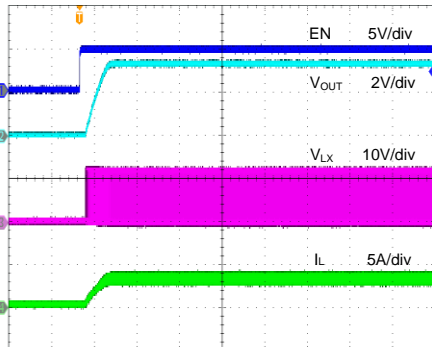
($V_{IN}=12V$, $V_{OUT}=3.3V$, $I_{LOAD}=0.3-3A$)



Time (800 μ s/div)

Startup from Enable

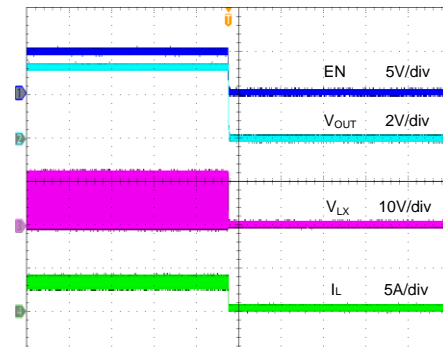
($V_{IN}=12V$, $V_{OUT}=3.3V$, $I_{LOAD}=3A$)



Time (2ms/div)

Shutdown from Enable

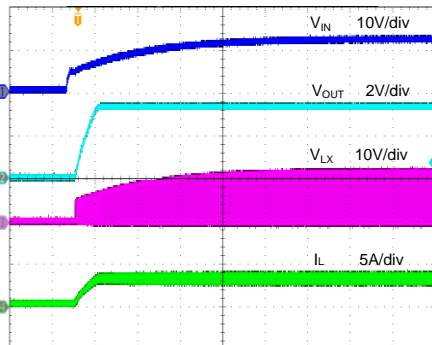
($V_{IN}=12V$, $V_{OUT}=3.3V$, $I_{LOAD}=3A$)



Time (2ms/div)

Startup from V_{IN}

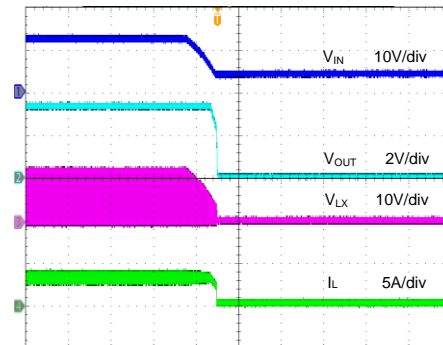
($V_{IN}=12V$, $V_{OUT}=3.3V$, $I_{LOAD}=3A$)



Time (2ms/div)

Shutdown from V_{IN}

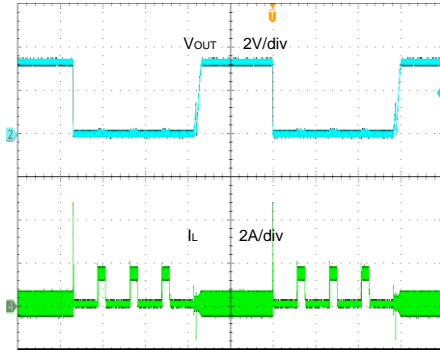
($V_{IN}=12V$, $V_{OUT}=3.3V$, $I_{LOAD}=3A$)



Time (2ms/div)

Short Circuit Protection

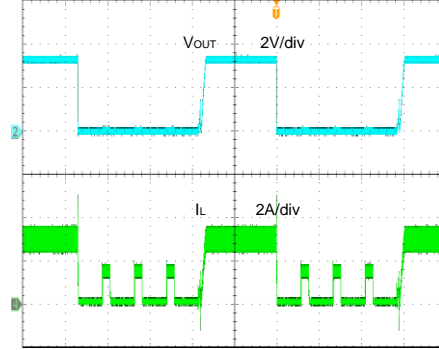
($V_{IN}=12V$, $V_{OUT}=3.3V$, Open to Short)



Time (10ms/div)

Short Circuit Protection

($V_{IN}=12V$, $V_{OUT}=3.3V$, 3A to Short)



Time (10ms/div)

Operation

The SY8113B1 is a high efficiency, 1.4MHz synchronous step-down DC/DC regulator capable of delivering up to 3A load current. It can operate over a wide input voltage range from 4.5V to 18V and integrate main switch and synchronous switch with very low $R_{DS(ON)}$ to minimize the conduction loss. The SY8113B1 adopts the instant PWM architecture to achieve fast transient responses for high step down applications.

The SY8113B1 provides protection functions such as cycle-by-cycle current limiting and thermal shutdown protection. The SY8113B1 will sense the output voltage conditions for the fault protection.

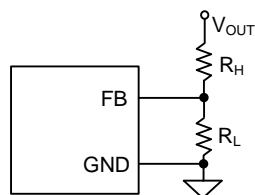
Applications Information

Because of the high integration in the SY8113B1, the application circuit based on this IC is rather simple. Only the input capacitor C_{IN} , the output capacitor C_{OUT} , the inductor L and the feedback resistors (R_H and R_L) need to be selected for the targeted applications specifications.

Feedback Resistor Dividers R_H and R_L

Choose R_H and R_L to program the proper output voltage. To minimize the power consumption under light loads, it is desirable to choose large resistance values for both R_H and R_L . A value of between 10k Ω and 1M Ω is highly recommended for both resistors. If V_{OUT} is 3.3V, $R_H=100k$ is chosen, then using the following equation, R_L can be calculated to be 22.1k:

$$R_L = \frac{0.6V}{V_{OUT} - 0.6V} R_H$$



Input Capacitor C_{IN}

The ripple current through the input capacitor is calculated as:

$$I_{CIN_RMS} = I_{OUT} \times \sqrt{D \times (1-D)}$$

Place a typical X5R or a better grade ceramic capacitor really close to the IN and GND pins to minimize the potential noise problem. Care should be taken to minimize the loop area formed by C_{IN} , and IN/GND pins. In this case, a 10 μ F low ESR ceramic capacitor is recommended.

Output Capacitor C_{OUT}

The output capacitor is selected to handle the output ripple noise requirements. Both steady state ripple and transient requirements must be taken into consideration when selecting this capacitor. For the best performance, it is recommended to use an X5R or a better grade ceramic capacitor with 16V rating and more than 10 μ F capacitance.

Output Inductor L

There are several considerations in choosing this inductor.

- 1) Choose the inductance to provide the desired ripple current. It is suggested to choose the ripple current to be about 40% of the maximum output current. The inductance is calculated as:

$$L = \frac{V_{OUT}(1 - V_{OUT}/V_{IN,MAX})}{f_{SW} \times I_{OUT,MAX} \times 40\%}$$

Where f_{SW} is the switching frequency and $I_{OUT,MAX}$ is the maximum load current.

The IC is quite tolerant of different ripple current amplitudes. Consequently, the final choice of the inductance can be slightly off the calculation value without significantly impacting the performance.

- 2) For FCCM mode converter, in order to avoid the Reverse Current Limit (1.3A min) being triggered at open load condition, when choosing the inductance, we have to make sure the 1/2 inductor ripple current (ΔI) is smaller than the Reverse Current Limit threshold. Otherwise the output voltage will be charged to higher value. The 1/2 inductor ripple current is calculated as:

$$\frac{1}{2} \Delta I = \frac{V_{OUT}(V_{IN} - V_{OUT})}{2 \times L \times f_{SW} \times V_{IN}} \leq 1.3$$

Where f_{SW} is the switching frequency and 1.3 is Bottom FET Reverse Current Limit. So the inductance can be calculated as:

$$L \geq \frac{V_{OUT}(V_{IN} - V_{OUT})}{2.6 \times V_{IN} \times f_{SW}}$$

- 3) The saturation current rating of the inductor must be selected to be greater than the peak inductor current under full load conditions.

$$I_{SAT, MIN} > I_{OUT, MAX} + \frac{V_{OUT}(1 - V_{OUT}/V_{IN, MAX})}{2 \times f_{SW} \times L}$$

- 4) The DCR of the inductor and the core loss at the switching frequency must be low enough to achieve the desired efficiency requirement. It is desirable to choose an inductor with $DCR < 50m\Omega$ to achieve good overall efficiency.

Minimum Duty Cycle and Maximum Duty Cycle

In the COT architecture, there is no limitation for small duty cycles, since even at very low duty cycles; the switching frequency can be reduced as needed once the on-time is close to the minimum on-time, to always ensure a proper operation.

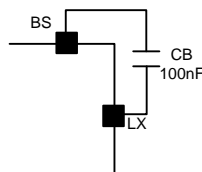
The device can support at least 54% maximum duty cycle operation under $-40^{\circ}C \sim 125^{\circ}C$ condition.

Soft-start

The SY8113B1 has a built-in soft-start to control the rising rate of the output voltage and limit the input current surge during the IC start-up. The typical soft-start time is 1ms.

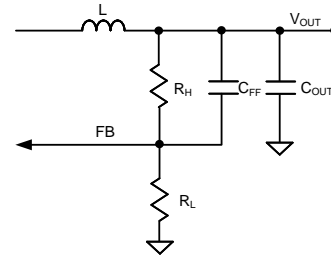
External Bootstrap Capacitor

This capacitor provides the gate driver voltage for the internal high side MOSFET. A 100nF low ESR ceramic capacitor connected between BS pin and LX pin is recommended.



Load Transient Considerations

The SY8113B1 integrates the compensation components to achieve good stability and fast transient responses. Adding a small ceramic capacitor in parallel with R_H will further speed up the load transient responses.

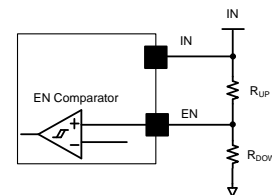


OCP and SCP Protection Method

If the high side power FET current gets higher than the peak current limit threshold, the high side power FET will turn off and the low side power FET will turn on. If the low side FET current gets higher than the valley current limit threshold, the low side FET will keep turning on until low side FET current decreases below the valley current limit threshold. So both peak and valley current are limited. If the load current continues to increase in these conditions, the output voltage will drop. When the output voltage falls below 33% of the regulation level, the output short will be detected and the IC will operate in hic-cup mode. The hic-cup on time will be 2ms and hic-cup off time will be 6ms. If the hard short is removed, the IC will return to normal operation.

Enable and Adjusting Under Voltage Lockout

The EN pin has accurate rising and falling threshold, it provides programmable ON/OFF control by connecting an external resistor divider. Once the EN pin voltage exceeds the rising threshold, the device will start operation. If the EN pin voltage is pulled below the falling threshold, the regulator will stop switching and enter the shutdown state.



It is not recommended to connect EN and IN directly. A resistor in a range of $1k\Omega$ to $1M\Omega$ should be adopted if EN is pulled high by IN.

Layout Design

The layout design of the SY8113B1 is relatively simple. For the best efficiency and to minimize the noise problem, we should place the following components close to the IC: C_{IN} , L, R_H and R_L .

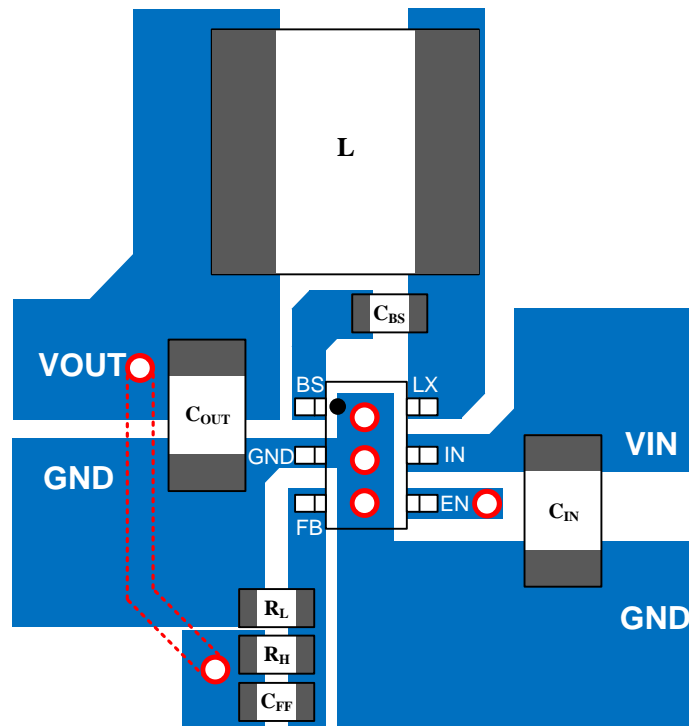
- 1) It is desirable to maximize the PCB copper area connecting to GND pin to achieve the best thermal and noise performance. If the board

space allows, a ground plane will be highly desirable.

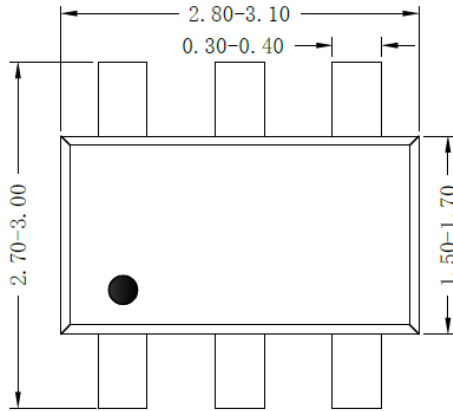
- 2) C_{IN} must be close to IN and GND pins. The loop area formed by C_{IN} and GND must be minimized.
- 3) The PCB copper area associated with LX pin must be minimized to avoid the potential noise problem.
- 4) The components R_H and R_L , and the trace connected to the FB pin must NOT be adjacent

to the LX net on the PCB layout to avoid the noise problem.

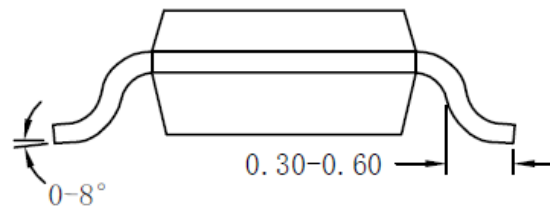
- 5) If the system chip interfacing with the EN pin has a high impedance state in the shutdown mode and the IN pin is connected directly to a power source such as a Li-Ion battery, it is desirable to add a pull-down $1M\Omega$ resistor between the EN and GND pins to prevent the noise from falsely turning on the regulator.



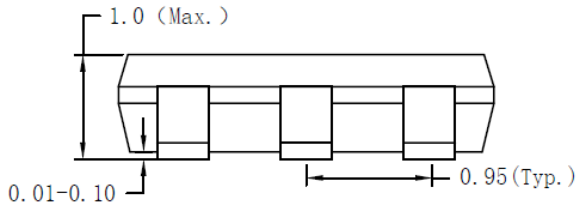
TSOT23-6 Package Outline & PCB Layout



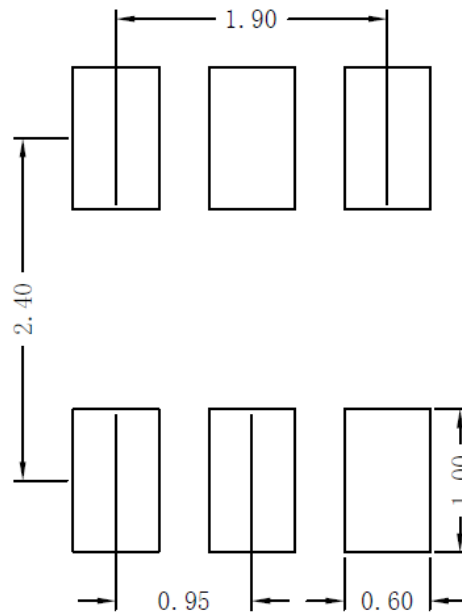
Top view



Side view



Front view



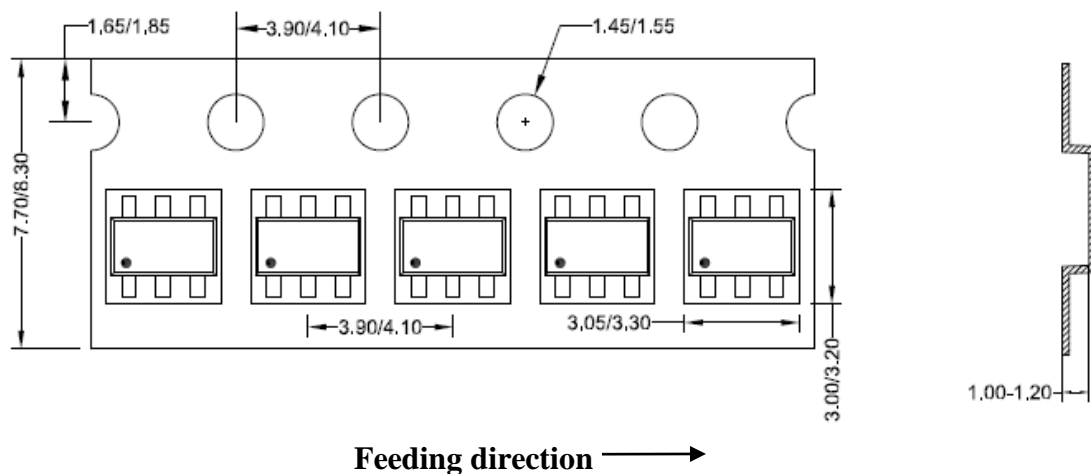
Recommended Pad Layout

Notes: All dimension in millimeter and exclude mold flash & metal burr.

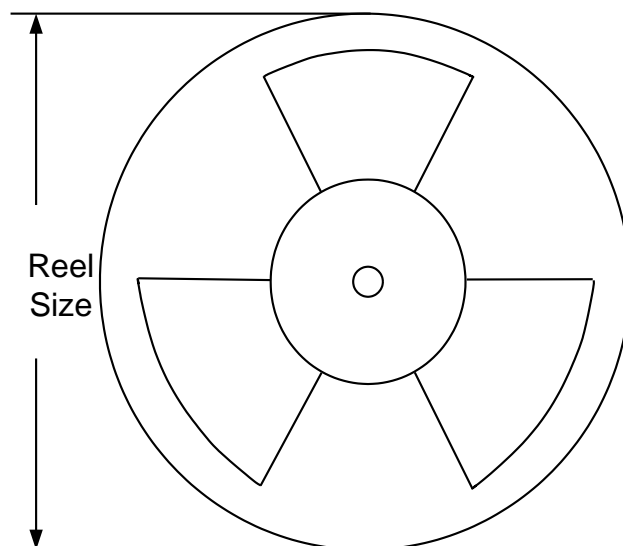
Taping & Reel Specification

1. Taping orientation

TSOT23-6



2. Carrier Tape & Reel specification for packages



Package types	Tape width (mm)	Pocket pitch(mm)	Reel size (Inch)	Trailer length(mm)	Leader length (mm)	Qty per reel
TSOT23-6	8	4	7"	400	160	3000

3. Others: NA

IMPORTANT NOTICE

1. **Right to make changes.** Silergy and its subsidiaries (hereafter Silergy) reserve the right to change any information published in this document, including but not limited to circuitry, specification and/or product design, manufacturing or descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products are sold subject to Silergy's standard terms and conditions of sale.
2. **Applications.** Application examples that are described herein for any of these products are for illustrative purposes only. Silergy makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification. Buyers are responsible for the design and operation of their applications and products using Silergy products. Silergy or its subsidiaries assume no liability for any application assistance or designs of customer products. It is customer's sole responsibility to determine whether the Silergy product is suitable and fit for the customer's applications and products planned. To minimize the risks associated with customer's products and applications, customer should provide adequate design and operating safeguards. Customer represents and agrees that it has all the necessary expertise to create and implement safeguards which anticipate dangerous consequences of failures, monitor failures and their consequences, lessen the likelihood of failures that might cause harm and take appropriate remedial actions. Silergy assumes no liability related to any default, damage, costs or problem in the customer's applications or products, or the application or use by customer's third-party buyers. Customer will fully indemnify Silergy, its subsidiaries, and their representatives against any damages arising out of the use of any Silergy components in safety-critical applications. It is also buyers' sole responsibility to warrant and guarantee that any intellectual property rights of a third party are not infringed upon when integrating Silergy products into any application. Silergy assumes no responsibility for any said applications or for any use of any circuitry other than circuitry entirely embodied in a Silergy product.
3. **Limited warranty and liability.** Information furnished by Silergy in this document is believed to be accurate and reliable. However, Silergy makes no representation or warranty, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information. In no event shall Silergy be liable for any indirect, incidental, punitive, special or consequential damages, including but not limited to lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges, whether or not such damages are based on tort or negligence, warranty, breach of contract or any other legal theory. Notwithstanding any damages that customer might incur for any reason whatsoever, Silergy's aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the Standard Terms and Conditions of Sale of Silergy.
4. **Suitability for use.** Customer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of Silergy components in its applications, notwithstanding any applications-related information or support that may be provided by Silergy. Silergy products are not designed, authorized or warranted to be suitable for use in life support, life-critical or safety-critical systems or equipment, nor in applications where failure or malfunction of an Silergy product can reasonably be expected to result in personal injury, death or severe property or environmental damage. Silergy assumes no liability for inclusion and/or use of Silergy products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.
5. **Terms and conditions of commercial sale.** Silergy products are sold subject to the standard terms and conditions of commercial sale, as published at <http://www.silergy.com/stdterms>, unless otherwise agreed in a valid written individual agreement specifically agreed to in writing by an authorized officer of Silergy. In case an individual agreement is concluded only the terms and conditions of the respective agreement shall apply. Silergy hereby expressly objects to and denies the application of any customer's general terms and conditions with regard to the purchase of Silergy products by the customer.
6. **No offer to sell or license.** Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights. Silergy makes no representation or warranty that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right. Information published by Silergy regarding third-party products or services does not constitute a license to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from Silergy under the patents or other intellectual property of Silergy.

For more information, please visit: www.silergy.com

© 2019 Silergy Corp.

All Rights Reserved.