



# SY8293

## High Efficiency, 800kHz, 40V Input, 3A Non-synchronous Step Down Regulator

### General Description

The SY8293 is a high efficiency 800 kHz, adaptive constant OFF time controlled non-synchronous step-down DC-DC regulator capable of delivering 3A output current respectively. The SY8293 can operate over a wide input voltage range from 5V to 40V and integrate the main switch with very low  $R_{DS(ON)}$  to minimize the conduction loss.

Low output voltage ripple and small external inductor and capacitor sizes are achieved with 800 kHz switching frequency.

### Ordering Information

SY8293 □(□□)□  
 □ Temperature Code  
 □ Package Code  
 □ Optional Spec Code

| Ordering Number | Package type | Note |
|-----------------|--------------|------|
| SY8293FCC       | SO8E         | --   |

### Features

- 5-40V Input Voltage Range
- Low  $R_{DS(ON)}$  for Internal N-Channel Power FET: 180 mΩ
- 800kHz Switching Frequency
- Adaptive Constant OFF Time Control
- Internal Soft-start Limits the Inrush Current
- 2% 0.6V Reference
- RoHS Compliant and Halogen Free
- Compact Package: SO8E

### Applications

- Set Top Box
- Portable TV
- Access Point Router
- DSL Modem
- LCD TV

### Typical Applications

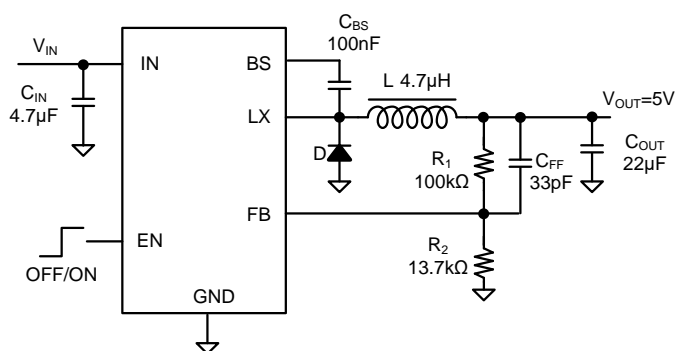


Figure 1. Schematic Diagram

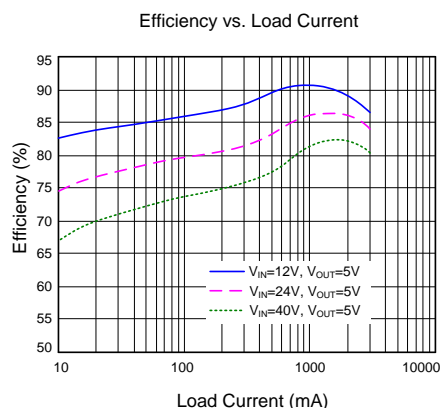
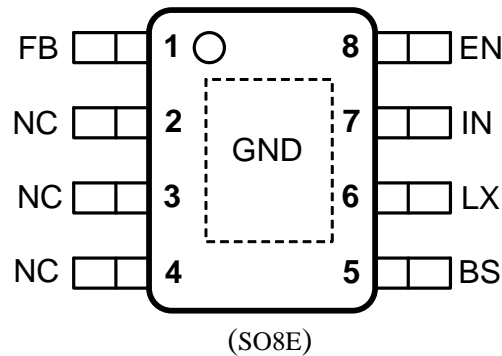


Figure2. Efficiency Figure

**Pinout** (top view)



Top Mark: ARZxyz (Device code: ARZ, x=year code, y=week code, z=lot number code)

| Pin Name | Pin Number     | Pin Description  |
|----------|----------------|--|
| FB       | 1              | Output feedback pin. Connect this pin to the center point of the output resistor divider (as shown in Figure 1) to program the output voltage:<br>$V_{OUT}=0.6 \times (1+R_1/R_2)$ |
| GND      | Exposed paddle | Ground pin   |
| BS       | 5              | Boot-strap pin. Supply high side gate driver. Decouple this pin to the LX pin with a 0.1μF ceramic capacitor.  |
| LX       | 6              | Inductor pin. Connect this pin to the switching node of inductor   |
| IN       | 7              | Input pin. Decouple this pin to GND pin with at least a 4.7μF ceramic capacitor.   |
| EN       | 8              | Enable control. Pull high to turn on. Do not leave it floating.  |
| NC       | 2, 3, 4        | Not connected.   |

**Absolute Maximum Ratings** (Note 1)

|   |                 |
|---|-----------------|
| Supply Input Voltage                    | 42V             |
| Enable Voltage                          | $V_{IN} + 0.6V$ |
| FB Voltage                              | 3.6V            |
| BS to LX Voltage                        | 3.6V            |
| Power Dissipation, PD @ TA = 25°C, SO8E | 3.3W            |
| Package Thermal Resistance (Note 2)     |                 |
| θJA                                     | 30°C/W          |
| θJC                                     | 10°C/W          |
| Junction Temperature Range              | 150°C           |
| Lead Temperature (Soldering, 10 sec.)   | 260°C           |
| Storage Temperature Range               | -65°C to 150°C  |

**Recommended Operating Conditions** (Note 3)

|                            |                |
|----------------------------|----------------|
| Supply Input Voltage       | 5V to 40V      |
| BS to LX Voltage           | 3.3V           |
| Junction Temperature Range | -40°C to 125°C |
| Ambient Temperature Range  | -40°C to 85°C  |

## Electrical Characteristics

( $V_{IN} = 12V$ ,  $V_{OUT} = 5V$ ,  $L = 3.9\mu H$ ,  $C_{OUT} = 22\mu F$ ,  $T_A = 25^\circ C$ ,  $I_{OUT} = 1A$  unless otherwise specified.)

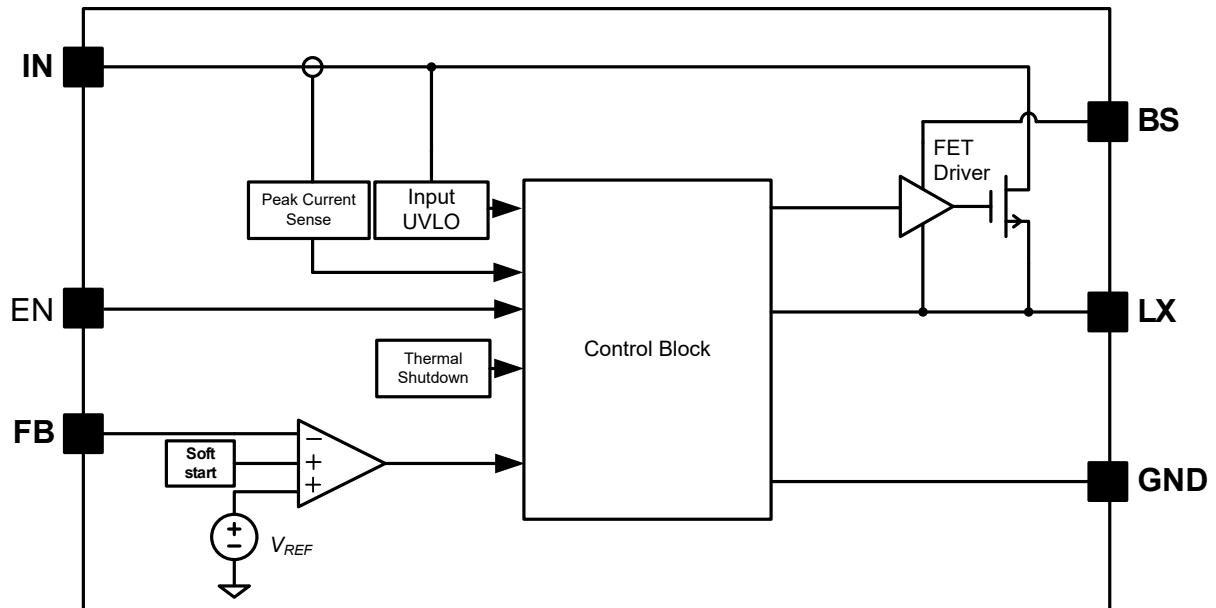
| Parameter                            | Symbol          | Test Conditions                            | Min   | Typ | Max   | Unit       |
|--------------------------------------|-----------------|--|-------|-----|-------|------------|
| Input Voltage Range                  | $V_{IN}$        |  | 5     |     | 40    | V          |
| Input UVLO Threshold                 | $V_{UVLO}$      | Rising                                     |       | 4.5 |       | V          |
| Input UVLO Threshold                 |                 | Falling                                    |       | 4.3 |       | V          |
| Input UVLO Hysteresis                | $V_{UVLO\_HYS}$ |  |       | 200 |       | mV         |
| Quiescent Current                    | $I_Q$           | $I_{OUT}=0$ , $V_{FB}=V_{REF}\times 105\%$ |       | 160 |       | $\mu A$    |
| Shutdown Current                     | $I_{SHDN}$      | $EN=0$                                     |       |     | 10    | $\mu A$    |
| Feedback Reference Voltage           | $V_{REF}$       |  | 0.588 | 0.6 | 0.612 | V          |
| FB Input Current                     | $I_{FB}$        | $V_{FB}=V_{IN}$                            | -50   |     | 50    | nA         |
| Power FET RON                        | $R_{DS(ON)1}$   |  |       | 180 |       | m $\Omega$ |
| Power FET Current Limit              | $I_{LIM}$       |  | 3.4   |     |       | A          |
| EN Rising Threshold                  | $V_{ENH}$       |  | 1.5   |     |       | V          |
| EN Falling Threshold                 | $V_{ENL}$       |  |       |     | 0.4   | V          |
| Minimum OFF Time                     | $t_{OFF}$       |  |       |     | 100   | ns         |
| Minimum ON Time                      | $t_{OFF}$       |  |       |     | 100   | ns         |
| Maximum ON Time                      | $t_{ON}$        |  |       | 2   |       | $\mu s$    |
| Oscillator Frequency                 | $f_{OSC}$       |  |       | 800 |       | kHz        |
| Thermal Shutdown Temperature         | $T_{SD}$        |  |       | 150 |       | $^\circ C$ |
| Thermal Shutdown Recovery Hysteresis | $T_{HYS}$       |  |       | 15  |       | $^\circ C$ |

**Note 1:** Stresses beyond the “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

**Note 2:**  $\theta_{JA}$  is measured in the natural convection at  $T_A = 25^\circ C$  on a low effective single layer thermal conductivity test board of JEDEC 51-3 thermal measurement standard.

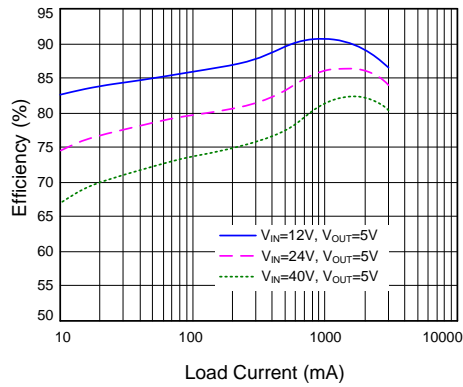
**Note 3:** The device is not guaranteed to function outside its operating conditions.

## Block Diagram



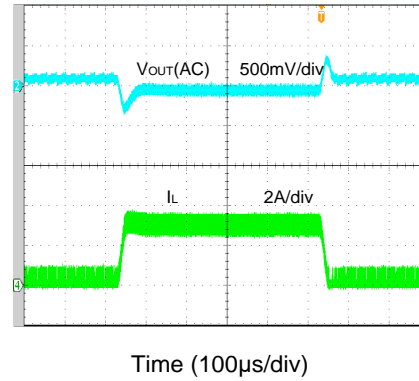
## Typical Performance Characteristics

Efficiency vs. Load Current



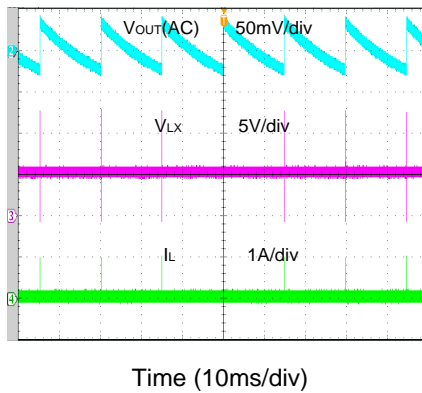
Load Transient

( $V_{IN}=12V, V_{OUT}=5V, I_O=0.3-3A$ )



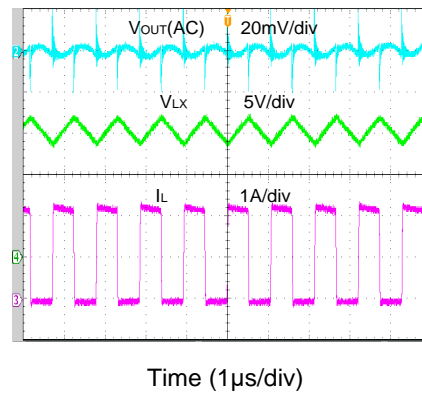
Output Ripple

( $V_{IN}=12V, V_{OUT}=5V, I_O=0A$ )



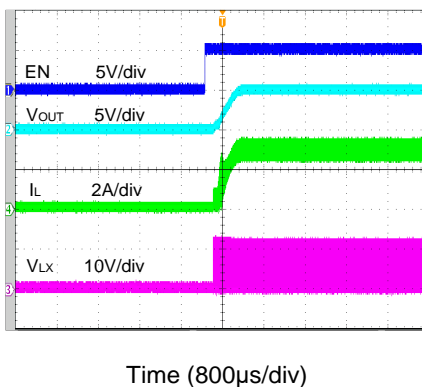
Output Ripple

( $V_{IN}=12V, V_{OUT}=5V, I_O=3A$ )



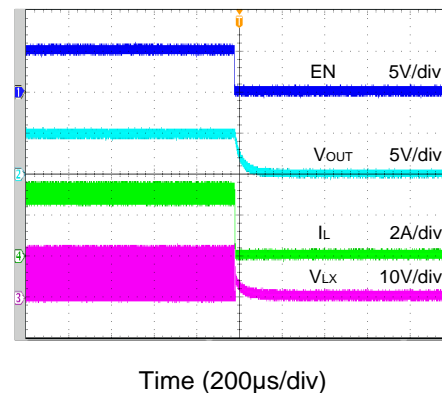
EN Startup

( $V_{IN}=12V, V_{OUT}=5V, I_O=3A$ )



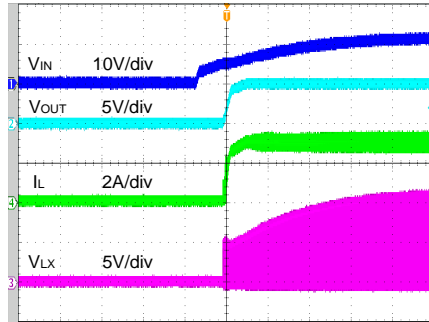
EN Shutdown

( $V_{IN}=12V, V_{OUT}=5V, I_O=3A$ )



## VIN Startup

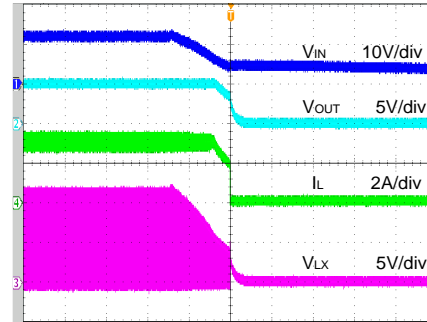
( $V_{IN}=12V$ ,  $V_{OUT}=5V$ ,  $I_O=3A$ )



Time (2ms/div)

## VIN Shutdown

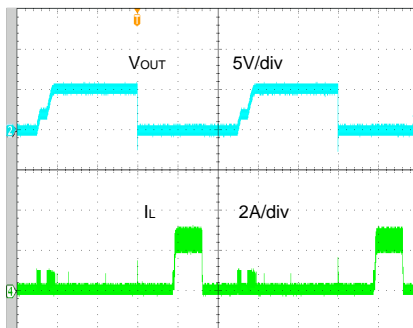
( $V_{IN}=12V$ ,  $V_{OUT}=5V$ ,  $I_O=3A$ )



Time (400μs/div)

## Short Circuit Protection

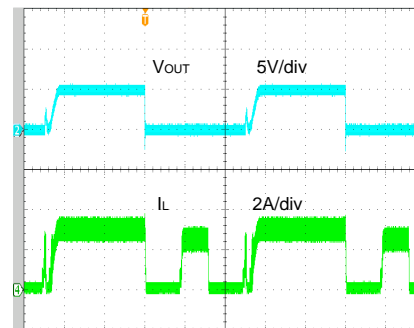
( $V_{IN}=12V$ ,  $V_{OUT}=5V$ , 0A~short)



Time (2ms/div)

## Short Circuit Protection

( $V_{IN}=12V$ ,  $V_{OUT}=5V$ , 3A~short)



Time (2ms/div)

## Operation

SY8293 is an asynchronous Buck regulator that integrates the PWM control, main switch on the same die. With ultra low  $R_{DS(ON)}$  power switch and proprietary PWM control, this regulator can achieve high efficiency and fast transient response. High switch frequency minimizes the external inductor and capacitor size, thus minimize the PCB area and cost. SY8293 also features cycle-by-cycle current limit, output short circuit protection and thermal shutdown protection.

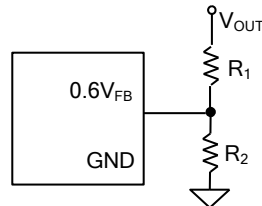
## Applications Information

Because of the high integration in the SY8293, the application circuit based on this regulator IC is rather simple. Only the input capacitor  $C_{IN}$ , the output capacitor  $C_{OUT}$ , the output inductor  $L$ , the rectifier diode  $D$  and the feedback resistors ( $R_1$  and  $R_2$ ) need to be selected for the targeted applications.

### Feedback Resistor Dividers $R_1$ and $R_2$ :

Choose  $R_1$  and  $R_2$  to program the proper output voltage. To minimize the power consumption under light loads, it is desirable to choose large resistance values for both  $R_1$  and  $R_2$ . A value of between  $10k\Omega$  and  $1M\Omega$  is highly recommended for both resistors. If  $V_{OUT}$  is 5V,  $R_1=100k$  is chosen, then using following equation,  $R_2$  can be calculated to be 13.7k:

$$R_2 = \frac{0.6V}{V_{OUT} - 0.6V} R_1$$



### Input Capacitor $C_{IN}$ :

The ripple current through input capacitor is calculated as:

$$I_{CIN\_RMS} = I_{OUT} \times \sqrt{D(1-D)}$$

To minimize the potential noise problem, place a typical X5R or better grade ceramic capacitor really close to the IN pin and the negative end of rectifier. A low ESR ceramic capacitor is recommended with greater than  $4.7\mu F$  capacitance.

### Output Capacitor $C_{OUT}$ :

The output capacitor is selected to handle the output ripple noise requirements. Both steady state ripple and transient requirements must be taken into consideration when selecting this capacitor. For the best performance, it is recommended to use an X5R or better grade ceramic capacitor with greater than  $22\mu F$  capacitance.

### Output Inductor $L$ :

There are several considerations in choosing this inductor.

- 1) Choose the inductance to provide the desired ripple current. It is suggested to choose the ripple current to be about 40% of the maximum output current. The inductance is calculated as:

$$L = \frac{V_{OUT}(1 - V_{OUT}/V_{IN,MAX})}{f_{SW} \times I_{OUT,MAX} \times 40\%}$$

Where  $f_{SW}$  is the switching frequency and  $I_{OUT,MAX}$  is the maximum load current.

The SY8293 is quite tolerant of different ripple current amplitude. Consequently, the final choice of inductance can be slightly off the calculation value without significantly impacting the performance.

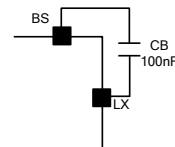
- 2) The saturation current rating of the inductor must be selected to be greater than the peak inductor current under full load conditions.

$$I_{SAT, MIN} > I_{OUT, MAX} + \frac{V_{OUT}(1 - V_{OUT}/V_{IN,MAX})}{2 \times f_{SW} \times L}$$

- 3) The DCR of the inductor and the core loss at the switching frequency must be low enough to achieve the desired efficiency requirement. It is desirable to choose an inductor with  $DCR < 50m\Omega$  to achieve a good overall efficiency.

### External Bootstrap Cap

This capacitor provides the gate driver voltage for internal high side MOSFET. A  $100nF$  low ESR ceramic capacitor connected between the BS pin and the LX pin is recommended.

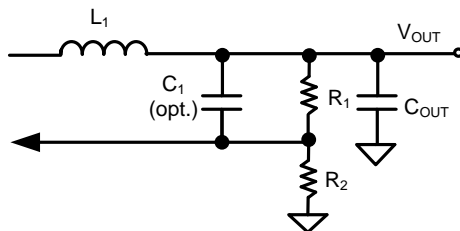


## Rectifier Diode

Because of high switching speed of SY8293, a schottky diode with low forward voltage and fast switching speed is desirable for the application. The voltage rating of the diode must be higher than maximum output voltage. The diode's average and peak current rating should exceed the average output current and peak current.

## Load Transient Considerations:

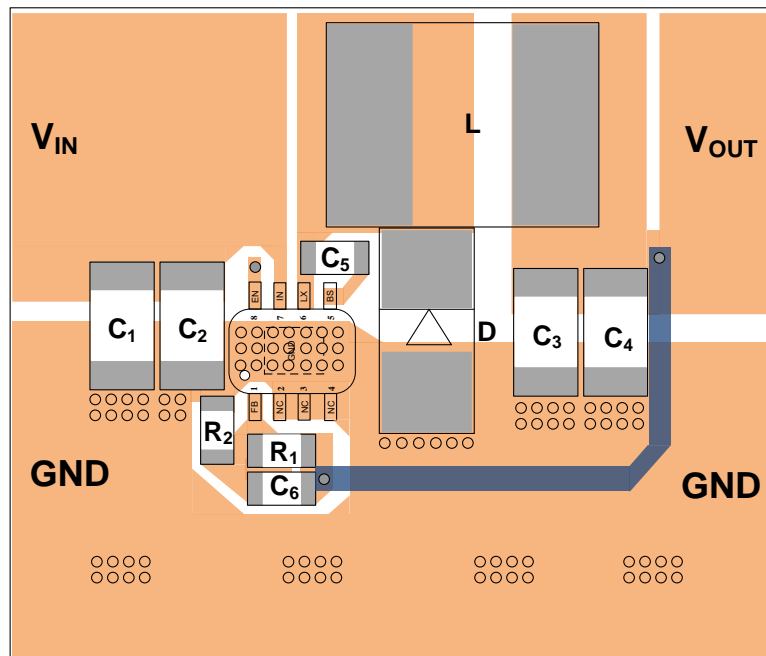
The SY8293 integrates the compensation components to achieve good stability and fast transient responses. In some applications, adding a small ceramic cap in parallel with R1 may further speed up the load transient response and is it is recommended for high step load applications.



## Layout Design:

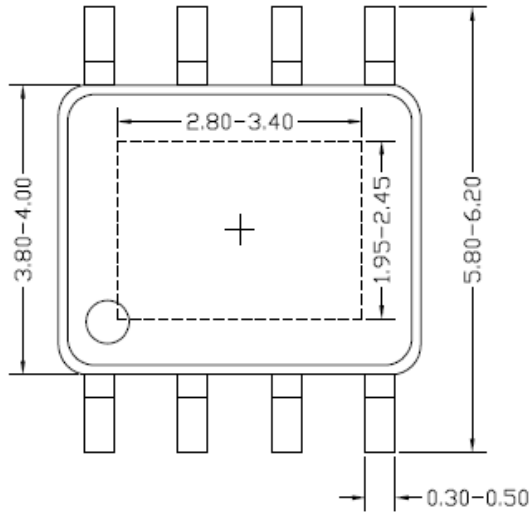
The layout design of SY8293 regulator is relatively simple. For the best efficiency and minimum noise problem, we should place the following components close to the IC:  $C_{IN}$ , L,  $R_1$  and  $R_2$ .

- 1) It is desirable to maximize the PCB copper area connecting to GND pin to achieve the best thermal and noise performance. If the board space allowed, a ground plane is highly desirable.
- 2) The loop area formed by IN, LX,  $C_{IN}$  and the rectifier must be minimized.
- 3) The PCB copper area associated with LX pin must be minimized to avoid the potential noise problem.
- 4) The components  $R_1$  and  $R_2$ , and the trace connecting to the FB pin must NOT be adjacent to the LX net on the PCB layout to avoid the noise problem.
- 5) If the system chip interfacing with the EN pin has a high impedance state at shutdown mode and the IN pin is connected directly to a power source, it is desirable to add a pull down 1MΩ resistor between the EN and GND pins to prevent the noise from falsely turning on the regulator at shutdown mode.

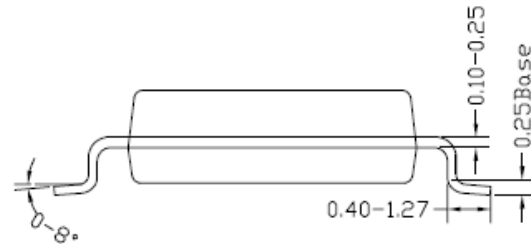




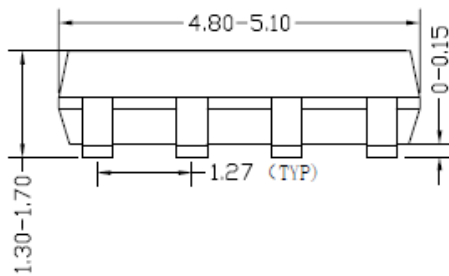
## SO8E Package Outline & PCB layout



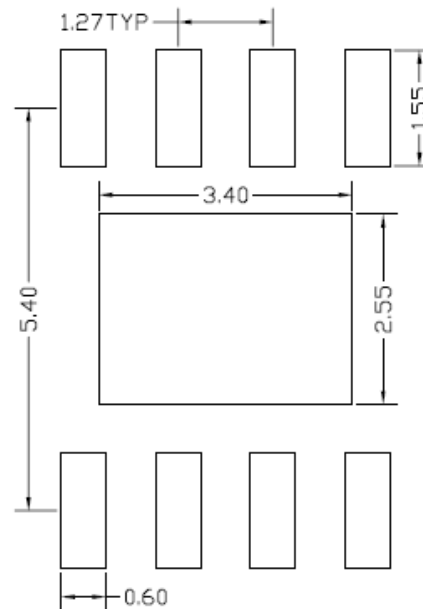
**Top view**



**Side view**



**Front view**



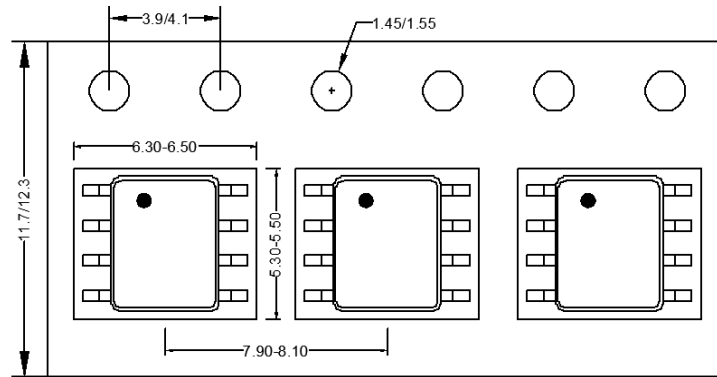
**Recommended PCB layout  
(Reference Only)**

**Notes:** All dimension in millimeter and exclude mold flash & metal burr.

## Taping & Reel Specification

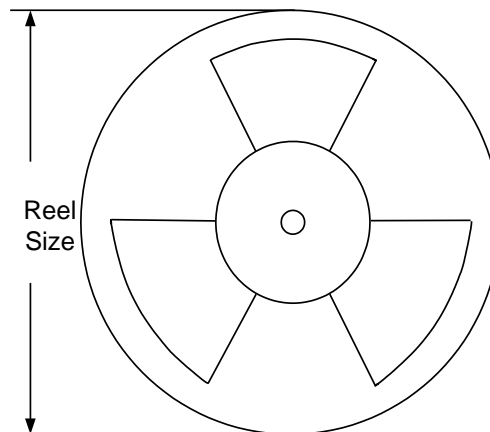
### 1. Taping orientation

**SO8E**



**Feeding direction** →

### 2. Carrier Tape & Reel specification for packages



| Package types | Tape width<br>(mm) | Pocket<br>pitch(mm) | Reel size<br>(Inch) | Trailer *<br>length(mm) | Leader *<br>length (mm) | Qty per reel<br>(pcs) |
|---------------|--------------------|---------------------|---------------------|-------------------------|-------------------------|-----------------------|
| SO8E          | 12                 | 8                   | 13"                 | 400                     | 400                     | 2500                  |

**Others: NA**



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