Application Notes: SY8286B

High Efficiency Fast Response, 6A, 23V Input Synchronous Step Down Regulator

General Description

The SY8286B develops a high efficiency synchronous step-down DC/DC regulator with 3.3V fixed output voltage and 6A current rating. The device integrates main switch and synchronous switch with very low $R_{DS(ON)}$ to minimize the conduction loss. The SY8286B also integrates a 3.3V/100mA LDO with bypass switch and individual enable control.

The SY8286B operates over a wide input voltage range from 4V to 23V. The DC/DC regulator adopts the instant PWM architecture to achieve fast transient responses for high step down applications and high efficiency at light loads. In addition, it operates at pseudo-constant frequency of 600kHz under heavy load conditions to minimize the size of inductor and capacitor.

Ordering Information

SY8286 □(□□)□
- Temperature Code
- Package Code
- Optional Spec Code

Ordering Number	Package type	Note
SY8286BRAC	QFN3×3-20	--

Features

- Low $R_{DS(ON)}$ for Internal Switches (Top/Bottom): 38/19 mΩ
- Wide Input Voltage Range: 4-23V
- 3.3V LDO with Individual Enable Control and Bypass Switch
- Integrated Bypass Switch: 1.5Ω
- Instant PWM Architecture to Achieve Fast Transient Responses
- Internal 1.2ms Soft-start Limits the Inrush Current
- Pseudo-constant Frequency: 600kHz.
- 6A Output Current Capability
- +/-1.5% Output Voltage Accuracy
- Power Good Indicator
- Output Discharge Function
- Output Current Limit Protection
- Short Circuit Latch-off Protection
- Output Over Voltage Latch-off Protection
- Input UVLO
- Over Temperature Protection
- RoHS Compliant and Halogen Free
- Compact Package: QFN3×3-20

Applications

- LCD-TV/Net-TV/3DTV
- Set Top Box
- Notebook
- High Power AP

Typical Applications

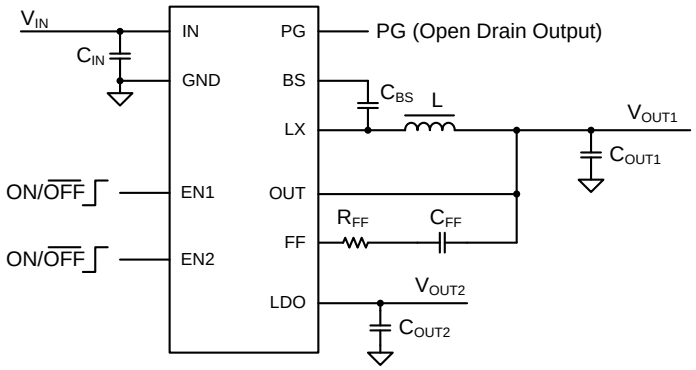


Figure1. Schematic Diagram

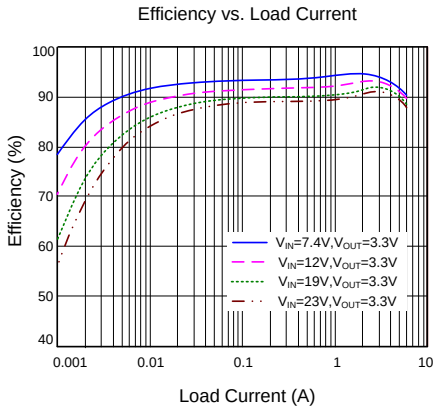
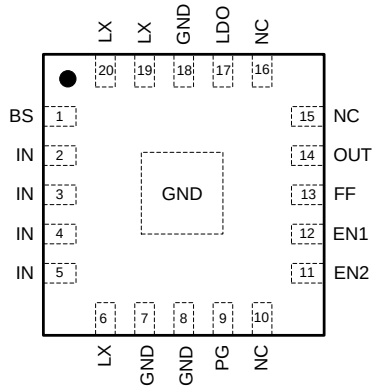


Figure 2. Efficiency vs. Load Current

Pinout (top view)



(QFN3×3-20)

Top Mark: AWV***xyz***, (Device code: AWV, ***x=year code, y=week code, z= lot number code***)

Pin Name	Pin Number	Pin Description
BS	1	Boot-strap pin. Supply high side gate driver. Decouple this pin to the LX pin with a 0.1μF ceramic capacitor.
IN	2,3,4,5	Input pin. Decouple this pin to the GND pin with at least a10μF ceramic capacitor.
LX	6,19,20	Inductor pin. Connect this pin to the switching node of the inductor.
GND	7,8,18,EP	Ground pin.
PG	9	PG is an open-drain output pin. This pin is externally pulled high when the output voltage is within 90% to 120% regulation voltage range. Otherwise this pin is internally pulled low.
NC	10, 15,16	Not connected.
EN2	11	Enable control of the IC and internal LDO. Pull this pin high to turn on the IC and internal LDO. Do not leave this pin floating.
EN1	12	Enable control of the DC/DC regulator. Pull this pin high to turn on the regulator. Do not leave this pin floating.
FF	13	Output feed forward pin. Connect an RC network from the output to this pin.
OUT	14	Output pin. Connect to the output of the DC/DC regulator. The pin also provides the bypass input for the internal LDO.
LDO	17	3.3V LDO output. Decouple this pin to the ground with at least a 4.7uF capacitor.

Block Diagram

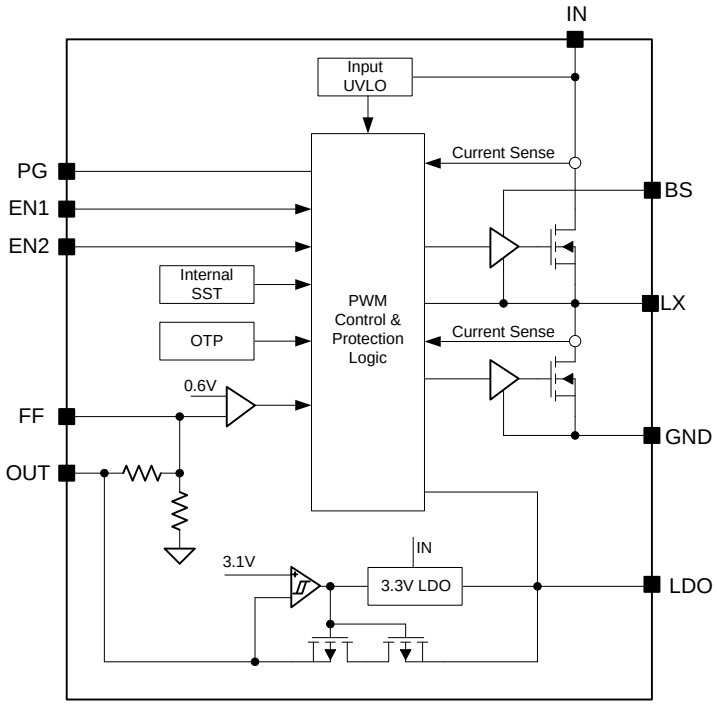


Figure3. Block Diagram

Absolute Maximum Ratings (Note 1)

IN, LX, PG ---------- 25V
BS-LX ---------- 4V
EN1, EN2 ---------- 25V
LDO ---------- 4V
OUT ---------- 6V
FF ---------- 6V
Power Dissipation,
P_D @ T_A = 25℃ QFN3×3-20 ---------- 3.3W
Package Thermal Resistance (Note 2)
θ_{JA}, QFN3×3-20 ---------- 30℃/W
θ_{JC}, QFN3×3-20 ---------- 4.5℃/W
Junction Temperature Range ---------- 150℃
Lead Temperature (Soldering, 10 sec.) ---------- 260℃
Storage Temperature Range ---------- -65℃ to 150℃
Dynamic LX Voltage in 10ns Duration ---------- IN+3V to GND-5V

Recommended Operating Conditions (Note 3)

Supply Input Voltage ---------- 4V to 23V
Junction Temperature Range ---------- -40℃ to 125℃
Ambient Temperature Range ---------- -40℃ to 85℃

Electrical Characteristics

(V_{IN} = 12V, C_{OUT} = 100μF, T_A = 25℃, I_{OUT} = 1A unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Input Voltage Range	V_{IN}		4.0		23	V
Quiescent Current	I_Q	I_{OUT}=0, V_{OUT}=V_{SET}×105%		75	90	μA
Shutdown Current 1	I_{SHDN1}	EN1=0, EN2=1			70	μA
Shutdown Current 2	I_{SHDN2}	EN1=0, EN2=0		6	10	μA
Output Voltage Set-point	V_{SET}		3.319	3.37	3.421	V
Top FET RON	$R_{DS(ON)1}$			38		mΩ
Bottom FET RON	$R_{DS(ON)2}$			19		mΩ
Output Discharge Current	I_{DIS}			70		mA
HSFET FET Current Limit	$I_{LMT,HSFET}$		12			A
Bottom FET Current Limit	$I_{LMT,LSFET}$		8			A
Soft-start Time	T_{SS}			1.2		ms
EN Rising Threshold	V_{ENH}		1			V
EN Falling Threshold	V_{ENL}				0.4	V
Input UVLO Threshold	V_{UVLO}				3.9	V
UVLO Hysteresis	V_{HYS}			0.2		V
Switching Frequency	f_{OSC}		510	600	690	kHz
Min ON Time	$t_{ON,MIN}$	V_{IN}=V_{INMAX}		50		ns
Min OFF Time	$t_{OFF,MIN}$			150		ns
Output Over Voltage Threshold		V_{OUT} rising	115	120	125	%V_{SET}
Output Over Voltage Hysteresis				5		%V_{SET}
Output OVP Delay				20		μs
Output Under Voltage Protection Threshold			55	60	65	%V_{SET}
Output UVP Delay				200		μs
Power Good Threshold		V_{OUT} rising (Good)	87.5	92.5	97.5	%V_{SET}
Power Good Hysteresis				2		%V_{SET}
Power Good Delay		Low to high		200		μs
		High to low		10		μs
LDO Output Voltage	V_{LDO}	V_{IN}=12V, No load	3.201	3.3	3.399	V
LDO Dropout Voltage	$V_{DROPOUT}$	I_{LDO}=100mA		200		mV
LDO Output Current Limit	I_{LMTLDO}		150		300	mA
Bypass Switch RON	R_{BYP}			1.5		Ω
Bypass Switch Turn-on Voltage	V_{BYP}		2.97	3.1		V
Bypass Switch Switchover Hysteresis				0.2		V
Bypass Switch OVP				120		%V_{LDO}
Thermal Shutdown Temperature	T_{SD}			150		℃
Thermal Shutdown Hysteresis	T_{HYS}			15		℃

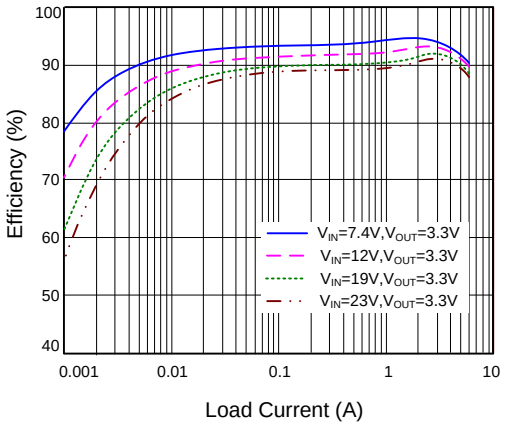
Note 1: Stresses beyond the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: θ_{JA} is measured in the natural convection at T_A = 25℃ on a four-layer Silergy evaluation board.

Note 3: The device is not guaranteed to function outside its operating conditions.

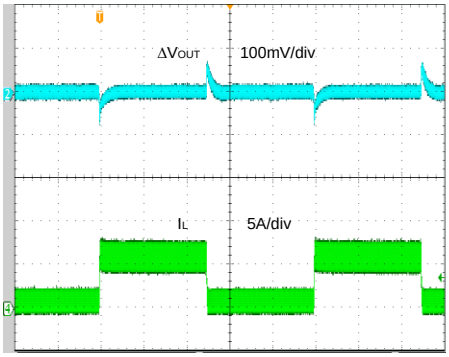
Typical Performance Characteristics

Efficiency vs. Load Current



Load Transient

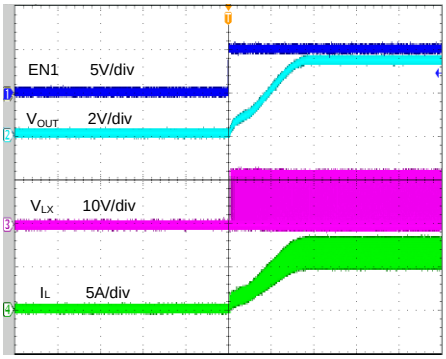
(V_{IN}=12V, V_{OUT}=3.3V, I_{OUT}=0.6-6A)



Time (200μs/div)

Startup from EN1

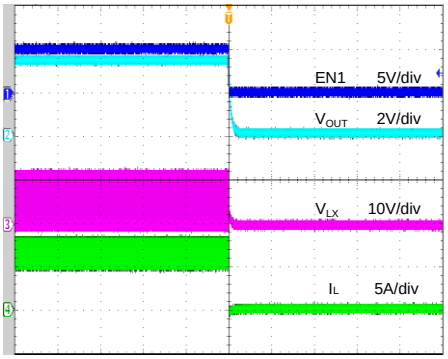
(V_{IN}=12V, V_{OUT}=3.3V, I_{OUT}=6A)



Time (800μs/div)

Shutdown from EN1

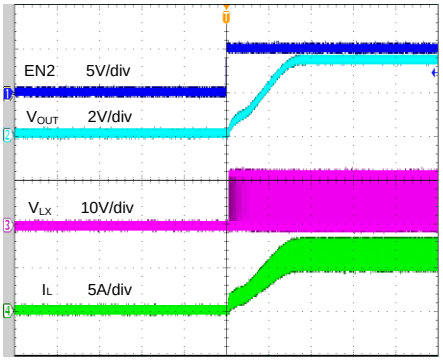
(V_{IN}=12V, V_{OUT}=3.3V, I_{OUT}=6A)



Time (800μs/div)

Startup from EN2

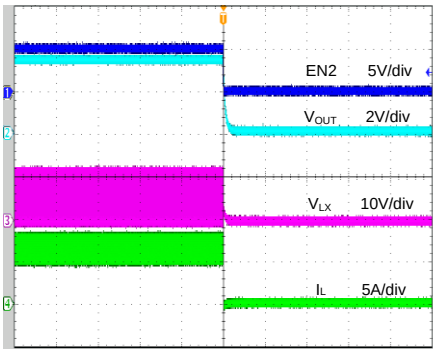
(V_{IN}=12V, V_{OUT}=3.3V, I_{OUT}=6A)



Time (800μs/div)

Shutdown from EN2

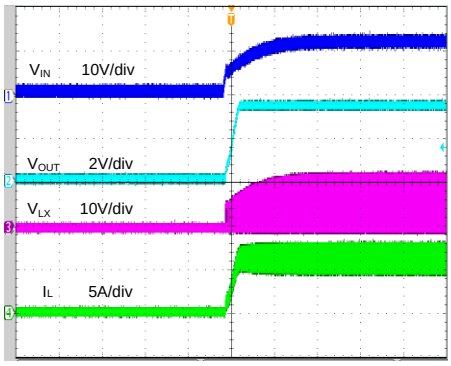
(V_{IN}=12V, V_{OUT}=3.3V, I_{OUT}=6A)



Time (800μs/div)

Startup from V_{IN}

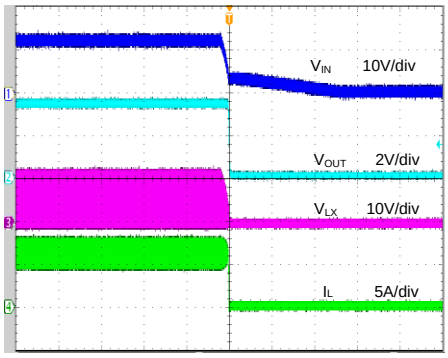
(V_{IN}=12V, V_{OUT}=3.3V, I_{OUT}=6A)



Time (4ms/div)

Shutdown from V_{IN}

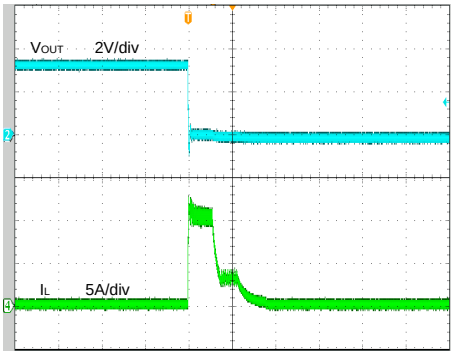
(V_{IN}=12V, V_{OUT}=3.3V, I_{OUT}=6A)



Time (4ms/div)

Short Circuit Protection

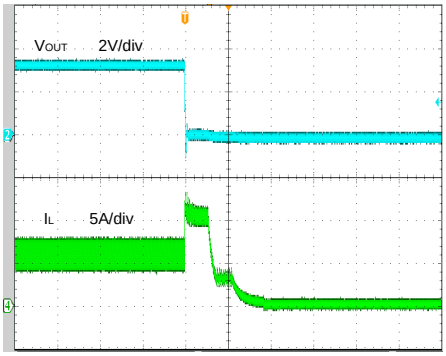
(V_{IN}=12V, V_{OUT}=3.3V,0A to Short)



Time (200μs/div)

Short Circuit Protection

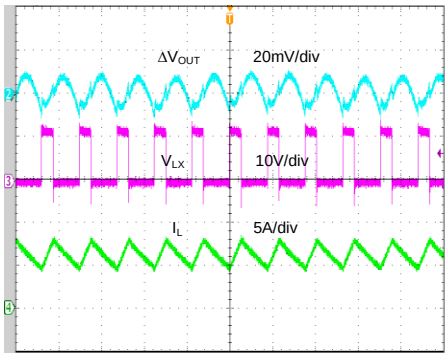
(V_{IN}=12V, V_{OUT}=3.3V, 6A to Short)



Time (200μs/div)

Output Ripple

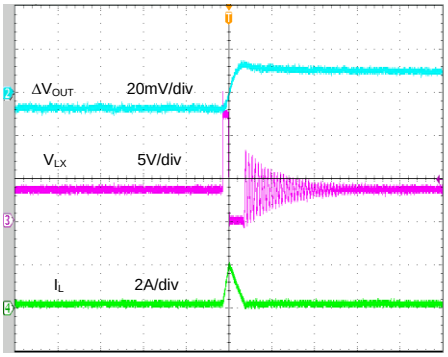
(V_{IN}=12V, V_{OUT}=3.3V, I_{OUT}=6A)



Time (2μs/div)

Output Ripple

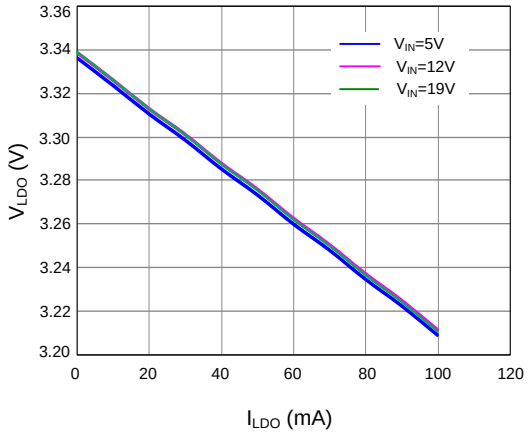
(V_{IN}=12V, V_{OUT}=3.3V, I_{OUT}=0A)



Time (2μs/div)

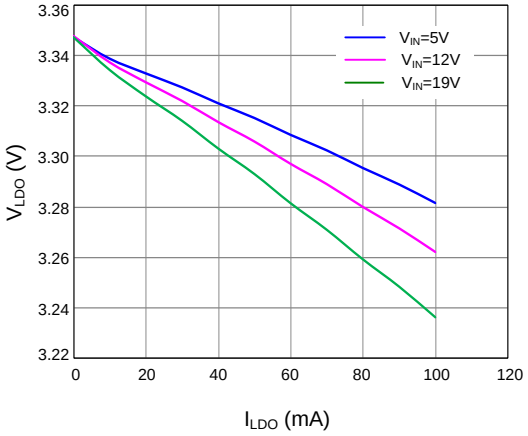
LDO Bypass Regulation

(Bypass Switch Turn-on, EN1=1, EN2=1)



LDO Load Regulation

(Bypass Switch Turn-off, EN1=0, EN2=1)



Operation

The SY8286B develops a high efficiency synchronous step-down DC/DC regulator capable of delivering 6A current. The device integrates main switch and synchronous switch with very low $R_{DS(ON)}$ to minimize the conduction loss.

The SY8286B has a fixed 3.3V DC/DC output and integrates a 3.3V 100mA LDO with bypass switch and individual enable control.

The SY8286B operates over a wide input voltage range from 4V to 23V. The DC/DC regulator adopts the instant PWM architecture to achieve fast transient responses for high step down applications and high efficiency at light loads. In addition, it operates at pseudo-constant frequency of 600kHz under heavy load conditions to minimize the size of inductor and capacitor.

Applications Information

Because of the high integration in the SY8286B, the application circuit based on this regulator is rather simple. Only the input capacitor C_{IN}, the output capacitor C_{OUT} and the output inductor L need to be selected for the targeted applications specifications.

Input Capacitor C_{IN}:

The ripple current through input capacitor is calculated as:

$$I_{CIN\_RMS} = I_{OUT} \times \sqrt{D(1\text{-}D)}\ .$$

To minimize the potential noise problem, a typical X5R or better grade ceramic capacitor should be placed really close to the IN and the GND pins. Care should be taken to minimize the loop area formed by C_{IN}, and the IN/GND pins. In this case, a 10μF low ESR ceramic capacitor is recommended.

Output Capacitor C_{OUT}:

The output capacitor is selected to handle the output ripple noise requirements. Both steady state ripple and transient requirements must be taken into consideration when selecting this capacitor. For most applications, an X5R or better grade ceramic capacitor greater than 66μF capacitance can work well. The capacitance derating with DC voltage must be considered.

Output Inductor L:

There are several considerations in choosing this inductor.

1) Choose the inductance to provide the desired ripple current. It is suggested to choose the ripple current to be about 40% of the maximum output current. The inductance is calculated as:

$$L = \frac{V_{OUT}(1 - V_{OUT}/V_{IN,MAX})}{f_{SW} \times I_{OUT,MAX} \times 40\%}$$

Where fsw is the switching frequency and $I_{OUT,MAX}$ is the maximum load current.

The SY8286B is quite tolerant of different ripple current amplitude. Consequently, the final choice of inductance can be slightly off the calculation value without significantly impacting the performance.

2) The saturation current rating of the inductor must be selected to be greater than the peak inductor current under full load conditions.

$$I_{SAT,MIN} > I_{OUT,MAX} + \frac{V_{OUT}(1\text{-}V_{OUT}/V_{IN,MAX})}{2 \times f_{SW} \times L}$$

3) The DCR of the inductor and the core loss at the switching frequency must be low enough to achieve the desired efficiency requirement. It is desirable to choose an inductor with DCR<10mΩ to achieve a good overall efficiency.

Soft-start

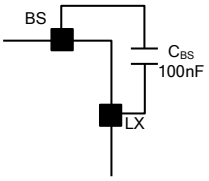
The SY8286B has a built-in soft-start to control the rise rate of the output voltage and limit the input current surge during the IC start-up. The typical soft-start time is 1.2ms.

Enable Operation

The device contains two enable pins to control the LDO and Buck regulator. Driving the EN2 pin high (>0.8V) enables the IC and the LDO. To enable the Buck regulator, both EN1 and EN2 should be driven high. When EN1 and EN2 are driven below 0.4V, the device will be shut down, reducing input current <10μA. For automatic start-up, connect the enable pins to IN directly or through a 100kΩ resistor.

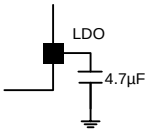
External Bootstrap Capacitor

This capacitor provides the gate driver voltage for internal high side MOSEFET. A 100nF low ESR ceramic capacitor connected between the BS pin and the LX pin is recommended.



LDO

The 3.3V LDO provides the power supply for internal analog circuit and driving circuit. This pin should be bypassed to ground with a 4.7μF ceramic capacitor. This pin is also capable sourcing 100mA current for external load.



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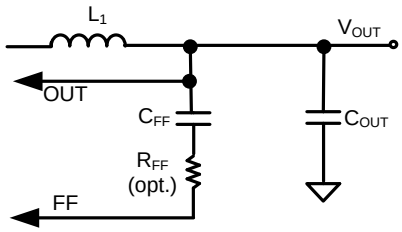
Power Good Indication

PG is an open-drain output pin. This pin will be pulled to ground if the output voltage is lower than 90% of regulation voltage. Otherwise this pin will go to a high impedance state.

Load Transient Considerations:

The SY8286B adopts the instant PWM architecture to achieve good stability and fast transient responses. In applications with high step load current, adding an RC network R_{FF} and C_{FF} between the OUT pin and the FF pin may further speed up the load transient responses.



Layout Design:

The layout design of the SY8286B is relatively simple. For the best efficiency and minimum noise problem, the following components should be placed close to the IC: C_{IN}, C_{LDO}, and L.

1) It is desirable to maximize the PCB copper area connecting to the GND pin to achieve the best thermal and noise performance. If the board space allowed, a ground plane is highly desirable.

2) C_{IN} must be close to the pins IN and GND. The loop area formed by C_{IN} and GND must be minimized.

3) The PCB copper area associated with the LX pin must be minimized to avoid the potential noise problem.

4) If the system chip interfacing with the enable pin has a high impedance state at shutdown mode and the IN pin is connected directly to a power source such as a Li-Ion battery, A 1MΩ pull-down resistor should be placed between the enable pin and the GND pins to prevent the noise from falsely turning on the regulator at shutdown mode.

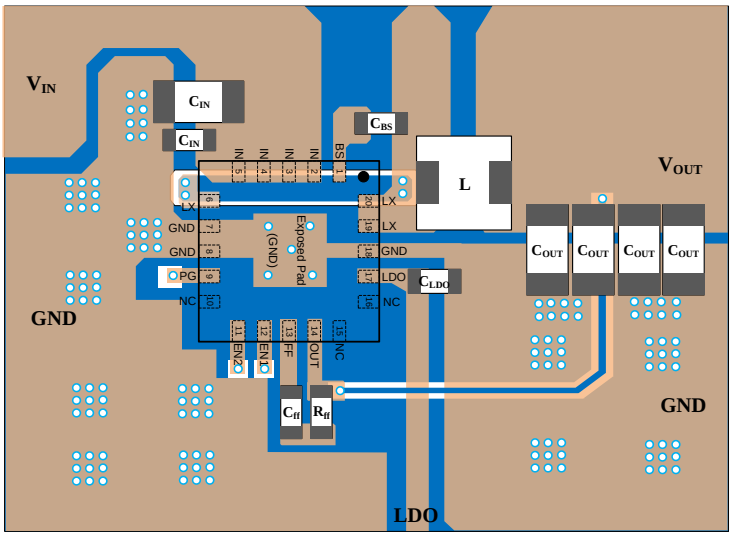
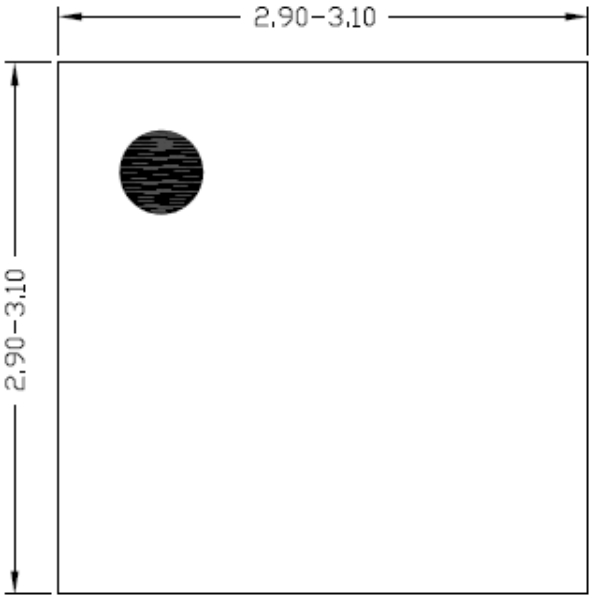
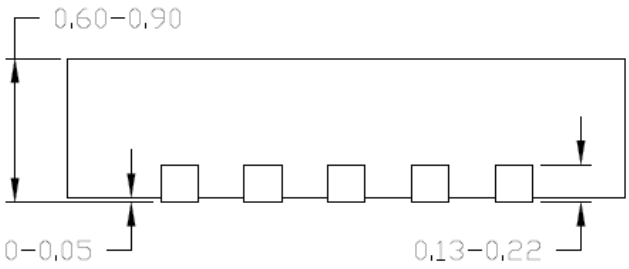


Figure4. PCB Layout Suggestion

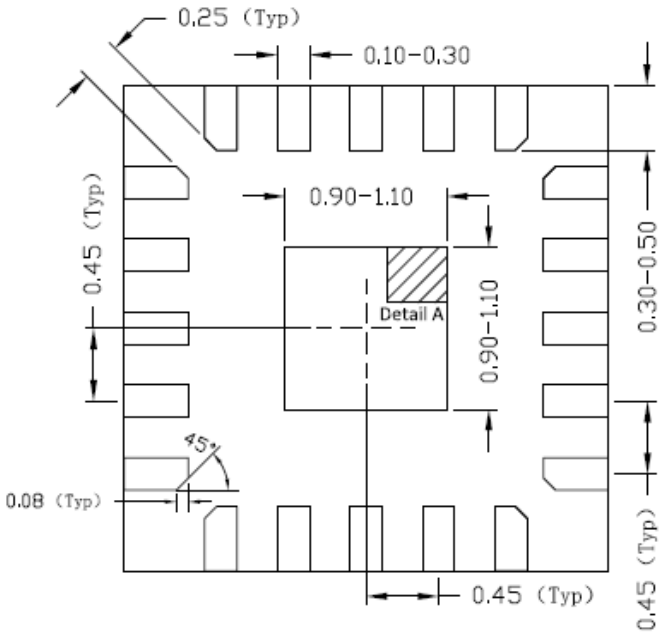
QFN3×3-20 Package Outline

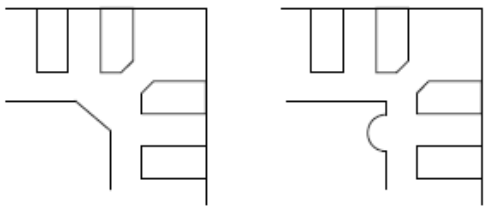


Top view



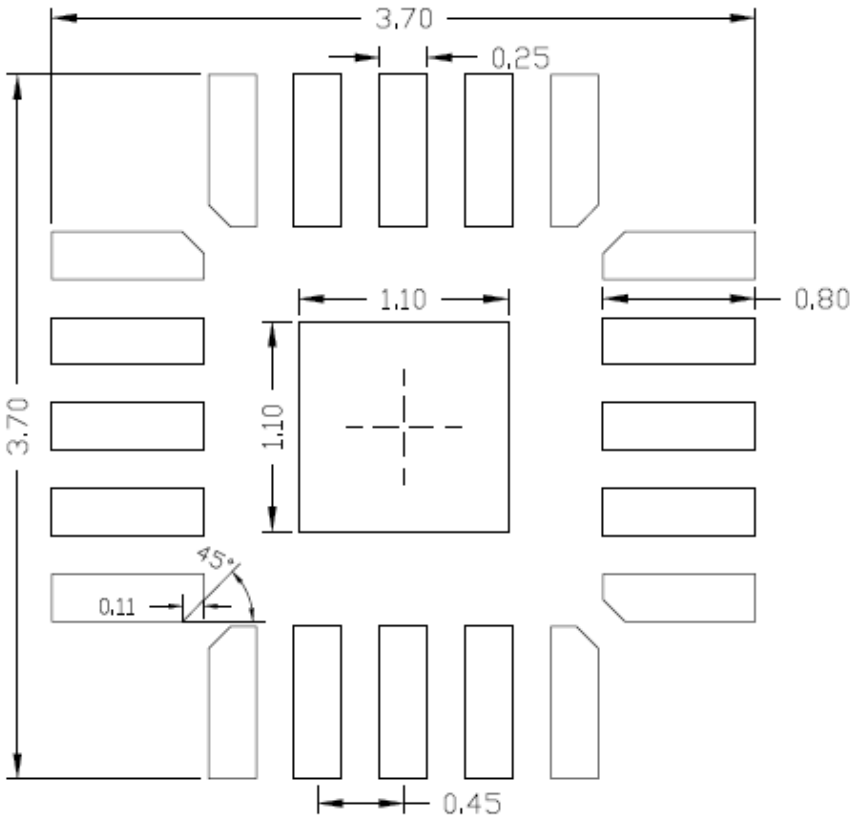
Side view





Detail A
Pin1 Identifier: two options

Bottom view

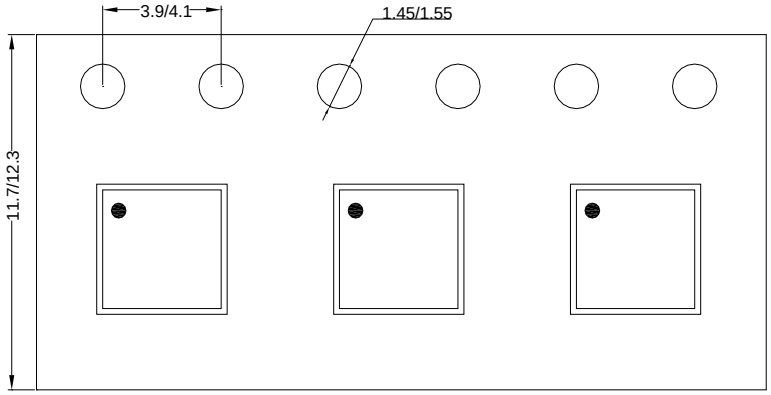


Recommended PCB layout
(Reference only)

Notes: **All dimension in millimeter and exclude mold flash & metal burr.**

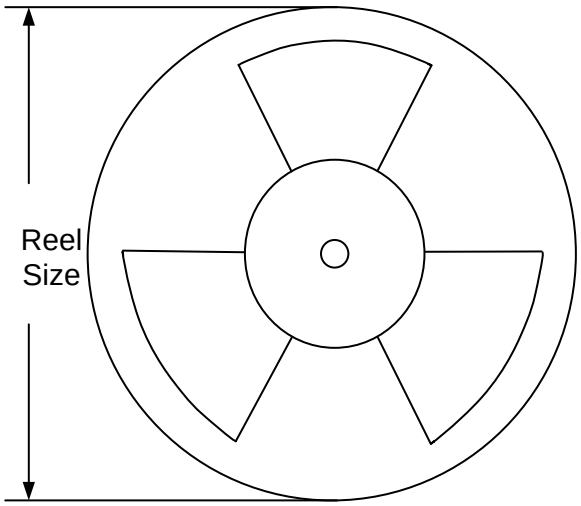
Taping & Reel Specification

1. QFN3×3-20 taping orientation



Feeding direction →

2. Carrier Tape & Reel specification for packages



Package types	Tape width (mm)	Pocket pitch(mm)	Reel size (Inch)	Trailer length(mm)	Leader length (mm)	Qty per reel
QFN3×3	12	8	13"	400	400	5000

3. Others: NA

Revision History

The revision history provided is for informational purpose only and is believed to be accurate, however, not warranted. Please make sure that you have the latest revision.

Date	Revision	Change
Jan 27, 2018	Revision 0.9G	Add “Revision History” in page 13, Important Notice in page 14.
May 30, 2016	Revision 0.9F	Update package outline (Recommended PCB layout)
May 5, 2016	Revision 0.9E	Update package outline (side view)
April 13, 2016	Revision 0.9D	Update the data in EC table (I_Q, I_{SHDN}, $I_{Discharge}$, V_{ENH}, V_{HYS}, V_{PG} threshold/ HYS, V_{LDO}
Dec 31, 2015	Revision 0.9C	Update general description.
Nov 26, 2015	Revision 0.9B	1. Features: Change “+/-1% Internal Vref” to “+/-1.5% output voltage accuracy” 2 PG pin description 2. Enable Operation in Application Information(Page9)
July 15, 2015	Revision 0.9A	Add " dynamic LX voltage" in Abs (Page3)
July 12, 2015	Revision 0.9	Initial Release

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