SY8371B

High Efficiency Fast Response, 10A, 28V Input Synchronous Step Down Regulator

General Description

The SY8371B develops a high efficiency synchronous step-down DC/DC regulator capable of delivering 10A current. The device integrates main switch and synchronous switch with very low $R_{DS(ON)}$ to minimize the conduction loss. In addition, it operates at pseudo constant frequency of 600kHz under heavy load conditions to minimize the size of inductor and capacitor. SY8371B also provides a fixed 3.3V LDO with 100mA current capability, which can be used to power the external peripheries, such as the keyboard controller in notebook. The 3.3V LDO can switch over to Buck regulator output to save power loss.

Silergy's proprietary Instant-PWM™ fast-response, constant-on-time (COT) PWM control method supports high input/output voltage ratios (low duty cycles), and fast transient response while maintaining a near constant operating frequency over line, load and output voltage ranges. This control method provides stable operation without complex compensation and even with low ESR ceramic capacitors.

The SY8371B operates over a wide input voltage range from 4V to 24V. Cycle-by-cycle current limit, input under voltage lock-out, internal soft-start, output under voltage protection, over voltage protection and thermal shutdown provide safe operation in all operating conditions.

Ordering Information

SY8371 □(□□)□
- Temperature Code
- Package Code
- Optional Spec Code

Ordering Number	Package type	Note
SY8371BTMC	QFN3×4-13	--

Features

- Low $R_{DS(ON)}$ for Internal Switches (Top/Bottom): 18/8mΩ
- Wide Input Voltage Range: 4~24V
- Integrated Bypass Switch: 1.5Ω
- Instant PWM Architecture to Achieve Fast Transient Responses
- Internal Soft-start Limits the Inrush Current
- Pseudo-constant Frequency: 600kHz
- Fixed 3.36V Output Voltage
- 10A Output Current Capability
- 100mA LDO Current Capability
- ±1% Internal Reference Voltage
- PFM/USM Selectable Light Load Operation Mode
- Power Good Indicator
- Output Discharge Function
- Cycle-by-cycle Valley Current and Peak Current Limit Protection
- Latch-off Mode Output Under Voltage Protection for Buck
- Latch-off Mode Output Over Voltage Protection for Buck
- Latch-off Mode Over Temperature Protection for Buck
- Auto-recovery Mode Output Under Voltage Protection for LDO
- Auto-recovery Mode Over Temperature Protection for LDO
- Input Under Voltage Lock-out(UVLO)
- RoHS Compliant and Halogen Free
- Compact Package: QFN3×4-13

Applications

- LCD-TV/Net-TV/3DTV
- Set Top Box
- Notebook
- High Power AP

Typical Applications

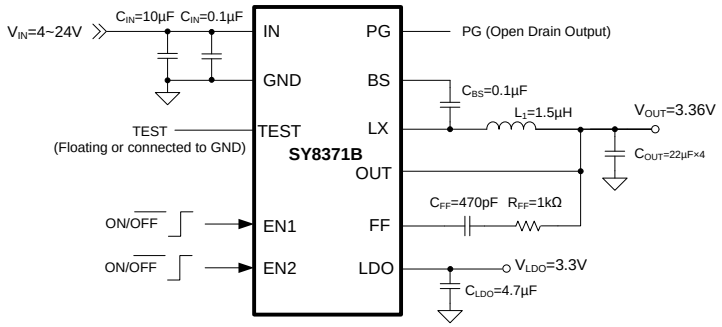


Figure1. Schematic Diagram

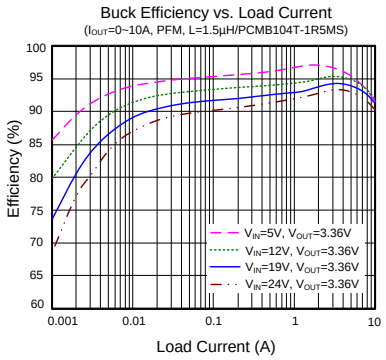
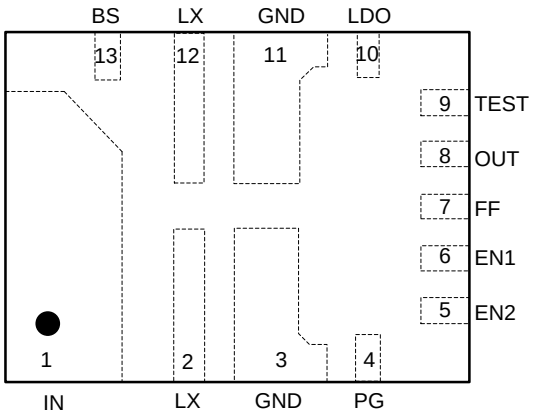


Figure2. Buck Efficiency vs. Load Current

Pinout (top view)



(QFN3×4-13)

Top Mark: **DFA*xyz*** (Device code: DFA, ***x=year code, y=week code, z= lot number code***)

Pin Name	Pin Number	Pin Description
IN	1	Input pin. Decouple this pin to GND pin with at least a 10μF ceramic capacitor. A 0.1μF input ceramic capacitor is recommended to reduce the input noise.
LX	2, 12	Inductor pin. Connect this pin to the switching node of inductor.
GND	3, 11	Ground pin.
PG	4	PG is an open-drain output pin. This pin is externally pulled high when the output voltage is within 90% to 120% of regulation voltage range. Otherwise, this pin is internally pulled low.
EN2	5	Enable control of the IC and internal LDO. Pull this pin high to turn on the IC and internal LDO. Do not leave this pin floating.
EN1	6	Enable control of the DC/DC regulator. Pull this pin high to turn on the regulator. Do not leave this pin floating. The pin is also used for controlling operation mode of the regulator under light load condition after the output of Buck regulator is within the regulation range. When its voltage is less than 1.6V, the Buck regulator works under ultra-sonic mode. When its voltage is larger than 2.2V, the Buck regulator works under PFM mode.
FF	7	Output feed forward pin. Connect RC network from the output to this pin.
OUT	8	Output pin. Connect to the output of DC/DC regulator. The pin also provides the bypass input for internal LDO.
TEST	9	For factory use only. Leave this pin floating or connect it to GND in application.
LDO	10	3.3V LDO output. Decouple this pin to ground with at least a 4.7μF capacitor.
BS	13	Boot-strap pin. Supply high side gate driver. Connect a 0.1μF ceramic capacitor between the BS pin and the LX pin.

Block Diagram

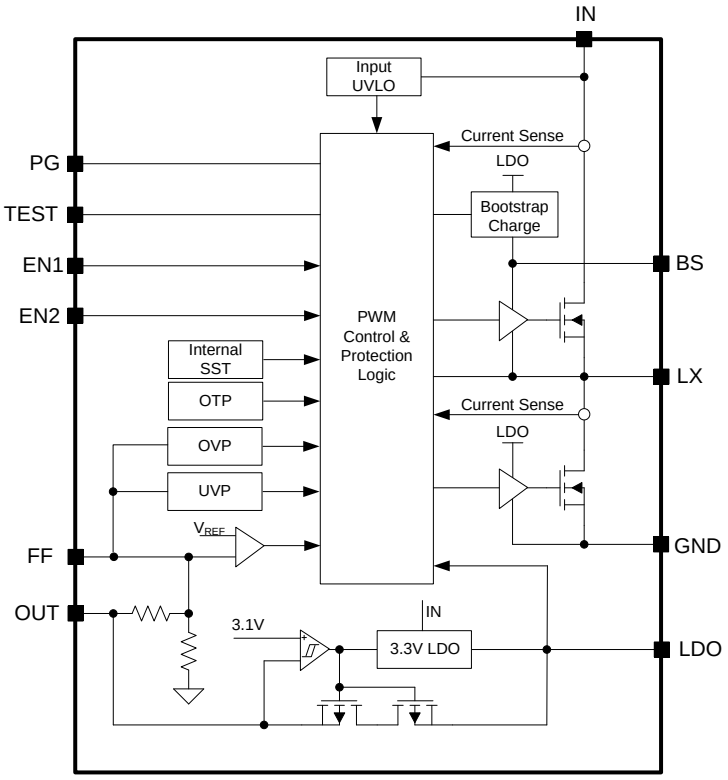


Figure3. Block Diagram

Absolute Maximum Ratings (Note 1)

Supply Input Voltage ---------- -0.3V to 28V
IN-LX, LX, PG, EN1, EN2 Voltage---------- -0.3V to 26V
BS-LX, FF, TEST Voltage---------- -0.3V to 4V
OUT, LDO Voltage---------- -0.3V to 4.5V
Maximum Power Dissipation, $P_{D,MAX}$ @ T_A = 25°C QFN3×4-13 ---------- 3.7W
Package Thermal Resistance (Note 2)
θ_{JA}, QFN3×4-13 ---------- 27°C/W
θ_{JC}, QFN3×4-13 ---------- 4.3°C/W
Junction Temperature Range ---------- -40°C to 150°C
Lead Temperature (Soldering, 10 sec.) ---------- 260°C
Storage Temperature Range ---------- -65°C to 150°C
Dynamic LX Voltage in 10ns Duration ---------- -5V to 29V
Dynamic LX Voltage in 20ns Duration ---------- -1V to 28V

Recommended Operating Conditions (Note 3)

Supply Input Voltage ---------- 4V to 24V
Junction Temperature Range ---------- -40°C to 125°C
Ambient Temperature Range ---------- -40°C to 85°C

Electrical Characteristics

(V_{IN}= 12V, C_{OUT} = 88µF, T_A= 25°C, I_{OUT} = 1A, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Input Voltage Range	V_{IN}		4		24	V
Input UVLO Threshold	V_{UVLO}	V_{IN} rising			3.9	V
Input UVLO Hysteresis	V_{HYS}			0.5		V
Quiescent Current	I_Q	I_{OUT}=0A, V_{OUT}=V_{SET}×105%		85	110	µA
Shutdown Current 1	I_{SHDN1}	EN1=0, EN2=1		65	90	µA
Shutdown Current 2	I_{SHDN2}	EN1=0, EN2=0		4	9	µA
Output Voltage Set-point	V_{SET}	CCM	3.31	3.36	3.41	V
Top FET $R_{DS(ON)}$	$R_{DS(ON)1}$			18		mΩ
Bottom FET $R_{DS(ON)}$	$R_{DS(ON)2}$			8		mΩ
Output Discharge Current	I_{DIS}	V_{OUT}=3.36V		90		mA
Top FET Current Limit	$I_{LMT,TOP}$			20		A
Bottom FET Current Limit	$I_{LMT,BOT}$		13			A
Bottom FET Reverse Current Limit	$I_{LMT,RVS}$	USM	3	5		A
Soft-start Time	t_{SS}	V_{OUT} from 0% to 100% V_{SET}		1.2		ms
EN2/EN1 Input Voltage High	$V_{EN,H}$		1			V
EN2/EN1 Input Voltage Low	$V_{EN,L}$				0.4	V
EN1 Voltage for Ultra-sonic Mode	$V_{EN1,USM}$		1		1.6	V
EN1 Voltage for PFM Mode	$V_{EN1,PFM}$		2.2		V_{IN}	V
Switching Frequency	f_{SW}	CCM	510	600	690	kHz
Ultra-sonic Mode Frequency	f_{USM}	USM mode, I_{OUT}=0A		27		kHz
Min ON Time	$t_{ON,MIN}$	V_{IN}=$V_{IN,MAX}$ (Note4)		50		ns
Min OFF Time	$t_{OFF,MIN}$			150		ns
Output Over Voltage Threshold	V_{OVP}	V_{FF} rising	117	120	123	%V_{REF}
Output Over Voltage Hysteresis	$V_{OVP,HYS}$			5		%V_{REF}
Output OVP Delay	$t_{OVP,DLY}$	(Note4)	20	30		µs
Output Under Voltage Protection Threshold	V_{UVP}		55	60	65	%V_{REF}
Output UVP Delay	$t_{UVP,DLY}$	(Note4)		200		µs
Power Good Threshold	V_{PG}	V_{FF} falling (not good)	80	83	86	%V_{REF}
Power Good Hysteresis	$V_{PG,HYS}$	V_{FF} rising (good)		7		%V_{REF}
Power Good Delay	$t_{PG,R}$	Low to high (Note4)		200		µs
	$t_{PG,F}$	High to low (Note4)		30		µs
Power Good Low Voltage	$V_{PG,LOW}$	Sink 5mA to PG pin, V_{FF}=0V			0.45	V
Power Good Leakage Current	$I_{PG,LKG}$	V_{PG}=3.3V			5	µA
LDO Output Voltage	V_{LDO}	BYP off, I_{LDO}=1mA	3.15	3.3	3.45	V
LDO Dropout Voltage	$V_{DROPOUT}$			300		mV
LDO Output Current Limit	$I_{LMT,LDO}$		150		300	mA
Bypass Switch $R_{DS(ON)}$	$R_{DS(ON),BYP}$			1.5		Ω
Bypass Switch Turn-on Voltage	V_{BYP}		2.97	3.1		V
Bypass Switch Switchover Hysteresis	$V_{BYP,\ HYS}$			0.2		V
Bypass Switch OVP Threshold	$V_{BYP,\ OVP}$	V_{OUT} sweeps	114	120	126	%V_{LDO}

Buck Thermal Shutdown Temperature	$T_{OTP,BUCK}$	T_J rising (Note4)		150		°C
Buck Thermal Shutdown Temperature Hysteresis	$T_{BUCK,HYS}$	T_J falling (Note4)		15		°C
LDO Thermal Shutdown Temperature	$T_{OTP,LDO}$	T_J rising (Note4)		160		°C
LDO Thermal Shutdown Temperature Hysteresis	$T_{LDO,HYS}$	T_J falling (Note4)		25		°C

Note 1: Stresses beyond the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: Package thermal resistance is measured in the natural convection at T_A = 25°C on a 8.5cm×8.5cm size, four-layer Silergy Evaluation Board with 2-oz copper.

Note 3: The device is not guaranteed to function outside its operating conditions.

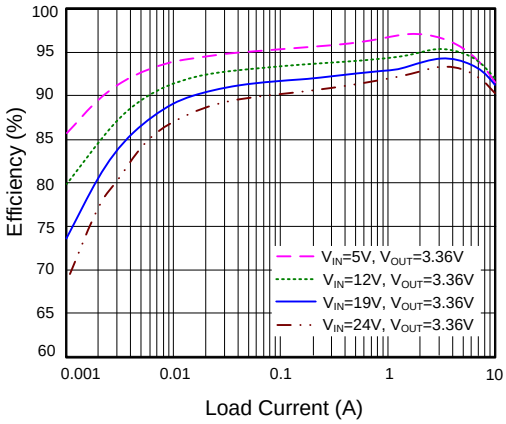
Note 4: Guaranteed by design.

Typical Performance Characteristics

(T_A=25°C, V_{IN}=12V, V_{OUT}=3.36V, L=1.5µH, C_{OUT}=88µF, C_{FF}=470pF, unless otherwise noted)

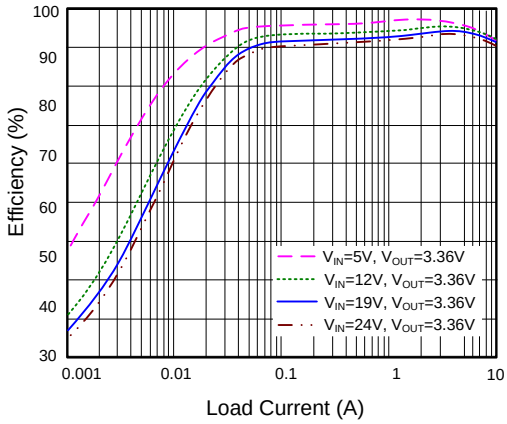
Buck Efficiency vs. Load Current

(I_{OUT}=0~10A, PFM, L=1.5µH/PCMB104T-1R5MS)



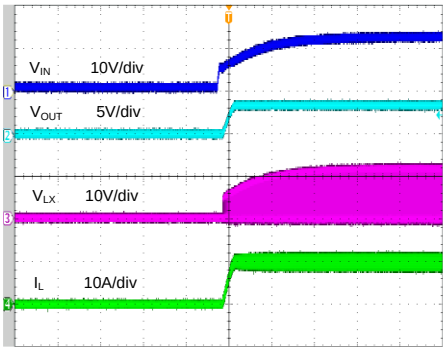
Buck Efficiency vs. Load Current

(I_{OUT}=0~10A, USM, L=1.5µH/PCMB104T-1R5MS)



Startup from V_{IN}

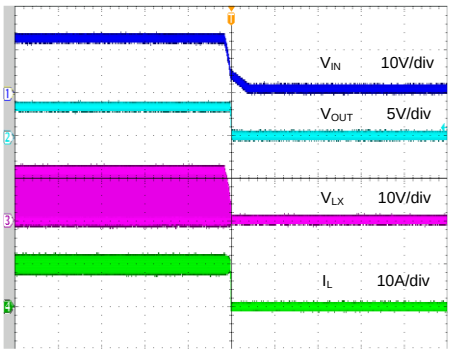
(V_{IN}=12V, V_{OUT}=3.36V, I_{OUT}=10A)



Time (4ms/div)

Shutdown from V_{IN}

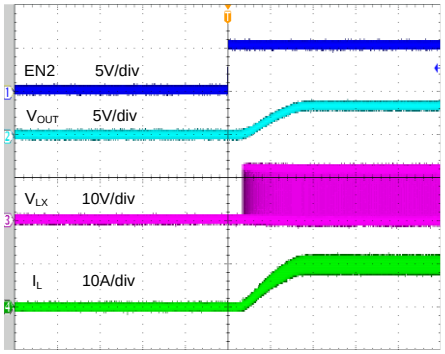
(V_{IN}=12V, V_{OUT}=3.36V, I_{OUT}=10A)



Time (4ms/div)

Startup from EN2

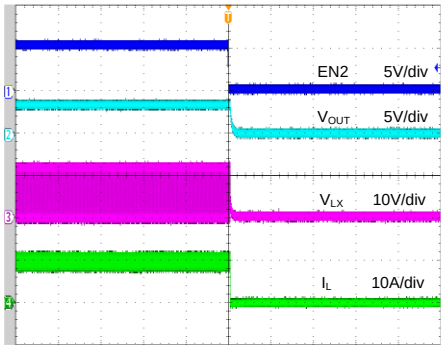
(V_{IN}=12V, V_{OUT}=3.36V, I_{OUT}=10A)



Time (800µs/div)

Shutdown from EN2

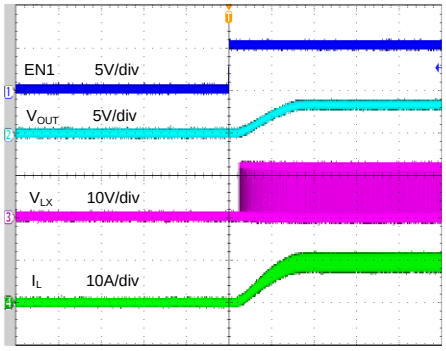
(V_{IN}=12V, V_{OUT}=3.36V, I_{OUT}=10A)



Time (800µs/div)

Startup from EN1

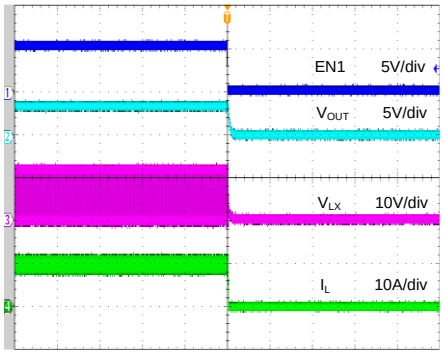
(V_{IN}=12V, V_{OUT}=3.36V, I_{OUT}=10A)



Time (800µs/div)

Shutdown from EN1

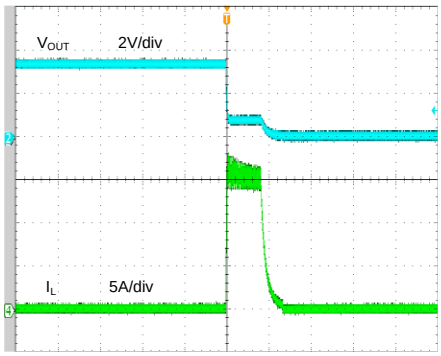
(V_{IN}=12V, V_{OUT}=3.36V, I_{OUT}=10A)



Time (800µs/div)

Output Short Circuit Protection

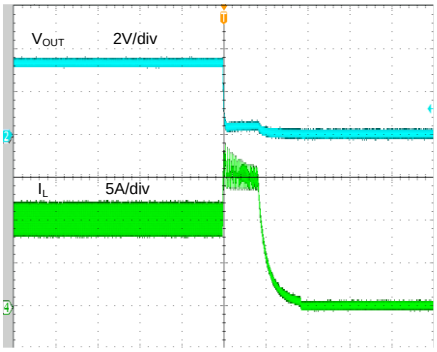
(V_{IN}=12V, V_{OUT}=3.36V, I_{OUT}=0A~Short)



Time (200µs/div)

Output Short Circuit Protection

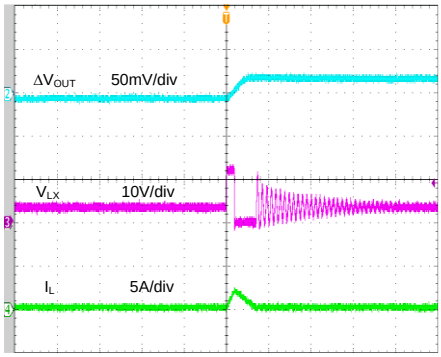
(V_{IN}=12V, V_{OUT}=3.36V, I_{OUT}=10A~Short)



Time (200µs/div)

Output Ripple

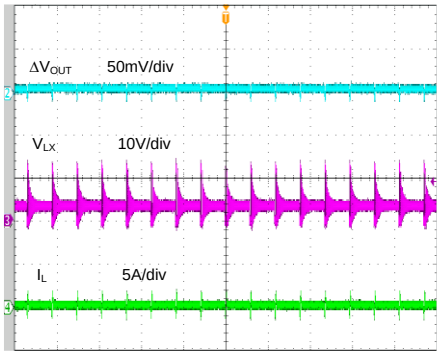
(V_{IN}=12V, V_{OUT}=3.36V, I_{OUT}=0A, PFM)



Time (2µs/div)

Output Ripple

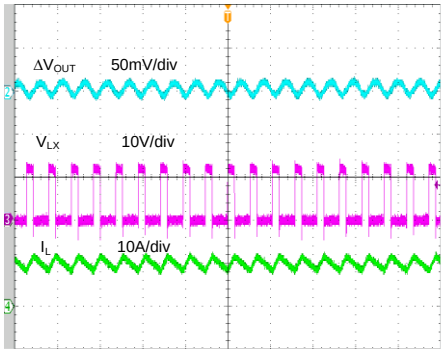
(V_{IN}=12V, V_{OUT}=3.36V, I_{OUT}=0A, USM)



Time (40µs/div)

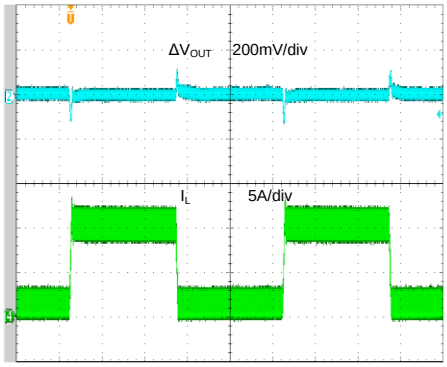
Output Ripple

(V_{IN}=12V, V_{OUT}=3.36V, I_{OUT}=10A)



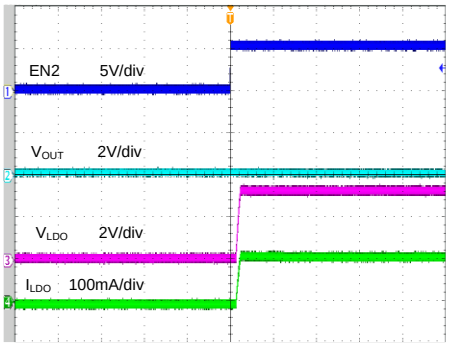
Load Transient

(V_{IN}=12V, V_{OUT}=3.36V, I_{OUT}=1~10A)



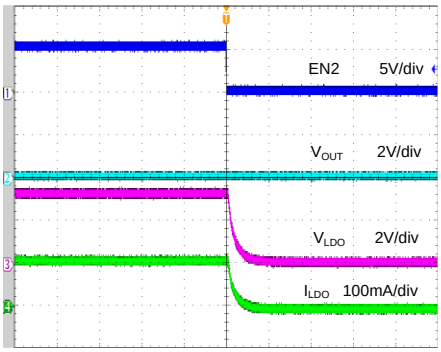
LDO Startup from EN2

(V_{IN}=12V, I_{LDO}=100mA, EN1=0)



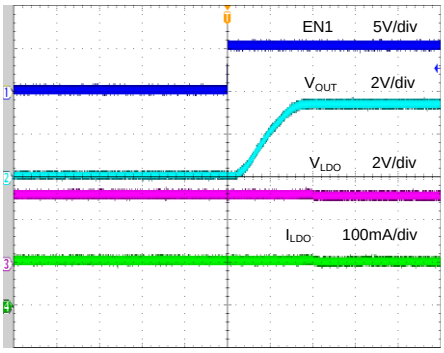
LDO Shutdown from EN2

(V_{IN}=12V, I_{LDO}=100mA, EN1=0)



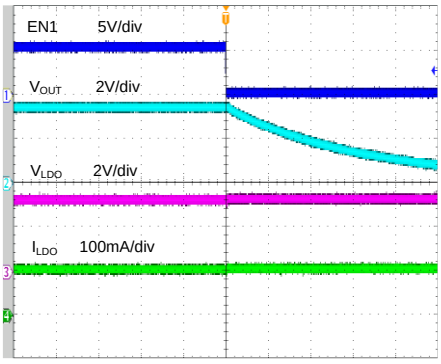
LDO Switchover When EN1 On

(V_{IN}=12V, V_{OUT}=3.36V, I_{OUT}=10A, I_{LDO}=100mA, EN2=1)

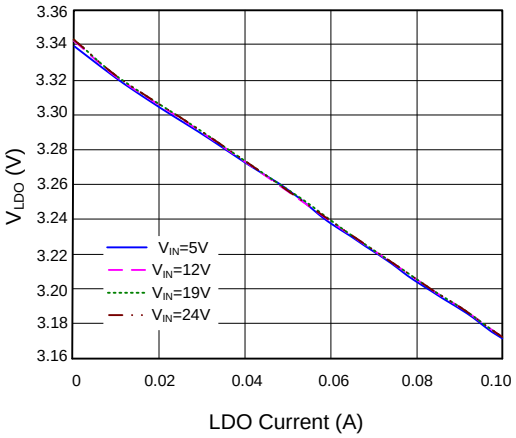


LDO Switchover When EN1 Off

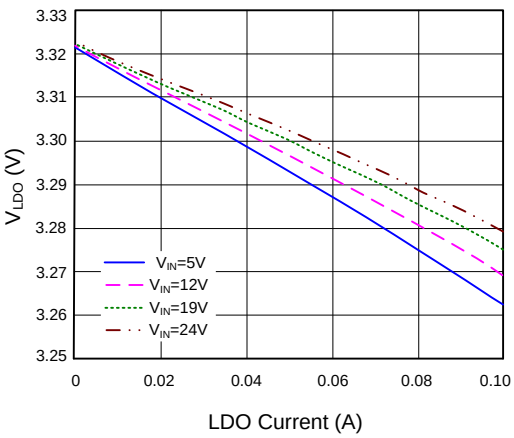
(V_{IN}=12V, V_{OUT}=3.36V, I_{OUT}=10A, I_{LDO}=100mA, EN2=1)



LDO Load Regulation (BYP ON)



LDO Load Regulation (BYP OFF)



Detailed Description

General Features

Constant-on-time Architecture

Fundamental to any constant-on-time (COT) architecture is the one-shot circuit or on-time generator, which determines how long to turn on the high-side power switch. Each on-time (t_{ON}) is a "fixed" period internally calculated to operate the step down regulator at the desired switching frequency considering the input and output voltage ration, $t_{ON}=(V_{OUT}/V_{IN})\times(1/f_{SW})$. For example, considering that a hypothetical converter targets 3.36V output from a 12V input at 600kHz, the target on-time is (3.36V/12V)×(1/600kHz) = 467ns. Each t_{ON} pulse is triggered by the feedback comparator when the output voltage as measured at FF drops below the target value. After one t_{ON} period, a minimum off-time ($t_{OFF,MIN}$) is imposed before any further switching is initiated, even if the output voltage is less than the target. This approach avoids the making any switching decisions during the noisy periods just after switching events and while the switching node (LX) is rapidly rising or falling.

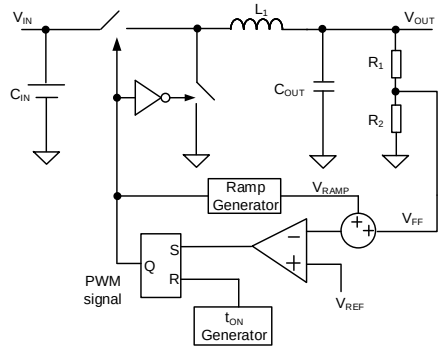
In a COT architecture, there is no fixed clock, so the high-side power switch can turn on almost immediately after a load transient and subsequent switching pulses can be quickly initiated, ramping the inductor current up to meet load requirements with minimal delays. Traditional current mode or voltage mode control methods must simultaneously monitor the feedback voltage, current feedback and internal ramps and compensation signals to determine when to turn off the high-side power switch and turn on the low-side synchronous rectifier. Considering these small signals in a switching environment are difficult to be noise-free after switching large currents, making those architectures difficult to apply in noisy environments and at low duty cycles.

Minimum Duty Cycle and Maximum Duty Cycle

In the COT architecture, there is no limitation for small duty cycle, since at very low duty cycle operation, once the on-time is close to the minimum on time, the switching frequency can be reduced as needed to always ensure a proper operation.

Under T_J=-40℃~125℃ condition, the device can support 3.36V fixed output even the input voltage is as low as 4V.

Instant-PWM Operation



Silergy's instant-PWM control method adds several proprietary improvements to the traditional COT architecture. Whereas most legacy based on COT implementations require a dedicated connection to the output voltage terminal to calculate the t_{ON} duration, instant-PWM control method derives this signal internally. Another improvement optimizes operation with low ESR ceramic output capacitors. In many applications it is desirable to utilize very low ESR ceramic output capacitors, but legacy COT regulators may become unstable in these cases because the beneficial ramp signal that results from the inductor current flowing into the output capacitor maybe become too small to maintain smooth operation. For this reason, instant-PWM synthesizes a virtual replica of this signal internally. This internal virtual ramp and the feedback voltage are combined and compared to the reference voltage. When the sum is lower than the reference voltage, the t_{ON} pulse is triggered as long as the minimum t_{OFF} has been satisfied and the inductor current as measured in the low-side synchronous rectifier is lower than the bottom FET current limit. As the t_{ON} pulse is triggered, the low-side synchronous rectifier turns off and the high-side power switch turns on. Then the inductor current ramps up linearly during the t_{ON} period. At the conclusion of the t_{ON} period, the high-side power switch turns off, the low-side synchronous rectifier turns on and the inductor current ramps down linearly. This action also initiates the minimum t_{OFF} timer to ensure sufficient time for stabilizing any transient conditions and settling the feedback comparator before the next cycle is initiated. This minimum t_{OFF} is relatively short so that during high speed load transient t_{ON} can be retriggered with minimal delay, allowing the inductor current to ramp quickly to provide sufficient energy to the load side.

In order to avoid shoot-through, a dead time (t_{DEAD}) is generated internally between the high-side power

switch off and the low-side synchronous rectifier on period or the low-side synchronous rectifier off and the high-side power switch on period.

Light Load Operation Mode Selection

PFM or USM light load operation is selected by EN1 pin. EN1 is not only Buck enable pin but also mode selection pin to control operation mode of the regulator under light load condition after the output of Buck regulator is within the regulation range. If the voltage on this pin is lower than 1.6V and higher than its rising threshold, the Buck regulator works under ultra-sonic mode (USM). If the voltage on this pin is greater than 2.2V, the Buck regulator works under pulse-frequency modulation mode (PFM).

If PFM light load operation is selected, under light load conditions, typically $I_{OUT} < 1/2 \times \Delta I_L$, the current through the low-side synchronous rectifier will ramp to near zero before the next t_{ON} time. When this occurs, the low-side synchronous rectifier turns off, preventing recirculation current that can seriously reduce efficiency under these light load conditions. As load current is further reduced, and the combined feedback and ramp signals remain much greater than the reference voltage, the instant-PWM control loop will not trigger another t_{ON} until needed, so the apparent operating switching frequency will correspondingly drop, further enhancing efficiency. The switching frequency can be lower than audible frequency area under deep light load or null load conditions. Continuous conduction mode (CCM) resumes smoothly as soon as the load current increases sufficiently for the inductor current to remain above zero at the time of the next t_{ON} cycle. The device enters CCM once the load current exceeds the critical level. After that, the switching frequency stays fairly constant over the output current range. The critical level of the load current is determined with

$$I_{OUT\_CTL} = \frac{\Delta I_L}{2} = \frac{V_{OUT} \times (1-D)}{2 \times f_{SW} \times L_1}$$

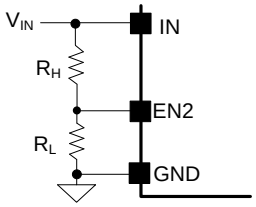
If USM light load operation is selected, it keeps the switching frequency above an audible frequency area even under deep light load or null load conditions. Once the device detects that both the high-side power switch and the low-side synchronous rectifier turn off for more than one certain time, it forces the low-side synchronous rectifier turn on in advance of one t_{ON} cycle and discharge the output capacitor electric quantity so that the switching frequency is out of audio range. There is also one feedback loop to match the low-side synchronous rectifier forced turn on time with the error amplifier output voltage to avoid output voltage becoming too high.

Input Under Voltage Lock-out (UVLO)

To prevent operation before all internal circuitry is ready and to ensure that the power and synchronous rectifier switches can be sufficiently enhanced, the instant-PWM incorporates one input under-voltage lockout protections.

The device remains in a low current state and all switching actions and LDO are inhibited until V_{IN} exceeds its own UVLO (rising) threshold. At that time, if EN2 is enabled, the LDO will be built up, then if EN1 is also enabled, the Buck will start-up by initiating a soft-start ramp. If V_{IN} falls below V_{UVLO} less than the input UVLO hysteresis, switching actions and LDO will again be suppressed.

If the input UVLO threshold is low for some high input UVLO threshold requirement applications, use EN2 to adjust the input UVLO by adopting two external divided resistors.



EN2/EN1 Control

The SY8371B has two enable pins to control the synchronous Buck regulator and LDO.

The Buck regulator and LDO are all turned off under S4/S5 state (EN2 = Low, EN1 = High or Low). Under S3 state (EN2 = High, EN1 = Low), only LDO output is turned on while the Buck regulator is turned off. Under S0 state (EN2 = High, EN1 = High), the Buck regulator and LDO are all turned on. Only if EN2 is high could LDO be turned on, and only if EN1 and EN2 are both high could the Buck regulator be turned on. See EN2/EN1 logic details in below table.

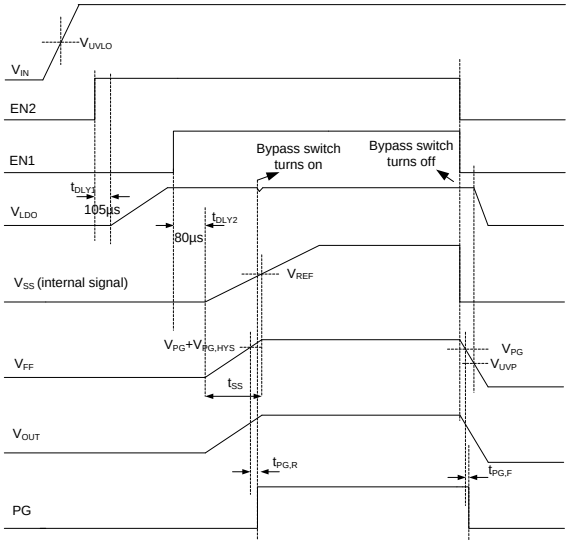
EN2	EN1	STATE	LDO	BUCK
High	High	S0	On	On
High	Low	S3	On	Off
Low	Low/High	S4/S5	Off	Off

The EN2/EN1 input is a high-voltage capable input with logic-compatible threshold. When EN2/EN1 is driven above 1V normal device operation will be enabled. When driven < 0.4V the device will be shut down, reducing the input current to < 10μA.

It is not recommended to connect EN and IN directly. A resistor in a range of 1kΩ to 1MΩ should be used if EN2/EN1 is pulled high by IN.

Startup and Shutdown

The SY8371B incorporates an internal soft-start circuit to smoothly ramp the Buck regulator output to the desired voltage whenever the device is enabled. Internally, the soft-start circuit clamps the output at a low voltage and then allows the output to rise to the desired voltage over approximately 1.2ms, which avoids high current flow and transients during startup. The startup and shutdown sequence are shown below.

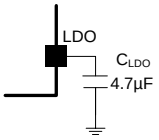


After V_{IN} exceeds its own UVLO (rising) threshold, the internal LDO regulator works and LDO is turned on after one delay time t_{DLY1} if EN2 is enabled, the Buck regulator is turned on after one delay time t_{DLY2} if EN1 is also enabled. When the output voltage is 90% of the regulation point, PG is high-impedance after one delay time $t_{PG,R}$, and at the same time, LDO output switches over to the Buck output if OUT voltage is higher than bypass switch turn-on voltage. LDO output will switch over to internal LDO regulator once either EN2 or EN1 is disabled.

If the output is pre-biased to a certain voltage before start-up, the device disables the switching of both the high-side power switch and the low-side synchronous rectifier until the voltage on the internal reference exceeds the sensed output voltage at the FF node.

LDO Output

SY8371B integrates one high performance, low drop-out linear regulator and this LDO output voltage is fixed 3.3V, which can not only power the internal gate drivers, PWM logic, analog circuitry and other blocks, but also power the external peripheries with 100mA capability. This LDO is intended mainly for an auxiliary 3.3V supply for the notebook system in standby time. Once the input voltage exceeds its own UVLO (rising) threshold, and EN2 is enabled, LDO is turned on and supplied power by V_{IN}. After the EN1 is also enabled, until the output voltage exceeds bypass switch turn-on voltage and at the same time PG becomes high-impedance, the internal LDO regulator will be turned off and the bypass switch will be turned on so that LDO output switch over to V_{OUT} to reduce power consumption. Connect a 4.7µF low ESR ceramic capacitor from LDO to GND.



Output Discharge

SY8371B discharges the output voltage when the converter shuts down from V_{IN} or EN2/EN1, or thermal shutdown, so that output voltage can be discharged in a minimal time, even load current is zero. The discharge FET in parallel with the low-side synchronous rectifier turns on after the low-side synchronous rectifier turns off when shut down logic is triggered. The output discharge current is typically 90mA. Note that the discharge FET is not active beyond these shutdown conditions.

Buck Output Power Good Indicator

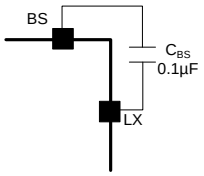
The Buck power good indicator is an open drain output controlled by a window comparator connected to the feedback signal. If V_{FF} is greater than $V_{PG}+V_{PG,HYS}$ and less than V_{OVP} for at least the power good delay time (low to high), PG will be high-impedance.

PG should be connected to V_{IN} or another voltage source through a resistor (e.g. 100kΩ). After V_{IN} exceeds its own UVLO (rising) threshold, the PG FET is turned on so that PG is pulled to GND before output voltage is ready. After feedback voltage V_{FF} reaches $V_{PG}+V_{PG,HYS}$, PG is pulled high (after one delay time typical 200µs). When V_{FF} drops to V_{PG}, or rises to V_{OVP} for one OVP delay time, PG is pulled low (after one delay time typical 30µs).

External Bootstrap Capacitor Connection

This device integrates a floating power supply for the gate driver that operates the high-side power switch. Proper operation requires a 0.1µF low ESR ceramic capacitor to be connected between BS and LX. This bootstrap capacitor provides the gate driver supply

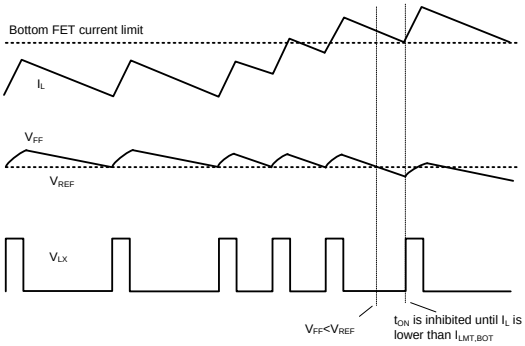
voltage for the high-side N-channel MOSFET power switch.



Fault Protection Modes

Buck Output Current Limit

Instant-PWM incorporates a cycle-by-cycle "valley" current limit. Inductor current is measured in the low-side synchronous rectifier when it turns on and as the inductor current ramps down. If the current exceeds the bottom FET current limit threshold, t_{ON} is inhibited until the current returns back to the limit threshold or lower.



When the valley current limit occurs, the output current limit value is $I_{LMT,OUT}=I_{LMT,BOT}+\Delta I_L/2$,

$$\Delta I_L = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times f_{SW} \times L_1}$$

The over current limit protection limits the inductor current but the OCP itself is one non-latch protection. When the load current is higher than the bottom FET current limit threshold by one half of the peak-to-peak inductor ripple current, the output voltage starts to drop. Once the feedback voltage falls lower than the under voltage protection (UVP) threshold and continues for one UVP delay time, the device will UVP latch off. On the other hand, over temperature protection may also be triggered under an over current condition and the device will OTP latch off.

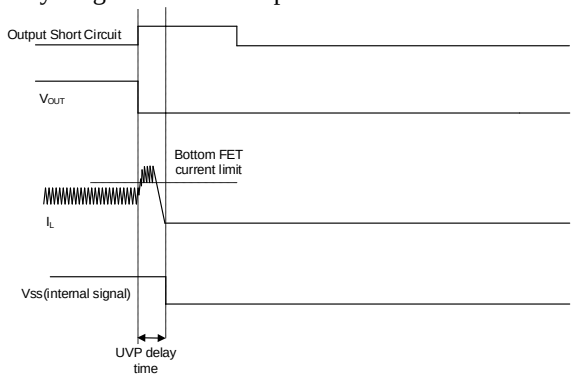
The device also features cycle-by-cycle "peak" current limit (top FET current limit). During t_{ON} time, the high-side power switch current is monitored. If the monitored current exceeds the top FET current limit, the high-side power switch is turned off, the low-side synchronous rectifier is turned on and then t_{ON} is inhibited. t_{ON} can be not inhibited any more once low-side synchronous rectifier current is lower than the bottom FET current limit value.

LDO Output Current Limit

The device features LDO current limit to guarantee LDO safe operation in all operating conditions. Once the LDO output voltage is less than its regular value after LDO is enabled, the internal LDO regulator or bypass switch will work under current limit condition until the LDO output voltage is within its regular range. For example, when the LDO output short circuit occurs, the LDO will work in a current limited way. LDO output voltage can recover after the short circuit condition is removed.

Buck Output Under Voltage Protection (UVP)

If V_{OUT} < ~60% of the set point for approximately 200μs occurring when the output short circuit or the load current is heavier than the maximum current capacity, the output under voltage protection (UVP) will be triggered, and the device will latch off. Recycling EN2 or EN1 input to re-enable the device.



Buck Output Over Voltage Protection (OVP)

This device includes Buck output over voltage protection (OVP). If the feedback voltage rises above the reference voltage level, the high-side power switch naturally remains off and different actions are adopted in different operation mode.

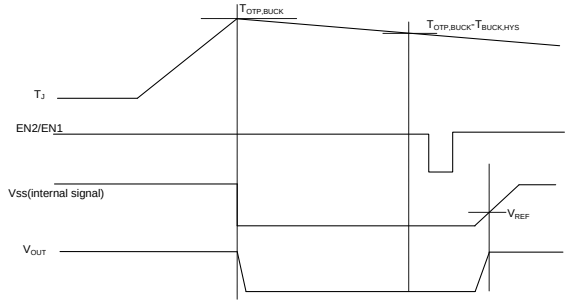
When operating in PFM light load mode, if the feedback voltage remains high, the low-side synchronous rectifier remains on until the inductor current reaches zero and the switching actions are suppressed. If the feedback voltage doesn't exceed over voltage protection threshold, the switching actions will be recovered once the combined feedback and ramp signals become lower than the reference voltage. If the feedback voltage exceeds over voltage protection threshold and lingers for one OVP delay time, and the output voltage exceeds bypass switch OVP voltage, the output over voltage protection (OVP) will be triggered, and the device

will latch off. Recycling EN2 or EN1 input to re-enable the device.

When operating in USM light load mode, if the feedback voltage remains high, the low-side synchronous rectifier forced turn on time will be longer and inductor current average value becomes more and more negative until the reverse current limit is triggered, trying to make output voltage lower. If the feedback voltage exceeds the over voltage protection threshold and lingers for one OVP delay time, and the output voltage exceeds bypass switch OVP voltage, the output over voltage protection (OVP) will be triggered, and the device will latch off. Recycling EN2 or EN1 input to re-enable the device. False OVP may happen under USM light load condition if the inductance is chosen too small and reverse current limit is triggered.

Buck Over Temperature Protection (OTP)

Instant-PWM includes Buck over temperature protection (OTP) circuitry to prevent overheating due to excessive power dissipation. When the Buck thermal sensor detects the Buck junction temperature exceeds 150°C, the over temperature protection (OTP) will be triggered, and the device will latch off (LDO output voltage is still alive). Recycling EN2 or EN1 input to re-enable the device after the junction temperature cools down about 15°C.



LDO Over Temperature Protection

The device also features auto-recovery mode LDO over temperature protection to guarantee LDO safe operation when the internal LDO regulator power loss is great. Once the LDO thermal sensor detects that LDO junction temperature exceeds 160°C, the LDO will be turned off. When the LDO junction temperature cools down by approximately 25°C, the LDO will be recovered again and Buck output will also be recovered as experiencing once EN2 input re-enabling.

Design Procedure

Buck Inductor Selection

The inductor is necessary to supply constant current to the output load while being driven by the switched input voltage.

Instant-PWM operates well over a wide range of inductor values. This flexibility allows for optimization to find the best trade-off of efficiency, cost and size for a particular application. Selecting a low inductor value will help reduce size and cost and enhance transient response, but will increase peak inductor ripple current, reducing efficiency and increasing output voltage ripple. The low DC resistance (DCR) of these low value inductors may help reduce DC losses and increase efficiency. On the other hand, higher inductor values tend to have higher DCR and will slow transient response.

A reasonable compromise between size, efficiency, and transient response can be determined by selecting a ripple current (ΔI_L) about 20% ~ 50% of the desired full output load current. Start calculating the approximate inductor value by selecting the input and output voltages, the operating frequency (f_{SW}), the maximum output current ($I_{OUT,MAX}$) and estimating a ΔI_L as some percentage of that current.

$$L_1 = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times f_{SW} \times \Delta I_L}$$

Use this inductance value to determine the actual inductor ripple current (ΔI_L) and required peak current inductor current $I_{L,PEAK}$.

$$\Delta I_L = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times f_{SW} \times L_1}$$

And $I_{L,PEAK} = I_{OUT,MAX} + \Delta I_L/2$

Select an inductor with a saturation current and thermal rating in excess of $I_{L,PEAK}$.

If USM light load operation is selected, make sure the inductor value is high enough to avoid reverse current limit is been triggered just under steady state if the load current is zero.

For highest efficiency, select an inductor with a low DCR that meets the inductance, size and cost targets. Low loss ferrite materials should be considered.

Buck Inductor Design Example

Consider a typical design for a device providing $3.36V_{OUT}$ at 10A from $12V_{IN}$, operating at 600kHz and using target inductor ripple current (ΔI_L) of 40% or 4A. Determine the approximate inductance value at first:

$$L_1 = \frac{3.36V \times (12V - 3.36V)}{12V \times 600kHz \times 4A} = 1\mu H$$

Next, select the nearest standard inductance value, in this case 1.5µH, and calculate the resulting inductor ripple current (ΔI_L):

$$\Delta I_L = \frac{3.36V \times (12V - 3.36V)}{12V \times 600kHz \times 1.5\mu H} = 2.69A$$

$I_{L,PEAK}$ = 10A + 2.69A/2 = 11.345A

The resulting 2.69A ripple current is 2.69A/10A is 26.9%, well within the 20% ~ 50% target.

$I_{L,PEAK,RVS}$ = 2.69A/2 = 1.345A < $I_{LIM,RVS}$

Finally, select an available inductor with a saturation current higher than the resulting $I_{L,PEAK}$ of 11.345A.

Buck Input Capacitor Selection

Input filter capacitors are needed to reduce the ripple voltage on the input, to filter the switched current drawn from the input supply and to reduce potential EMI. When selecting an input capacitor, be sure to select a voltage rating at least 20% greater than the maximum voltage of the input supply and a temperature rating above the system requirements. X5R series ceramic capacitors are most often selected due to their small size, low cost, surge current capability and high RMS current ratings over a wide temperature and voltage range. However, systems that are powered by a wall adapter or other long and therefore inductive cabling may be susceptible to significant inductive ringing at the input to the device. In these cases, consider adding some bulk capacitance like electrolytic, tantalum or polymer type capacitors. Using a combination of bulk capacitors (to reduce overshoot or ringing) in parallel with ceramic capacitors (to meet the RMS current requirements) is helpful in these cases.

Consider the RMS current rating of the input capacitor, paralleling additional capacitors if required to meet the calculated RMS ripple current,

$$I_{CIN\_RMS} = I_{OUT} \times \sqrt{D \times (1-D)}$$

The worst-case condition occurs at D = 0.5, then

$$I_{CIN\_RMS,MAX} = \frac{I_{OUT}}{2}$$

For simplification, choose an input capacitor with an RMS current rating greater than half of the maximum load current.

On the other hand, the input capacitor value determines the input voltage ripple of the converter. If there is an input voltage ripple requirement in the system, choose an appropriate input capacitor that meets the specification.

Given the very low ESR and ESL of ceramic capacitors, the input voltage ripple can be estimated by

$$V_{CIN\_RIPPLE,CAP} = \frac{I_{OUT}}{f_{SW} \times C_{IN}} \times D \times (1\text{-}D)$$

The worst-case condition occurs at D = 0.5, then

$$V_{CIN\_RIPPLE,CAP,MAX} = \frac{I_{OUT}}{4 \times f_{SW} \times C_{IN}}$$

The capacitance value is less important than the RMS current rating. In most applications a single 10µF X5R capacitor is sufficient. Take care to locate the ceramic input capacitor as close to the device IN and GND pin as possible.

Buck Output Capacitor Selection

Instant-PWM provides excellent performance with a wide variety of output capacitor types. Ceramic and POS types are most often selected due to their small size and low cost. Total capacitance is determined by the transient response and output voltage ripple requirements of the system.

Buck Output Ripple

Output voltage ripple at the switching frequency is caused by the inductor current ripple (ΔI_L) on the output capacitors ESR (ESR ripple) as well as the stored charge (capacitive ripple). When considering total ripple, both should be considered.

$$V_{RIPPLE,ESR} = \Delta I_L \times ESR$$

$$V_{RIPPLE,CAP} = \frac{\Delta I_L}{8 \times C_{OUT} \times f_{SW}}$$

Consider a typical application with ΔI_L = 2.69A using four 22µF ceramic capacitors, each with an ESR of ~6mΩ for parallel total of 88µF and 1.5mΩ ESR.

$$V_{RIPPLE,ESR} = 2.69A \times 1.5m\Omega = 4.04mV$$

$$V_{RIPPLE,CAP} = \frac{2.69A}{8 \times 88\mu F \times 600kHz} = 6.37mV$$

Total ripple = 10.41mV. The actual capacitive ripple may be higher than calculated value because the capacitance decreases with the voltage on the capacitor.

Using a 150µF 40mΩ POS cap, the above result is

$$V_{RIPPLE,ESR} = 2.69A \times 40m\Omega = 107.6mV$$

$$V_{RIPPLE,CAP} = \frac{2.69A}{8 \times 150\mu F \times 600kHz} = 3.74mV$$

Total ripple = 111.34mV

Buck Output Transient Undershoot/Overshoot

If very fast load transient must be supported, consider the effect of the output capacitor on the output transient undershoot and overshoot. Instant-PWM responds quickly to changing load conditions, however, some considerations must be needed, especially when using small ceramic capacitors which have low capacitance at low output voltages which results in insufficient stored energy for load transient. Output transient undershoot and overshoot

have two causes: voltage changes caused by the ESR of the output capacitor and voltage changes caused by the output capacitance and inductor current slew rate.

ESR undershoot or overshoot may be calculated as $V_{ESR} = \Delta I_{OUT} \times ESR$. Using the ceramic capacitor example above and a fast load transient of ± 5A, V_{ESR} = ±5A × 1.5mΩ = ±7.5mV. The POS capacitor result with the same load transient, V_{ESR} = ± 5A × 40mΩ = ±200mV.

Capacitive undershoot (load increasing) is a function of the output capacitance, the load step, the inductor value and the input-output voltage difference and the maximum duty factor. During a fast load transient, the maximum duty factor of instant-PWM is a function of t_{ON} and the minimum t_{OFF} as the control scheme is designed to rapidly ramp the inductor current by grouping together many t_{ON} pulses in this case. The maximum duty factor D_{MAX} may be calculated by

$$D_{MAX} = \frac{t_{ON}}{t_{ON} + t_{OFF,MIN}}$$

Given this, the capacitive undershoot may be calculated by

$$V_{UNDERSHOOT,CAP} = -\frac{L_1 \times \Delta I_{OUT}^2}{2 \times C_{OUT} \times (V_{IN,MIN} \times D_{MAX} - V_{OUT})}$$

Consider a 5A load increase using the ceramic capacitor case when V_{IN} = 12V. At V_{OUT} = 3.36V, the result is t_{ON} = 467ns, $t_{OFF,MIN}$ = 150ns, D_{MAX} = 467 / (467 + 150) = 0.757 and

$$V_{UNDERSHOOT,CAP} = -\frac{1.5\mu H \times (5A)^2}{2 \times 88\mu F \times (12V \times 0.757 - 3.36V)} = -37.22mV$$

Using the POS capacitor case, the above result is

$$V_{UNDERSHOOT,CAP} = -\frac{1.5\mu H \times (5A)^2}{2 \times 150\mu F \times (12V \times 0.757 - 3.36V)} = -21.84mV$$

Capacitive overshoot (load decreasing) is a function of the output capacitance, the inductor value and the output voltage.

$$V_{OVERSHOOT,CAP} = \frac{L_1 \times \Delta I_{OUT}^2}{2 \times C_{OUT} \times V_{OUT}}$$

Consider a 5A load decrease using the ceramic capacitor case above. At V_{OUT} =3.36V the result is

$$V_{OVERSHOOT,CAP} = \frac{1.5\mu H \times (5A)^2}{2 \times 88\mu F \times 3.36V} = 63.41mV$$

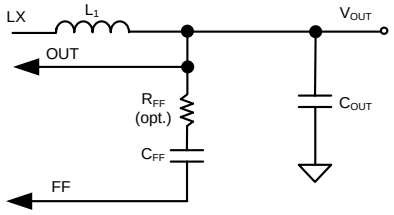
Using the POS capacitor case, the above result is

$$V_{OVERSHOOT,CAP} = \frac{1.5\mu H \times (5A)^2}{2 \times 150\mu F \times 3.36V} = 37.2mV$$

Combine the ESR and capacitive undershoot and overshoot to calculate the total overshoot and undershoot for a given application.

Load Transient Considerations:

The SY8371B adopts the instant PWM architecture to achieve good stability and fast transient responses. In applications with high step load current, adding an RC network R_{FF} and C_{FF} between the OUT pin and the FF pin may further speed up the load transient responses. R_{FF} = 1kΩ and C_{FF} = 220pF have been shown to perform well in most applications. Increase C_{FF} will speed up the load transient response if there is no stability issue.



Note that when C_{OUT} > 500µF and minimum load current is low, set feed-forward values as R_{FF} = 1kΩ and C_{FF} = 2.2nF to provide sufficient ripple to FF for small output ripple and good transient behavior.

Thermal Design Considerations

Maximum power dissipation depends on the thermal resistance of the IC package, the PCB layout, the surrounding airflow, and the difference between the junction and ambient temperatures. The maximum power dissipation may be calculated by:

$P_{D,MAX} = (T_{J,MAX} - T_A) / \theta_{JA}$

Where, $T_{J,MAX}$ is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction to ambient thermal resistance.

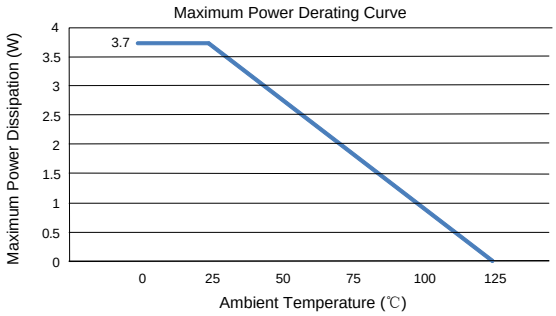
To comply with the recommended operating conditions, the maximum junction temperature is 125°C. The junction to ambient thermal resistance θ_{JA} is layout dependent. For the QFN3×4-13 package the thermal resistance θ_{JA} is 27°C/W when measured on a standard Silergy 8.5cm×8.5cm size four-layer thermal test board. These standard thermal test layouts have a very large area with long 2-oz. copper traces connected to each IC pin and very large, unbroken 1-oz. internal power and ground planes.

Meeting the performance of the standard thermal test board in a typical tiny evaluation board area requires wide copper traces well-connected to the IC's backside pads leading to exposed copper areas on the component side of the board as well as good thermal via from the exposed pad connecting to a wide middle-layer ground plane and, perhaps, to an exposed copper area on the board's solder side.

The maximum power dissipation at T_A=25°C may be calculated by the following formula:

$P_{D,MAX}$ = (125℃ − 25℃) / (27℃/W) = 3.7W

The maximum power dissipation depends on operating ambient temperature for fixed $T_{J,MAX}$ and thermal resistance θ_{JA}. Use the derating curve in figure below to calculate the effect of rising ambient temperature on the maximum power dissipation.



Layout Design

Follow these PCB layout guidelines for optimal performance and thermal dissipation.

Input Capacitors: Place the input capacitor very near IN and GND, minimizing the loop formed by these connections. And the input capacitor should be connected to the IN and GND by wide copper plane. A 0.1μF input ceramic capacitor is recommended to reduce the input noise.

Output Capacitors: Guarantee the C_{OUT} negative sides are connected with GND pin by wide copper traces instead of vias, in order to achieve better accuracy and stability of output voltage.

LDO Capacitor: Place the LDO capacitor close to LDO using short, direct copper trace to one nearest device GND pin (pin 11).

Feedback Network and Output Line: Place the feedback components (R_{FF} and C_{FF}) as close to FF pin as possible. Avoid routing the feedback line near LX, BS or other high frequency signal as it is noise sensitive. Make the feedback sampling point Kelvin connect with C_{OUT} rather than the inductor output terminal. Keep output line width at least 20mil as it is also the 100mA LDO's bypass input.

LX Connection: Keep LX area small to prevent excessive EMI, while providing wide copper traces to minimize parasitic resistance and inductance. Wide LX copper trace between pin 2 and pin 12 should be adopted to improve efficiency.

BS Capacitor: Place the BS capacitor on the same layer as the device, keep the BS voltage path (BS, LX and C_{BS}) as short as possible.

Control Signals: It is not recommended to connect control signals and IN directly. A resistor in a range of 1kΩ to 1MΩ should be used if they are pulled high by IN.

GND Vias: Place adequate number of vias on the GND layer around the device for better thermal performance. The exposed GND pad should be connected by a larger copper area than its size, place four GND vias on it for heat dissipation.

PCB Board: A four-layer layout with 2-oz copper is strongly recommended to achieve better thermal performance. The top layer and bottom layer should place power IN and GND copper plane as wide as possible. Middle1 layer should place all GND layer for conducting heat and shielding middle2 layer signal line from top layer crosstalk. Place signal lines on middle2 layer instead of the other layers, so that the other layers' GND plane not be cut apart by these signal lines.

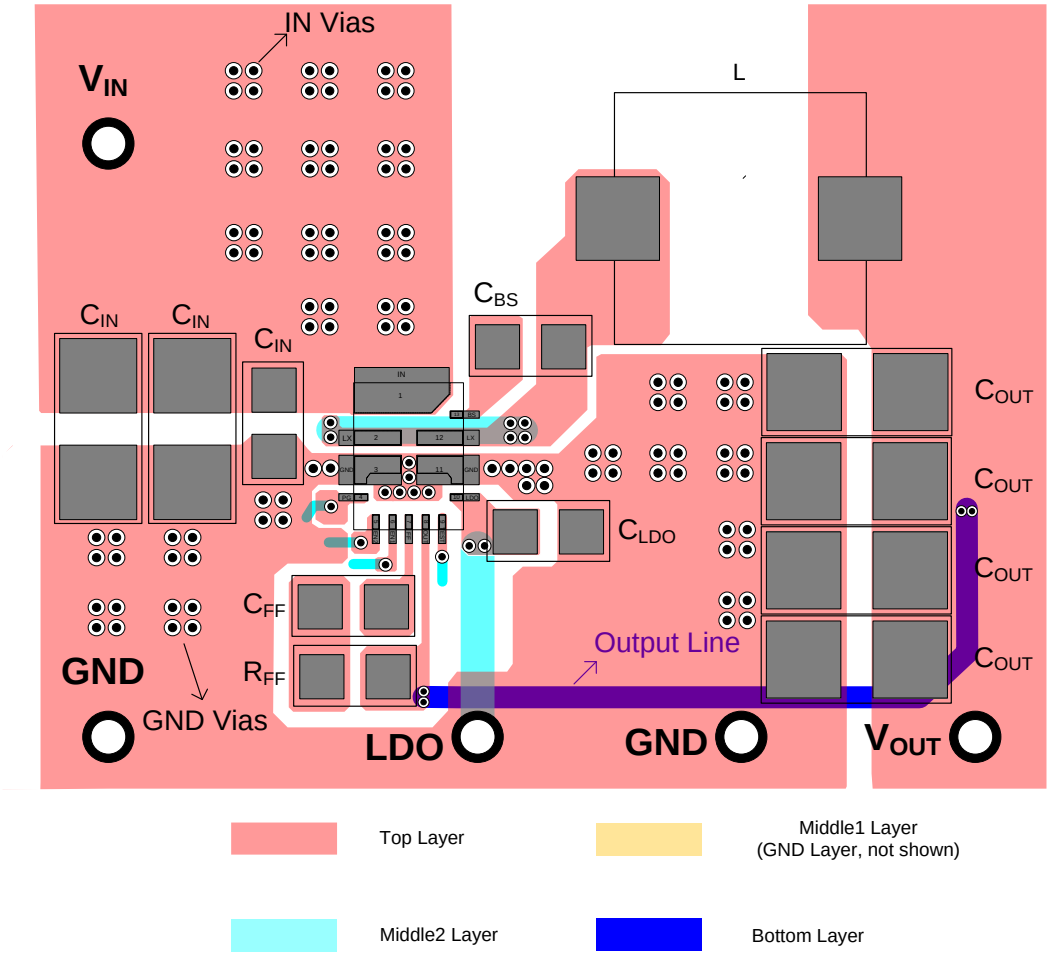
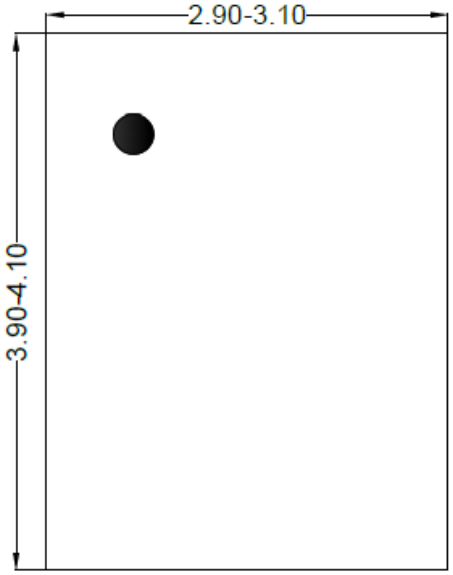
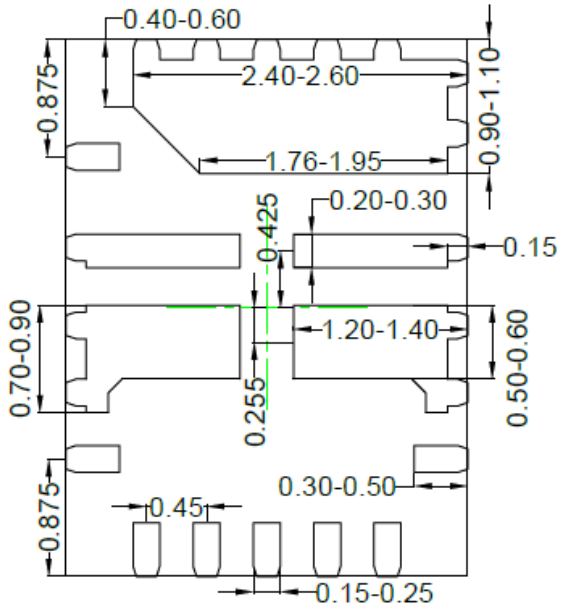


Figure4. PCB Layout Suggestion

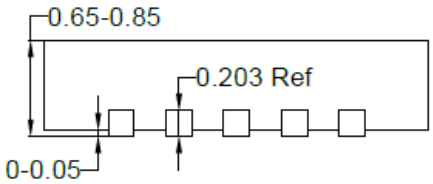
QFN3×4-13 Package Outline Drawing



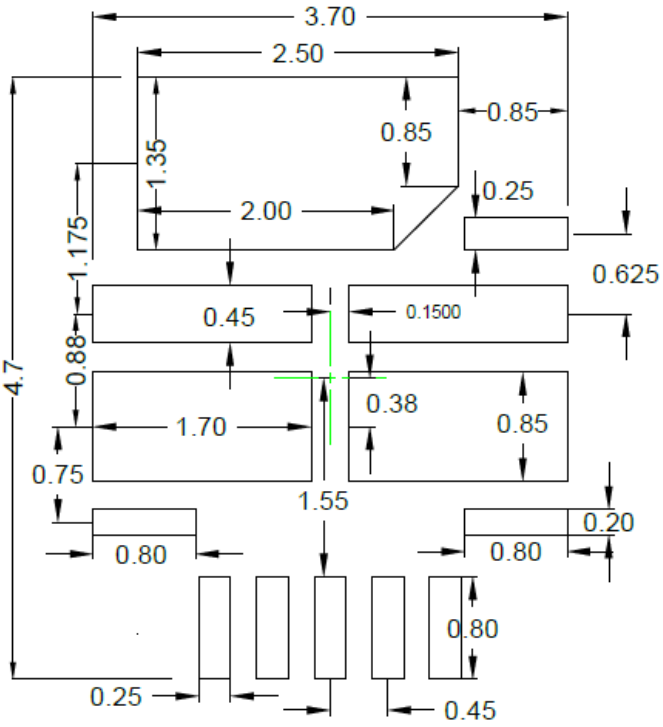
Top View



Bottom View



Front View

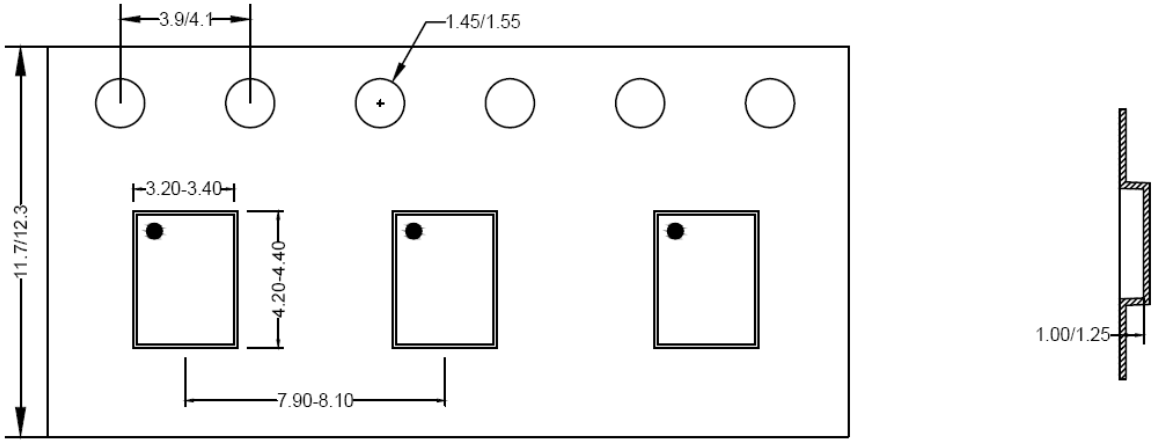


Recommended PCB layout
(Reference only)

Notes: 1, All dimension in millimeter and exclude mold flash & metal burr;
2, center line on drawing refers to the chip body center

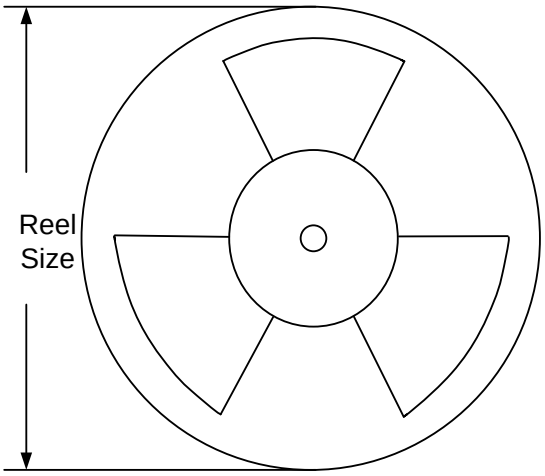
Taping & Reel Specification

1. QFN3×4-13 taping orientation



Feeding direction ⟶

2. Carrier Tape & Reel specification for packages



Package types	Tape width (mm)	Pocket pitch(mm)	Reel size (Inch)	Trailer length(mm)	Leader length (mm)	Qty per reel
QFN3×4	12	8	13”	400	400	5000

3. Others: NA

Revision History

The revision history provided is for informational purpose only and is believed to be accurate, however, not warranted. Please make sure that you have the latest revision.

Date	Revision	Change
Jan.22, 2021	Revision 0.9C	Add “A 0.1μF input ceramic capacitor is recommended to reduce the input noise.” in the pin description and the layout design;
Nov.30, 2020	Revision 0.9B	Update the package Outline Drawing. (page 19)
Nov.05, 2020	Revision 0.9A	Add (IN-LX) voltage in Absolute Maximum Ratings (page 3)
Jul.20, 2020	Revision 0.9	Initial Release

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