SY6862B

2 to 1 Power MUX for USB PD Application

General Description

The SY6862B is a 2 to 1 power MUX switch for USB PD application. The SY6862B integrates two low on resistance power paths: high voltage power path and 5V voltage power path. The high voltage power path is a bi-directional channel. It can be configured as sink port or source port. Both directions have reverse block function.

The SY6862B is integrated CC bypass path. HOST_CCx is isolated to CONN_CCx when dead battery or VCONN is applied. If CONN_CCx is selected as CC line, CONN_CCx can be bypassed to HOST_CCx by I²C control.

SY6862B support USB PD fast role swap. Once detected VBUS is lower than 4.75V, the high voltage channel will be shut down and the 5V power path will be turned on in 100us and act as a new source.

Ordering Information

SY6862 □(□□)□
- Temperature Code
- Package Code
- Optional Spec Code

Ordering Number	Package type	Note
SY6862BQLC	QFN3×4-16	

Features

- 2 to 1 Power MUX:
  - High Voltage Channel: 4.5V to 23V for VCHG Input Range.
  - 5V Channel: 4V to 5.5V for V5V Input Range
- Smooth Ramp Control When Channel Transition
- Reverse Blocking Function
- Bi-direction Control for High Voltage Channel
- Fast Role Swap
- I²C Interface
- CC Bypass and Isolation Control
- Dead Battery Wake up Function
- VCONN Path for E-mark Cable
- Protection:
  - Output Current Limit Setting
  - OCP/OVP/TSD/UVP
- RoHS Compliant and Halogen Free
- Compact Package QFN3×4-16

Applications

- USB PD
- Desktop PC
- Laptop PC
- Smart Phone

Typical application

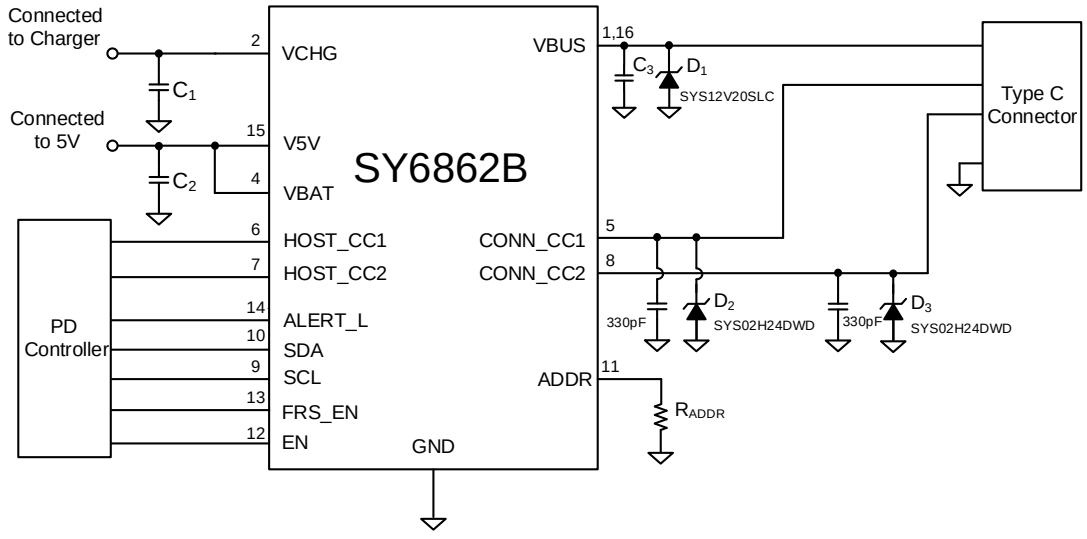
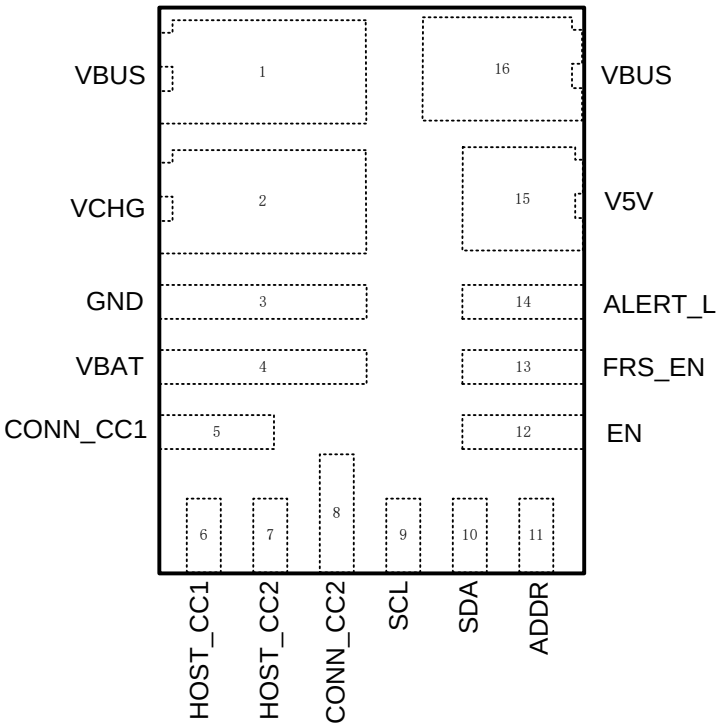


Fig.1 Schematic diagram

Pin-out (top view)



(QFN3×4-16)

Top mark: ECE***xyz*** (Device code: ECE, ***x=year code, y=week code, z= lot number code***)

Pin Name	Pin Number	Pin Description
VBUS	1,16	Connector VBUS pin. Input/output and discharge switches, and powers the IC in the dead battery case.
VCHG	2	4.5V to 23V power input pin. Decouple this pin to PGND with a ceramic capacitor.
GND	3	Ground pin.
VBAT	4	2.5V to 5.5V battery input to provide VCONN power.
CONN_CC1	5	Connect to Type C connector CC1.
HOST_CC1	6	Connect to the host's Type C port controller's CC1 pin.
HOST_CC2	7	Connect to the host's Type C port controller's CC2 pin.
CONN_CC2	8	Connect to Type C connector CC2 .
SCL	9	I^2C Interface serial clock pin. Logic level input.
SDA	10	I^2C Interface serial data pin. Logic level input/output.
ADDR	11	The device address set pin. Connect a resistor to GND to program the I^2C address.
EN	12	Enable control. Pull high to active the device.
FRS_EN	13	Fast role swap function enable pin. Pull high to enable FRS function. Pull low to disable. Do not leave it floating.
ALERT_L	14	Open drain output to signal interrupts. Externally pulled up.
V5V	15	5V input; Provides power for 5V out. Also powers the IC in normal operation.

Block Diagram

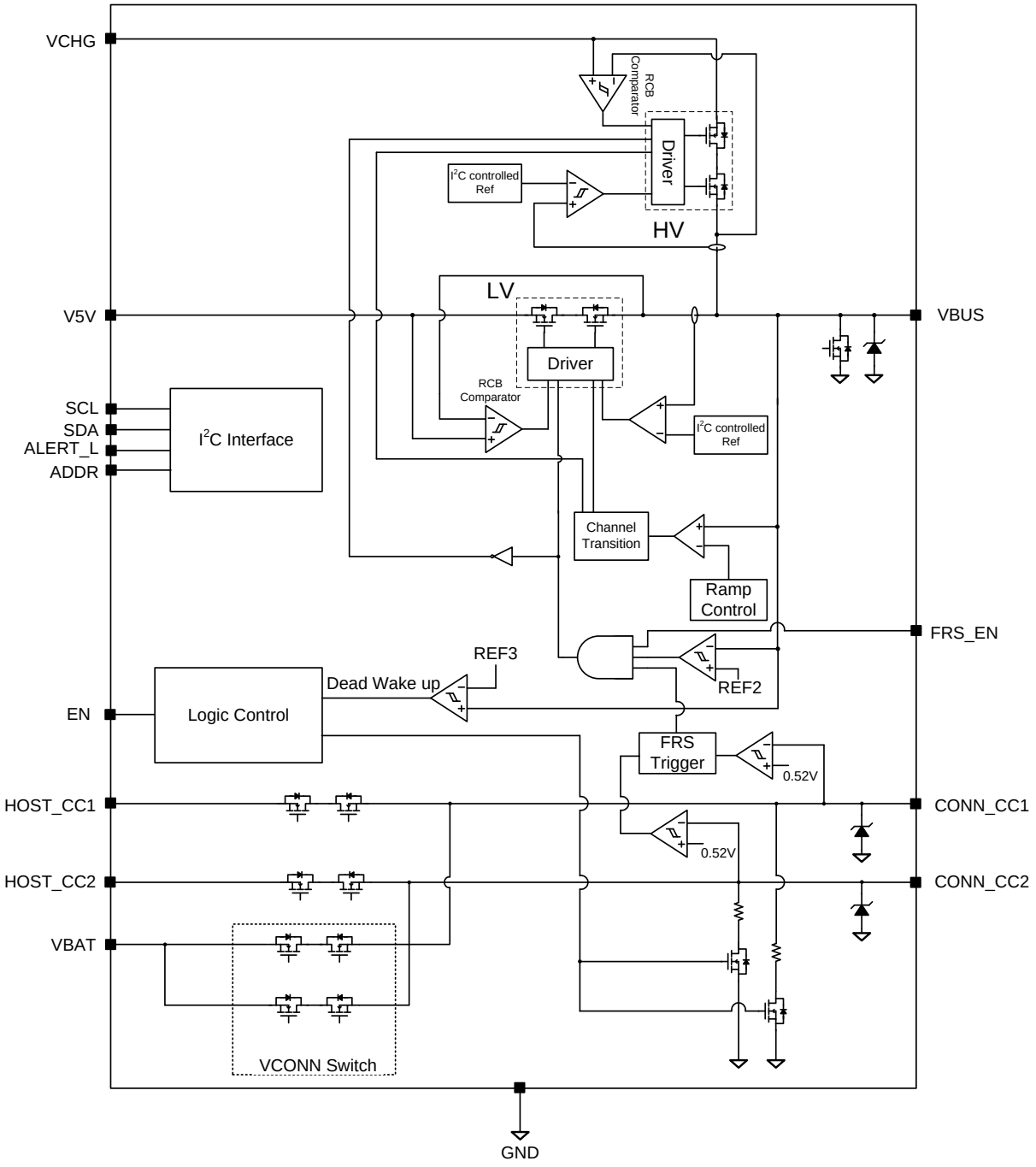


Figure2. Block Diagram

Absolute Maximum Ratings (Note 1)

VCHG ---------- -0.3V to 25V
V5V, VBAT ---------- -0.3V to 6V
CONN_CCx ---------- -0.3V to 30V
VBUS ---------- -0.3V to 28V
EN, FRS ---------- -0.3V to 28V
SCL, SDA, ADDR, ALERT_L, HOST_CCx ---------- -0.3V to 3.6V
Power Dissipation, P_D @ T_A = 25°C QFN3×4 ---------- 2.2W
Package Thermal Resistance (Note 2)
θ_{JA} ----------45°C/W
θ_{JC} ----------28°C/W
Junction Temperature Range ---------- -40°C to 150°C
Lead Temperature (Soldering, 10 sec.) ---------- 260°C
Storage Temperature Range ---------- -65°C to 150°C

ESD Susceptibility (Note 2)

HBM (Human Body Mode)
VBUS, CONN_CC1, CONN_CC2 ---------- 8kV
VCHG, V5V, VBAT, HOST_CC1, HOST_CC2, ALERT_L, EN, SCL, SDA, ADDR, GND, FRS_EN ---------- 2kV

CDM (Charged Device Mode)
All Pins ---------- 500V

Recommended Operating Conditions (Note 3)

VCHG ---------- 4.5V to 23V
V5V, VBAT ---------- 4V to 5.5V
CONN_CCx ---------- 0V to 28V
VBUS, EN, FRS ---------- 0V to 25V
SCL, SDA, ADDR, ALERT_L, HOST_CCx ---------- 0V to 3.3V
Junction Temperature Range ---------- -40°C to 125°C
Ambient Temperature Range ---------- -40°C to 85°C

Electrical Characteristics

(V5V = 5V, VCHG =20V, T_A = 25°C, I_{OUT}= 1A. Unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Voltage Range for Charger Pin	V_{CHG}		4.5		23	V
Voltage Range for VBUS	V_{BUS}		4.0		25	V
Voltage Range for V5V	V_{V5V}		4.0		5.5	V
Voltage Range for VBAT	V_{BAT}		2.5		5.5	V
Under Voltage Protection for VCHG	V_{UVP_CHG}				4.4	V
Hysteresis of Under Voltage Protection for VCHG	$V_{UVP\_CHG\_HYS}$			0.2		V
Under Voltage Protection for VBUS	V_{UVP_VBUS}				3.9	V
Hysteresis of Under Voltage Protection for VBUS	$V_{UVP\_VBUS\_HYS}$			0.1		V
Under Voltage protection for V5V	V_{UVP_V5V}				3.9	V
Hysteresis Under Voltage protection for V5V	$V_{UVP\_V5V\_HYS}$			0.2		V
Under Voltage Protection for VBAT	V_{UVP_BAT}				2.45	V
Hysteresis Under Voltage Protection for V5V	$V_{UVP\_BAT\_HYS}$			0.1		V
Quiescent Current	I_{Q_CHG}	V_{CHG}=20V, V_{V5V}=0V, EN=1, V_{BAT}=0V, OVP_SET=111, Null load. HV channel is selected, source mode		200		µA
		V_{CHG}=20V, V_{V5V}=5V, EN=1, V_{BAT}=0V, OVP_SET=111, Null load. V5V channel is selected		200		µA
	I_{Q_VBUS}	VBUS =20V, V_{V5V}=0V, EN=1, OVP_SET=111, VOUT null load. HV channel is selected, sink mode		200		µA
	I_{Q_V5V}	V_{CHG}=0V, V_{V5V}=5V, EN=1, V_{BAT}=0V, OVP_SET=111, Null load. V5V channel is selected		200		µA
	I_{Q_BAT}	V_{CHG}=0V, V_{V5V}=0V, EN=1, V_{BAT}=5V, OVP_SET=111, Null load.		10		µA
Shutdown Current	I_{SHDN_CHG}	V_{CHG}=20V, V_{V5V}=0V, EN=0, V_{BAT}=0V, OVP_SET=111, Null load.		15		µA
		V_{CHG}=20V, V_{V5V}=5V, EN=0, V_{BAT}=0V, OVP_SET=111, Null load.		20		µA
	I_{SHDN_V5V}	V_{CHG}=0V, V_{V5V}=5V, EN=0, V_{BAT}=0V, OVP_SET=111, Null load.		15		µA
Shutdown Current	I_{SHDN_VBAT}	V_{CHG}=0V, V_{V5V}=0V, EN=0, V_{BAT}=5V, OVP_SET=111, Null load.		8		µA
On Resistance of HV Power Path	$R_{DS(ON)\_HV}$	HV channel is selected, Load is 1A		27	33	mΩ

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
On Resistance of 5V Power Path	$R_{DS(ON)\_5V}$	5V channel is selected, Load is 2A		41	48	mΩ
On Resistance of V_{CONN}	$R_{DS(ON)\_CC}$	VCONN is enabled, load=200mA		170	210	mΩ
On Resistance of CC Bypass	$R_{DS(ON)\_BP}$	CCx_BPS is enable, Load=1mA		40	55	Ω
Reverse Block Threshold for HV	$V_{TH\_RCB\_HV}$	VBUS - VCHG when HV channel is ON		50		mV
Reverse Block Threshold for LV	$V_{TH\_RCB\_5V}$	VBUS - V5V when 5V channel is ON		50		mV
Reverse Block Response Time	t_{REV}			1		µs
Over Voltage Protection for V5V	V_{OVP_V5V}		5.7	6	6.3	V
Over Voltage Protection for VBAT	V_{OVP_CC}		5.7	6	6.3	V
Over Response Time	t_{OV}	V5V rise from 5V to 7V		100		ns
Over Voltage Protection for HV	V_{OVP_HV}	Default: OVP_SET=000	5.7	6	6.3	V
		OVP_SET=001	8	8.4	8.8	V
		OVP_SET=010	10.7	11.3	11.8	V
		OVP_SET=011	11.7	12.3	12.9	V
		OVP_SET=100	13.5	14.2	14.9	V
		OVP_SET=101	17	17.9	18.8	V
		OVP_SET=110	20.5	21.6	22.7	V
		OVP_SET=111	22.5	23.7	24.9	V
Over Response Time of HV Channel	t_{OV_HV}	OVP_SET=000, VBUS change from 5V to 8V		100		ns
Sourcing/Sinking Current Limit Threshold for HV Power Path	I_{LIM_HV}	Current limit control bit [00]	1	1.25	1.5	A
		Current limit control bit [01]	1.5	1.75	2	A
		Default: Current limit control bit [10]	3	3.3	3.6	A
		Current limit control bit [11]	5	5.5	6	A
Sourcing Current Limit Threshold for 5V Power Path	I_{LIM_5V}	Current limit control bit [00]	1	1.25	1.5	A
		Current limit control bit [01]	1.5	1.75	2	A
		Current limit control bit [10]	2	2.25	2.5	A
		Default: Current limit control bit [11]	3	3.3	3.6	A
Current Limit Response Time for HV Power Path/ ALERT_L Response Time for Over Current Protection	t_{OC}	Current limit response time control bit[00]		1		ms
		Default: Current limit response time control bit[01]		10		ms
		Current limit response time control bit[10]		50		ms
		Current limit response time control bit[11]		100		ms
V_{CONN} Current Limit Threshold	I_{VCONN}	VBAT=5V, VCONNx=1	600	660	720	mA
Current Limit Response Time of V_{CONN}	t_{VCONN_OC}			4		µs

Parameter		Symbol	Test Conditions	Min	Typ	Max	Unit
Thermal Shutdown Temperature		T_{SD}			150		°C
Thermal Shutdown Hysteresis		T_{HYS}			15		°C
Transition Speciation							
Positive Slew Rate of VBUS When Channel Transition		V_{SLEW_POS}			2		V/ms
Negative Slew Rate of VBUS When Channel Transition		V_{SLEW_NEG}			-2		V/ms
Rise Time of V_{CONN}		t_{rise_VCONN}			250		μs
Transition Response Time		t_D	Measure from I^2C ACK to VOUT start rise or fall		1		ms
Discharge Resistance		R_{DSG}	RDSG bit[00]		200		Ω
			RDSG bit[01]		400		Ω
			RDSG bit[10]		800		Ω
			RDSG bit[11]		1600		Ω
Discharge Time		t_{DSG}	TDSG bit[00]		50		ms
			TDSG bit[01]		100		ms
			TDSG bit[10]		200		ms
			TDSG bit[11]		400		ms
Fast Role Swap Trigger Threshold		V_{FRS}	HV_DR=0, FRS_EN=1, VBUS drop, measure V5V - VBUS		40		mV
Fast Role Swap Trigger Threshold on CC		V_{FRS_CC}	HV_ER=0, FRS_EN=1, CC_FRS=1	0.49	0.52	0.55	V
Fast Role Swap Response		t_{FRS}	V5V =5V. From VOUT drop below than 4.75V to VOUT back 4.75V			100	μs
$\overline{EN}$/EN Threshold	Logic-low Voltage	V_{IL}	(Note 4)			0.4	V
	Logic-high Voltage	V_{IH}	(Note 4)	1.5			V
I^2C Compatible Interface							
Maximum Operating Frequency			(Note 4)		1		MHz
SDA and SCL Input Logic Threshold		Logic_L	(Note 4)			0.4	V
		Logic_H	(Note 4)	1.5			V
SDA Output Low Voltage			(Note 4)			0.4	V

Note 1: Stresses beyond the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability

Note 2: θ_{JA} is measured in the natural convection at T_A = 25°C on a high effective 4-layer thermal conductivity test board of JEDEC 51-7 thermal measurement standard.

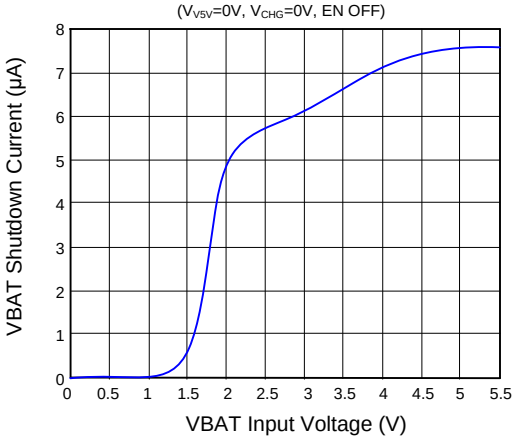
Note 3: The device is not guaranteed to function outside its operating conditions.

Note 4: Guaranteed by design, not production test.

Typical Performance Characteristic

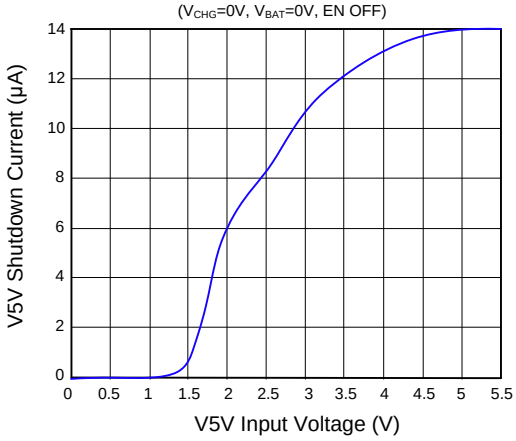
VBAT Shutdown Current vs. VBAT Input Voltage

(V_{V5V}=0V, V_{CHG}=0V, EN OFF)



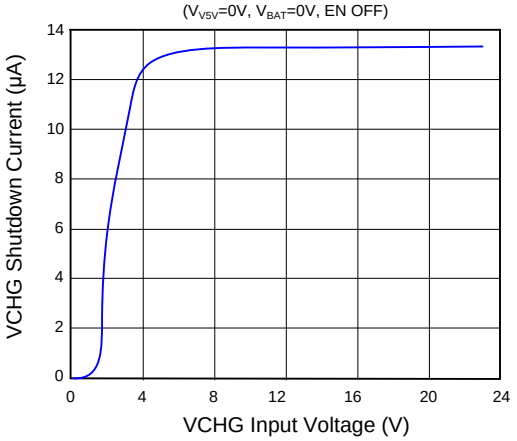
V5V Shutdown Current vs. V5V Input Voltage

(V_{CHG}=0V, V_{BAT}=0V, EN OFF)



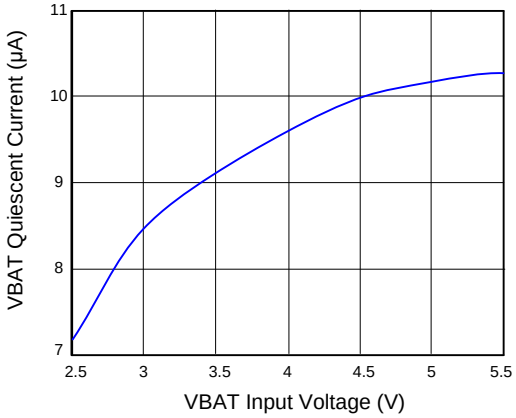
VCHG Shutdown Current vs. VCHG Input Voltage

(V_{V5V}=0V, V_{BAT}=0V, EN OFF)



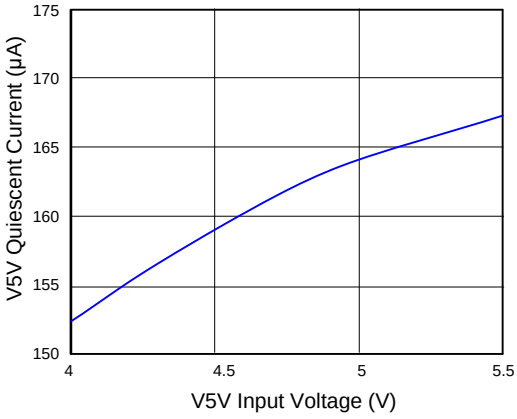
VBAT Quiescent Current vs. VBAT Input Voltage

(V_{CHG}=0V, V_{V5V}=0V, EN ON)



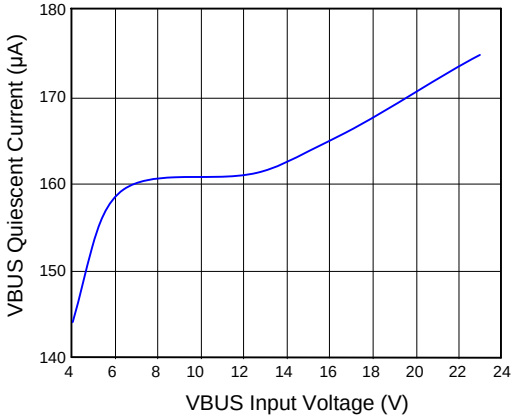
V5V Quiescent Current vs. V5V Input Voltage

(V_{CHG}=0V, V_{BAT}=0V, V5V channel is selected, EN ON)



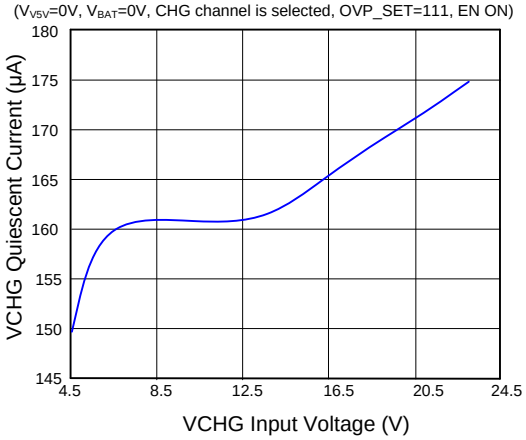
VBUS Quiescent Current vs. VBUS Input Voltage

(V_{V5V}=0V, V_{BAT}=0V, CHG channel is selected, OVP_SET=111, EN ON)



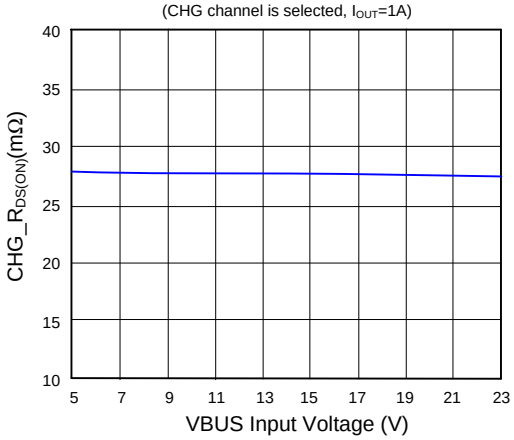
VCHG Quiescent Current vs. VCHG Input Voltage

(V_{V5V}=0V, V_{BAT}=0V, CHG channel is selected, OVP_SET=111, EN ON)



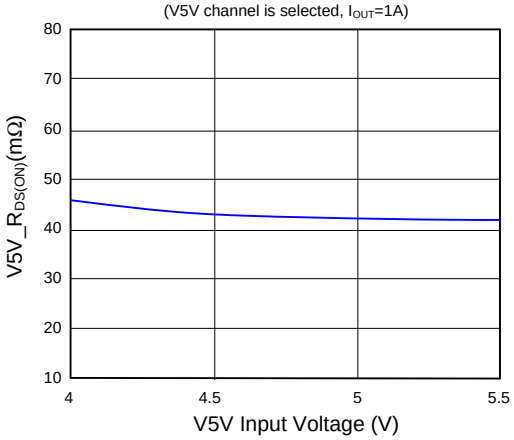
CHG_$R_{DS(ON)}$ vs. VBUS Input Voltage

(CHG channel is selected, I_{OUT}=1A)



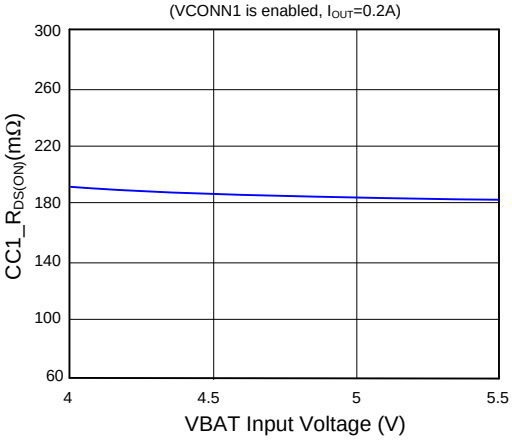
V5V_$R_{DS(ON)}$ vs. V5V Input Voltage

(V5V channel is selected, I_{OUT}=1A)



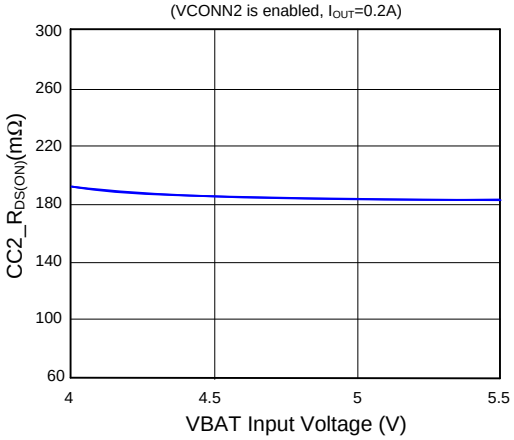
CC1_$R_{DS(ON)}$ vs. VBAT Input Voltage

(VCONN1 is enabled, I_{OUT}=0.2A)



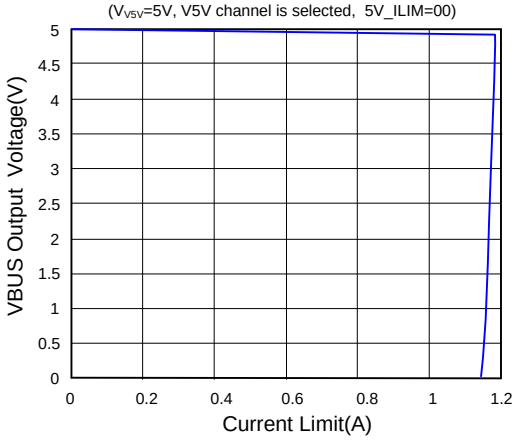
CC2_$R_{DS(ON)}$ vs. VBAT Input Voltage

(VCONN2 is enabled, I_{OUT}=0.2A)



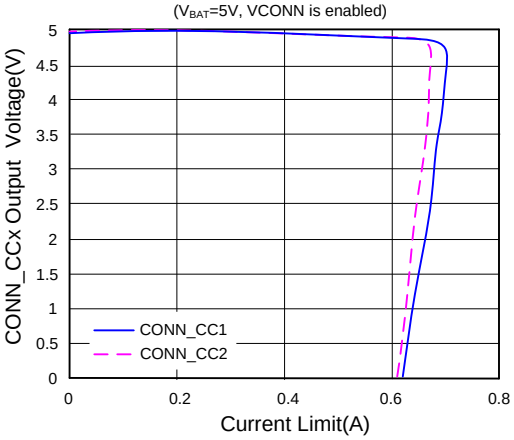
Current Limit vs. VBUS Output Voltage

(V_{V5V}=5V, V5V channel is selected, 5V_ILIM=00)



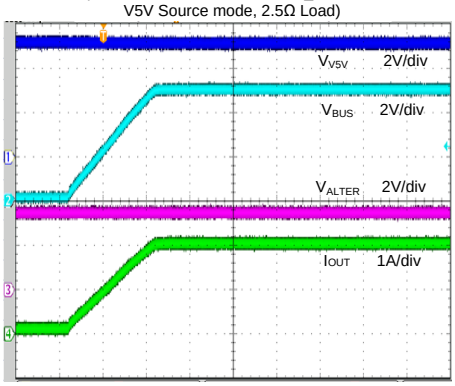
Current Limit vs. CONN_CCx Output Voltage

(V_{BAT}=5V, VCONN is enabled)



V5V_Source ON

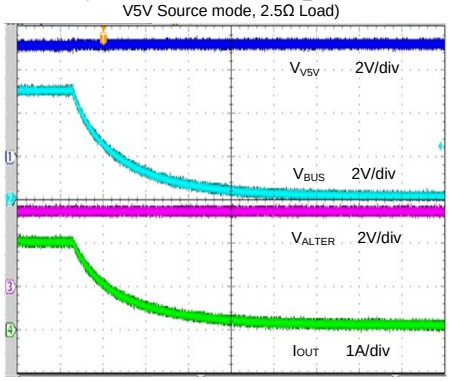
(V_{V5V}=5V, C_{V5V}=C_{BUS}=10uF, 5V_ILIM=11, V5V Source mode, 2.5Ω Load)



Time (800μs/div)

V5V_Source OFF

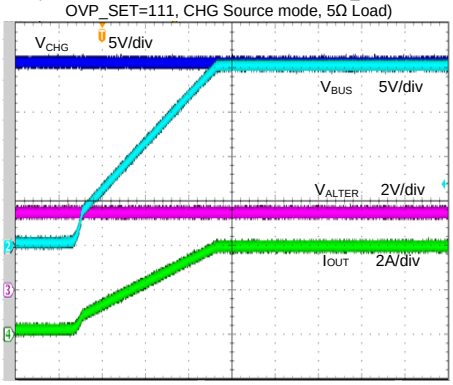
(V_{V5V}=5V, C_{V5V}=C_{BUS}=10uF, 5V_ILIM=11, V5V Source mode, 2.5Ω Load)



Time (20μs/div)

CHG_Source ON

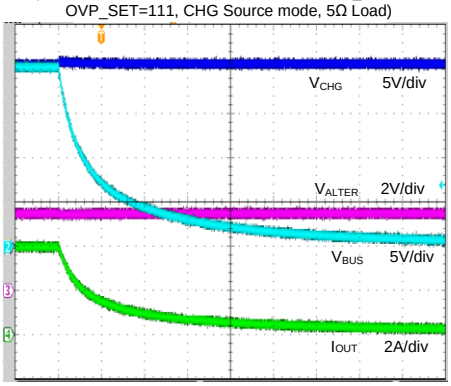
(V_{CHG}=20V, V_{V5V}=5V, C_{CHG}=C_{BUS}=10uF,CHG_ILIM=11, OVP_SET=111, CHG Source mode, 5Ω Load)



Time (2ms/div)

CHG_Source OFF

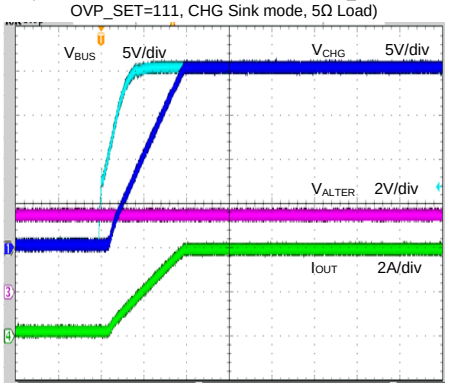
(V_{CHG}=20V, V_{V5V}=5V, C_{CHG}=C_{BUS}=10uF, CHG_ILIM=11, OVP_SET=111, CHG Source mode, 5Ω Load)



Time (20μs/div)

VBUS ON

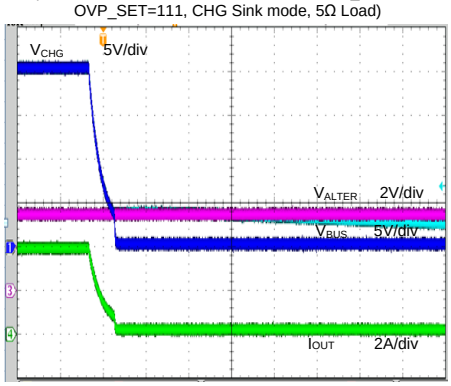
(V_{BUS}=20V, V_{V5V}=5V, C_{CHG}=C_{BUS}=10uF, CHG_ILIM=11, OVP_SET=111, CHG Sink mode, 5Ω Load)



Time (4ms/div)

VBUS OFF

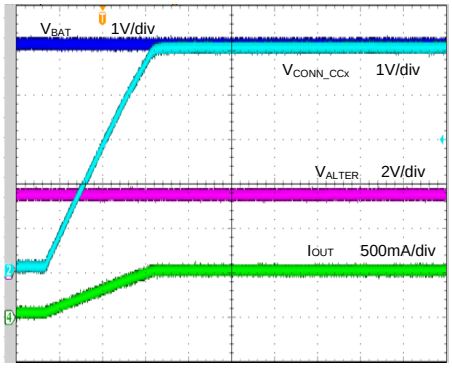
(V_{BUS}=20V, V_{V5V}=5V, C_{CHG}=C_{BUS}=10uF, CHG_ILIM=11, OVP_SET=111, CHG Sink mode, 5Ω Load)



Time (4ms/div)

VCONN Switch ON

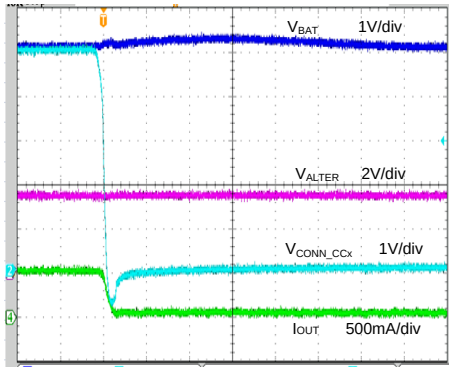
(V_{BAT}=5V, C_{BAT}=1uF, VCONN=1, 10Ω Load)



Time (100µs/div)

VCONN Switch OFF

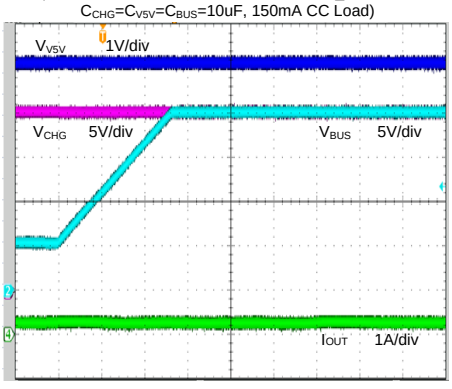
(V_{BAT}=5V, C_{BAT}=1uF, VCONN=0, 10Ω Load)



Time (1µs/div)

Positive Voltage Transitions

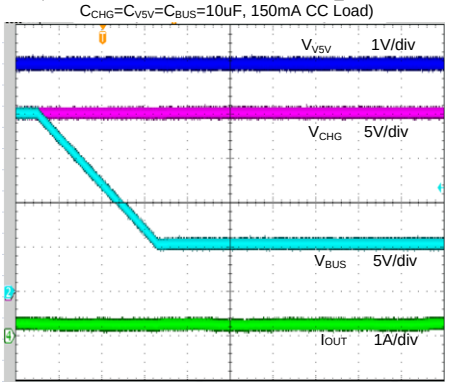
(V_{V5V}=5V, V_{CHG}=20V, V_{BUS}=5V→20V,OVP_SET=111, C_{CHG}=C_{V5V}=C_{BUS}=10uF, 150mA CC Load)



Time (2ms/div)

Negative Voltage Transitions

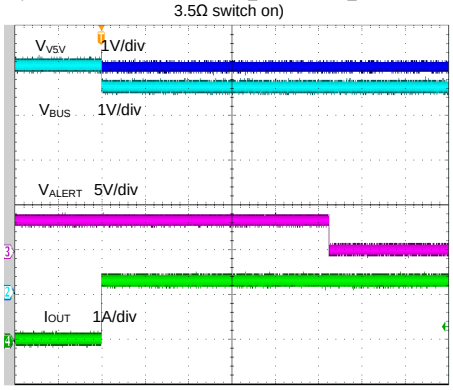
(V_{V5V}=5V, V_{CHG}=20V, V_{BUS}=20V→5V,OVP_SET=111, C_{CHG}=C_{V5V}=C_{BUS}=10uF, 150mA CC Load)



Time (2ms/div)

V5V Channel Over Current Response

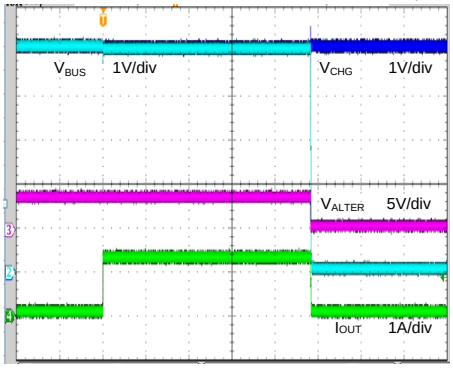
(V_{V5V}=5V, V5V Source mode, 5V_ILIM=00, OC_DELAY=10, 3.5Ω switch on)



Time (10ms/div)

CHG Channel Over Current Response

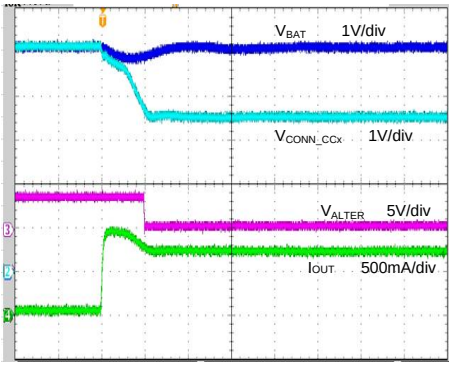
(V_{CHG}=5V, CHG_ILIM=00, DSG_Time=00, OC_DELAY=10, CHG Source mode, C_{CHG}=C_{BUS}=10uF, 3.5Ω switch on)



Time (10ms/div)

VCONN Channel Over Current Response

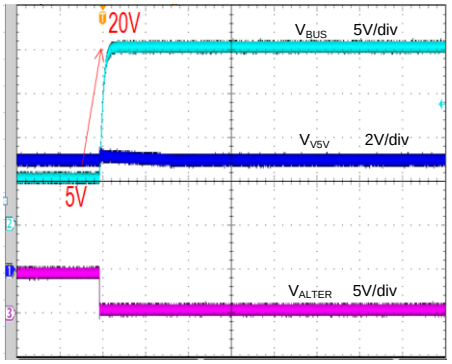
(V_{BAT}=5V, C_{BAT}=1uF, Load=5Ω ON)



Time (4μs/div)

V5V Over Voltage Protection Response

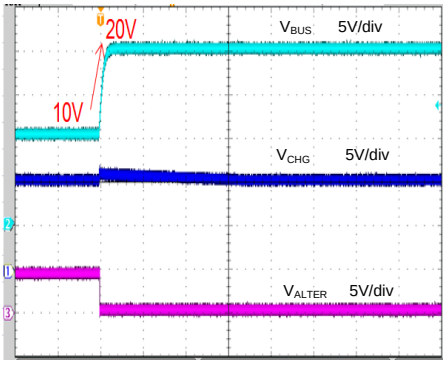
(V_{V5V}=5V, V_{BUS}=5.0V→20.0V, V5V Source mode, C_{V5V}=C_{VBUS}=10uF)



Time (10ms/div)

CHG Over Voltage Protection Response

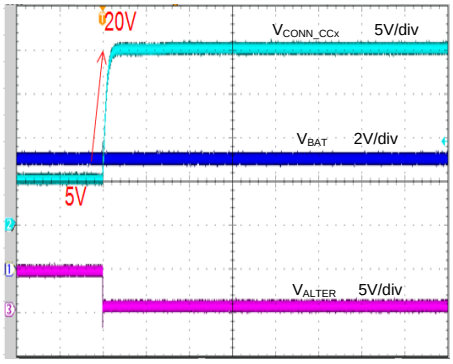
(V_{V5V}=5V, V_{CHG}=10V, OVP_SET=010,V_{BUS}=10.0V→20.0V, CHG Source mode, C_{CHG}=C_{VBUS}=10uF)



Time (10ms/div)

VBAT Over Voltage Protection Response

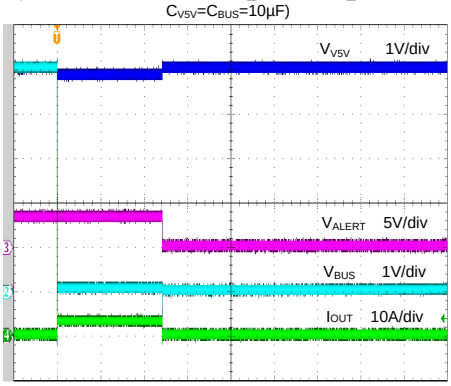
(V_{V5V}=V_{BAT}=5V, VCONN is enabled $V_{CONN\_CC1/2}$=5.0V→20.0V, C_{BAT}=1uF)



Time (10ms/div)

V5V Channel Short Response

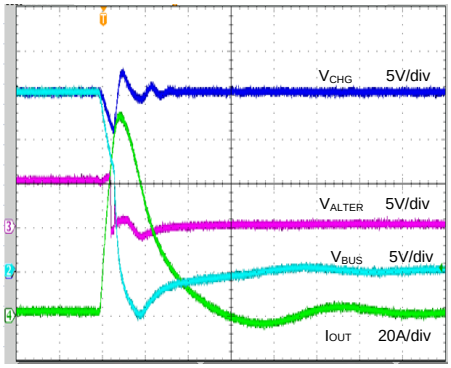
(V_{V5V}=5V, V5V Source Mode, 5V_ILIM=11, OC_DELAY=10, C_{V5V}=C_{BUS}=10μF)



Time (20ms/div)

CHG Channel Short Response

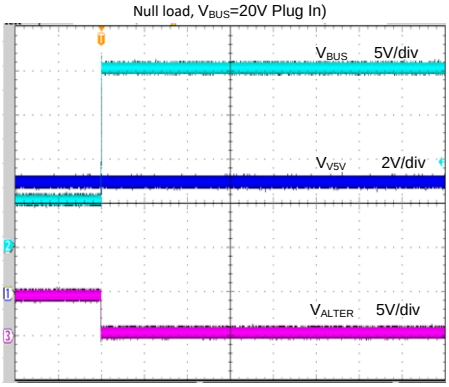
(V_{CHG}=20V, CHG Source mode, EN=ON, C_{CHG}=C_{BUS}=10uF)



Time (2μs/div)

V5V Channel Hot Plug Response

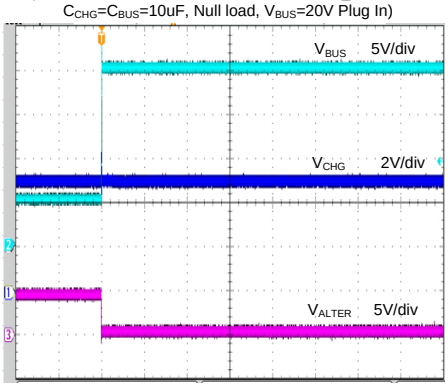
(V_{V5V}=5V, V5V Souece mode, EN ON,C_{V5V}=C_{BUS}=10uF, Null load, V_{BUS}=20V Plug In)



Time (10ms/div)

CHG Channel Hot Plug Response

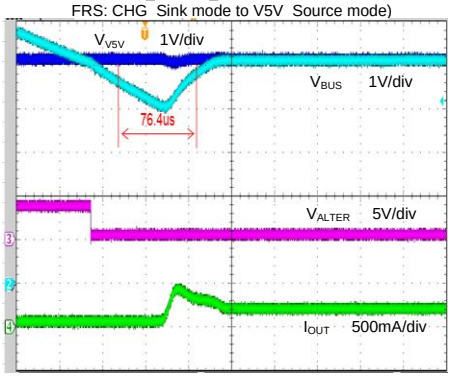
(V_{CHG}=5V, CHG Source mode, EN ON, OVP_SET=000, C_{CHG}=C_{BUS}=10uF, Null load, V_{BUS}=20V Plug In)



Time (10ms/div)

Fast Role Swap

(V_{V5V}=5V , V_{BUS}=10V plug out , C_{V5V}=C_{BUS}=10uF, FRS_EN=CC_FRS=1,0.2A Load, FRS: CHG Sink mode to V5V Source mode)



Time (40μs/div)

Operation

The SY6862B is a 2 to 1 power multiplexer switch providing programmable over current protection and over voltage protection for USB PD application. The SY6862B has a bi-directional high voltage power path that is capable of sinking or sourcing modes through an internal switch path designed to support USB-PD power up to 23V at 5A of current.

The SY6862B incorporates the back to back N-channel MOSFET on two low on resistance power path, so the IC could prevent the current-flow from OUT to IN when OUT being externally forced to a higher voltage than IN.

1. I²C Compatible Interface

The SY6862B integrates an I²C compatible interface. To ensure compatibility with a wide range of system processors, the I²C interface supports clock speeds of up to 400kHz ("Fast-Mode") and uses standard I²C commands. The SY6862B always operates as a slave device, and is addressed using a 7-bit slave address followed by an 8th bit, which indicates whether the transaction is a read-operation or a write-operation.
The I²C interface is fully functional after power supply is above UVLO threshold.

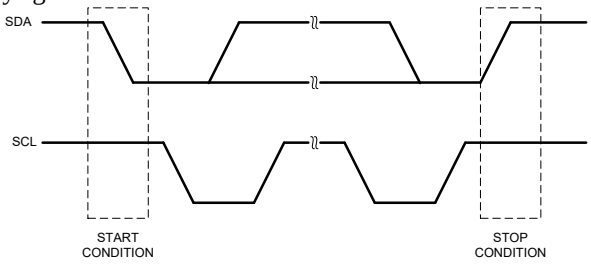
I²C Device Address

When communicating with multiple devices using the I²C interface, each device must have its own unique address so the host can distinguish between the devices. The most significant 5-bits of the device address is '10000' The 6th and 7th-bit device address of SY6862B is select by ADDR pin.

RADDR	Device Address
ADDR short to GND	1000000
44.2k	1000001
200k	1000010
ADDR tie to VCC	1000011

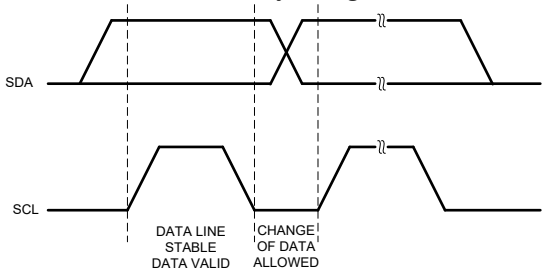
START and STOP Conditions

The START condition is a HIGH to LOW transition of the SDA line while SCL is HIGH. The STOP condition is a LOW to HIGH transition on the SDA line while SCL is HIGH. A STOP condition must be sent before each START condition. The I²C master always generates the START and STOP conditions.



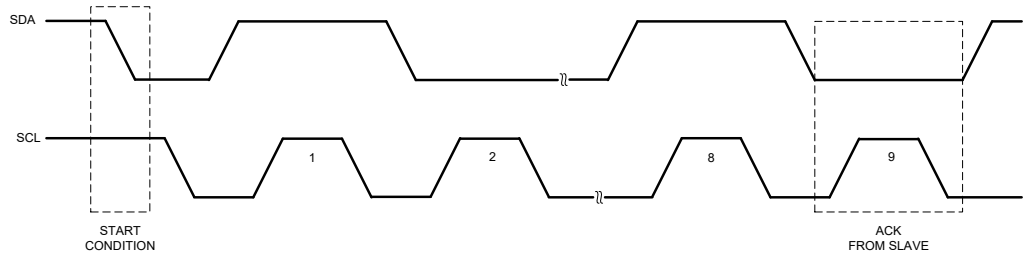
Data Validity

The data on the SDA line must be stable during the HIGH period of the SCL, unless generating a START or STOP condition. The HIGH or LOW state of the data line can only change when the clock signal on the SCL line is LOW.



Acknowledge

Each address and data transmission uses 9-clock pulses. The ninth pulse is the acknowledge bit (ACK). After the START condition, the master sends 7-slave address bits and an R/$\overline{W}$ bit during the next 8-clock pulses. During the ninth clock pulse, the device that recognizes its own address holds the data line low to acknowledge. The acknowledge bit is also used by both the master and the slave to acknowledge receipt of register addresses and data.

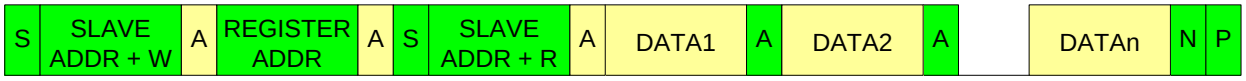


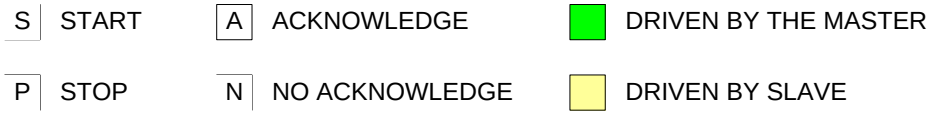
Data Transactions

All transactions start with a control byte sent from the I²C master device. The control byte begins with a START condition, followed by 7-bits of slave address followed by the R/$\overline{W}$ bit. The R/$\overline{W}$ bit is 0 for a write or 1 for a read. If any slave devices on the I²C bus recognize their address, they will acknowledge by pulling the SDA line low for the last clock cycle in the control byte. If no slaves exist at that address or are not ready to communicate, the data line will be 1, indicating a Not Acknowledge condition. Once the control byte is sent, and the SY6862B acknowledges it, the 2nd byte sent by the master must be a register address byte. The register address byte tells the SY6862B which register the master will write or read. Once the SY6862B receives a register address byte it responds with an acknowledgement. If a STOP condition is detected after the register address byte is received, the SY6862B takes no further action but storing the register address byte. The registers address byte auto increase when multiple date bytes are transited.

Write

Random Read





Register Map

Status register: 0x00

Bit 7							Bit 0
OC_HV	RVS	OC_5V	OVP	FRS	TSD	Vsafe5V	Vsafe0V
R	R	R	R	R	R	R	R

Bit 7 OC_HV: Over current indicator for High voltage power path. Load current exceeds the current limit value for longer than Toc. This bit will be set and power FET is turned off. This bit will be cleared when read if the error condition has been removed. This bit will cause the ALERT_L pin to be asserted

1 = Load current exceeds the current limit value.

0 = High voltage power path not over current

Bit 6 RVS: Reverse Block indicator for selected power path. When OUT is higher than IN 50mV, this bit will be set to 1. This bit will be cleared when read if the error condition has been removed. This bit will cause the ALERT_L pin to be asserted

- High voltage path is enabled, source mode.

1 = VBUS > VCHG +50mV

0 = Reverse block is not triggered

- High voltage path is enabled, sink mode.

1 = VCHG > VBUS +50mV

0 = Reverse block is not triggered

- 5V voltage path is selected.

1 = VBUS > V5V +50mV

0 = Reverse block is not triggered

Bit 5 OC_5V: Over current indicator for 5V voltage power path. This bit will be cleared when read if the error condition has been removed. This bit will cause the ALERT_L pin to be asserted

1 = Load current exceeds the current limit value.

0 = 5V voltage power path not over current

Bit 4 OVP: Over Voltage Protection for the selected channel. When 5V channel is selected, SY6862B will detect the VBUS voltage. Once VBUS is larger than 6V, this bit will be set to 1 and power FET will be turned off. When HV channel is selected, SY6862B will detect the VBUS voltage. Once the VBUS is larger than the presetting threshold by OVP_SET, this bit will be set to 1 and power FET will be turned off.

1 = VBUS OVP is triggered

0 = OVP is not triggered

Bit 3 FRS: Fast role swap is triggered. VBUS is lower than 4.75V. Fast role swap is triggered. HV channel is shutdown. V5V is turned on in 100us. This bit will be cleared when read. This bit will cause the ALERT_L pin to be asserted.

1 = FRS is triggered

0 = FRS is not triggered

Bit 2 TSD: Thermal shutdown indicator. When the junction temperature exceeds 150℃, this bit is set to 1. And Power FET is turned off. This bit will be cleared when read if the error condition has been removed. This bit will cause the ALERT_L pin to be asserted.

1 = The junction temperature exceeds 150℃.

0 = The junction temperature is within safe range.

Bit 1 Vsafe5V: Indicator VBUS is at Vsafe5V range.

1 = 4.0V< VBUS < 5.5V

0 = VBUS is out of Vsafe5V range.

Bit 0 Vsafe0V: Indicator VBUS is at Vsafe0V range.

1 = VBUS < 0.8V

0 = VBUS >0.8V

Control Register 1: 0x01

Bit 7							Bit 0
Power_ENB	HV_ILIM		5V_ILIM		HV_DR	CH_SEL	Reserved
W/R	W/R	W/R	W/R	W/R	W/R	W/R	W/R

Bit 7 Power_ENB: Power delivery enable control. Default: 0. This bit will be set to 1 when OC_HV, OVP, TSD is set to high.

1 = Both channel is turned off.

0 = High voltage channel or 5V voltage channel is active. Which channel is active decided by CH_SEL.

Bit 6-5 HV_ILIM: High voltage power path source current limit control bit. Default: 10.

00 = 1.25A

01 = 1.75A

10 = 3.3A

11 = 5.5A

Bit 4-3 5V_ILIM: 5V voltage power path source current limit control bit. Default: 11.

00 = 1.25A

01 = 1.75A

10 = 2.25A

11 = 3.3A

Bit 2 HV_DR: High voltage path power delivery direction control. Default: 0.

1 = Source mode, Delivery power from VCHG to VBUS.

0 = Sink mode, Delivery power from VBUS to VCHG

Bit 1 CH_SEL: Channel selection bit. Default: 1.

1 = High voltage power path is selected.

0 = 5V voltage power path is selected.

Bit 0 Reserved.

Control Register 2: 0x02

Bit 7							Bit 0
OC_DELAY		DSG_TIME		DSG_RON		SDSG	FDSG
W/R	W/R	W/R	W/R	W/R	W/R	W/R	W/R

Bit 7-6 OC_DELAY: Program the over current response delay time. Default: 01.

00: 1ms

01: 10ms

10: 50ms

11: 100ms

Bit 5-4 DSG_TIME: Program the discharge time. Default: 10.

00: 50ms

01: 100ms

10: 200ms

11: 400ms

Bit 3-2 DSG_RON: Program the discharge resister. Default: 00.

00: 200Ω

01: 400Ω

10: 800Ω

11: 1600Ω

Bit 1 SDSG: Smart Discharge mode, Default: 1.

0: Discharge FET ON/OFF is only controlled by FDSG bit.

1: SY6862B worked at smart discharge function.

Bit 0 FDSG: Force Discharge mode, Default: 0.

0: Discharge FET is controlled by SDSG.

1: Discharge FET is forced turned on.

Control Register 3: 0x03

Bit 7							Bit 0
BUSY	OVP_SET			RVS_MASK	Reserved	Reserved	RST_REG
R	W/R	W/R	W/R	W/R	W/R	W/R	W/R

Bit 7 BUSY: I^2C busy indicate. When SY6862B is in channel transition state or count discharge time period, this bit will be set to 1. After this channel transition or discharge timer expired, the bit will set to 0 automatically.

1 = I^2C busy, the command of I^2C will be ignored

0 = Receive I^2C command normally

Bit 6-4 OVP_SET: Over voltage protection setting for HV channel. Default: 000

000: 5V power profile application, typical OVP value is 6V

001: 7V power profile application, typical OVP value is 8.4V

010: 9V power profile application, typical OVP value is 11.1V

011: 10V power profile application, typical OVP value is 12.1V

100: 12V power profile application, typical OVP value is 14.2V

101: 15V power profile application, typical OVP value is 17.9V

110: 18V power profile application, typical OVP value is 21.6V

111: 20V power profile application, typical OVP value is 23.7V

Bit 3 RVS_MASK : LV and HV reverse blocking protection interrupt mask. Default:0.

1: ALERT_L is not response when LV or HV reverse blocking protection is triggered.

0: ALERT_L is pulled low immediately when LV or HV reverse blocking protection is triggered.

Bit 0 RST_REG: Reset all I^2C registers to default value

1: Reset all I^2C registers to default value

0: Default value. No action

Control Register 4: 0x04

Bit 7							Bit 0
CC1_BPS	CC2_BPS	VCONN1	VCONN2	VBAT_OVP	VCONN_OC	CC_FRS	Reserved
W/R	W/R	W/R	W/R	R	R	W/R	W/R

Bit 7 CC1_BPS: Combine HOST_CC1 to CONN_CC1. Before Combine HOST_CC1 to CONN_CC1, the exposed Rd should be removed first. Default: 0.

1 = HOST_CC1 and CONN_CC1 are internal connected.

0 = HOST_CCx and CONN_CCx are isolated.

Bit 6 CC2_BPS: Combine HOST_CC2 to CONN_CC2. Before Combine HOST_CC2 to CONN_CC2, the exposed Rd should be removed first. Default: 0.

1 = HOST_CC2 and CONN_CC2 are internal connected.

0 = HOST_CCx and CONN_CCx are isolated.

Bit 5 VCONN1: VCONN select bit. Default: 0.

1 = Select CONN_CC1 as VCONN. CC1_BPS is set to 0. CONN_CC1 is connected to VBAT.

0 = CONN_CC1 is not selected as VCONN.

Bit 4 VCONN2: VCONN select bit. Default: 0.

1 = Select CONN_CC2 as VCONN. CC2_BPS is set to 0. CONN_CC2 is connected to VBAT.

0 = CONN_CC2 is not selected as VCONN.

Bit 3 VBAT_OVP: When VBAT is over 6V, VBAT_OVP is set to 1. This bit will be cleared when read if the error condition has been removed. This bit will cause the ALERT_L pin to be asserted

1 = VBAT_OVP triggered
0 = VBAT_OVP not triggered

Bit 2 VCONN_OC: VCONN channel over current indication: Once load current is larger ICONN, the VCONN channel will turned off and the VCONNx bit is set to 0. This bit will be cleared when read if the error condition has been removed. This bit will cause the ALERT_L pin to be asserted

1 = Over current on VCONN.

0 = Load is normal on VCONN.

Bit 1 CC_FRS: Fast Role Swap signal detect enable pin. Default: 0.

0: Fast Role Swap signal detection is enabled on CC pin

1: Fast Role Swap signal detection is not enabled. FRS is controlled by FRS_EN and VBUS detection.

2. Channel transition sequence

The SY6862B integrated smooth channel transition control to match USB PD specification. Positive transition sequence is shown below. The voltage ramp will remain monotonic until the voltage reaches final voltage. At the onset of transition, old voltage should not drop more than 150mV. And during transition, load power consumption shall not over 150mW.

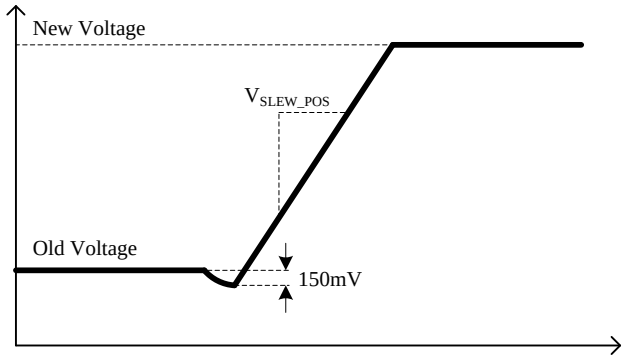


Figure3. Positive Transition

The waveform for a negative voltage transition is shown as Fig. 4. The voltage ramp will remain monotonic until the voltage reaches the final voltage. At the onset of transition, old voltage should not drop more than 150mV. And during transition, load power consumption shall not over 150mW.

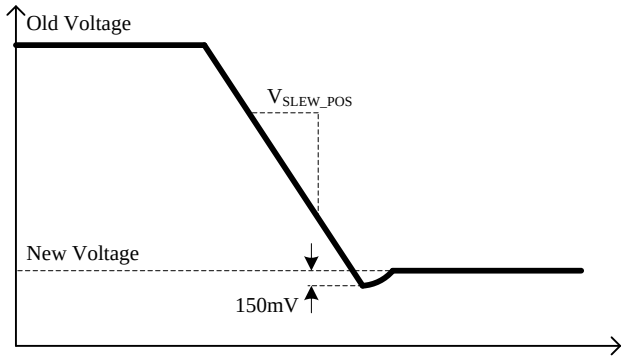


Figure4. Negative Transition

3. EN Control

The EN pin is used for enabling or disabling power segment of the device. When VCHG, V5V or VBAT is presented and EN is high, the power FET can be configured on and off by I^2C, Otherwise the power FET is keeps off. In order to wake up a dead battery system, Once VCHG, V5V and VBAT are under UVLO and VBUS is at Vsafe5V, EN state will be ignored. HV channel will be turned on to deliver power to the dead battery system.

4. Dead Battery Wake up

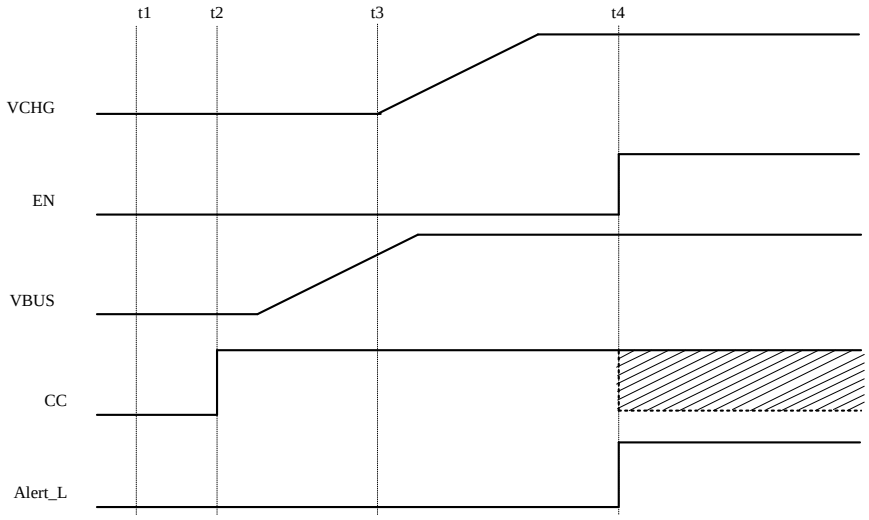


Figure5. Dead Battery Mode Timing Diagram

t1: System is under dead battery condition; the CCs expose an Rd resister to GND as a UFP.

t2: A USB type C DFP is connected. Rd is detected by the DFP.

t3: VBUS is powered on by DFP. Once VBUS is higher than 4.5V, HV power path turned on. VCHG starts rise up.

t4: System logic circuit is supplied by VCHG; EN may be set high after VCHG is high. And once the EN is high, CC pins is connected HOST_CC pins. The CC state is controlled by Host. Alert_L is pulled high.

5. Fast Role Swap

The SY6862B integrates fast role swap function which can support swap from UFP to DFP in 150μs to meet USB PD 3.0 specification. Set CC_FRS to 0, and CCx_BPS to 1, when CCx is lower than 0.52V for longer than 30μs, VCHG channel stop sink current. Meanwhile VBUS will decrease as DFP not provide power anymore. When VBUS drop below than V5V-40mV, the V5V channel will be turned on immediately and pull VBUS above 4.75V within 100μs.

If CC_FRS is set to 1, the SY6862B won't detect CC voltage. During VCHG channel working at sink mode, when VBUS drop below V5V-40mV, VCHG channel is shut down and V5V channel turned on within 100μs.

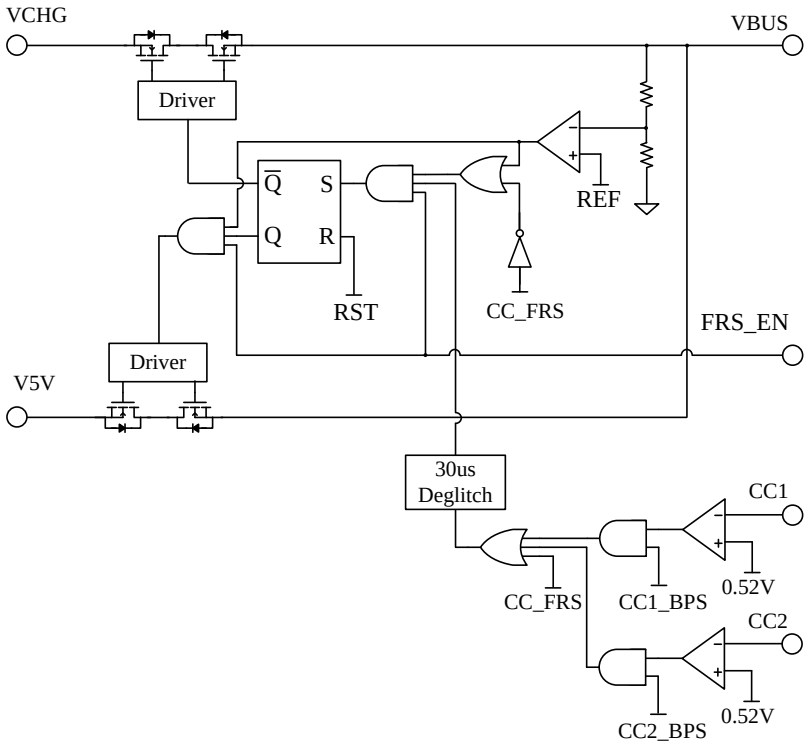


Figure6. Fast Role Swap Block Diagram

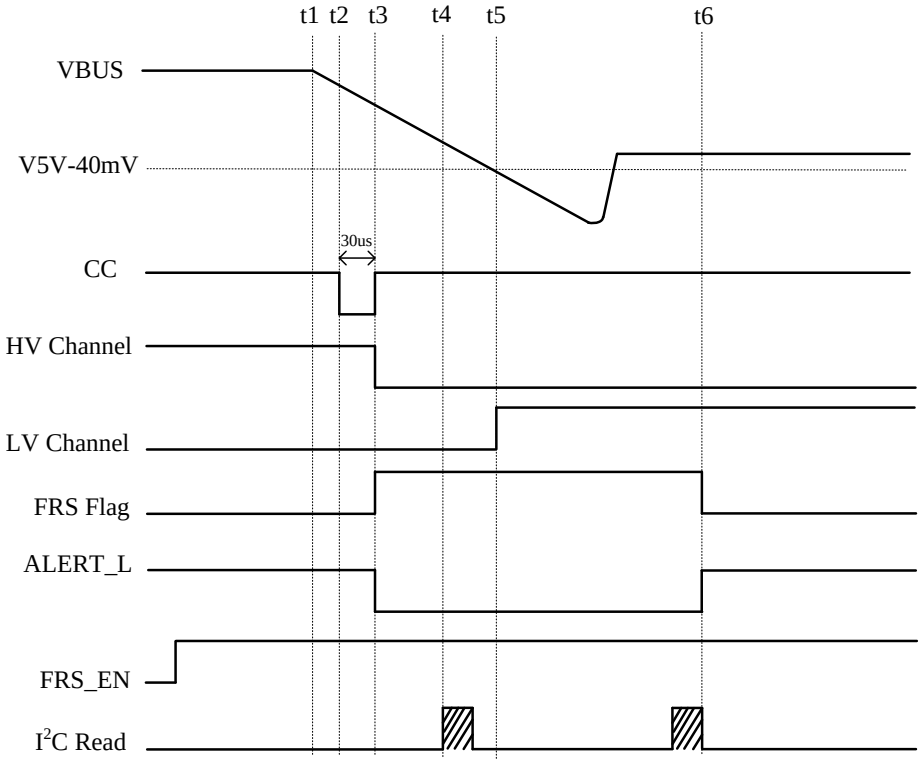


Figure 7. Timing Diagram on CC_FRS=0

t1: VBUS power supply is detached.

t2: Hub sends FRS signal on CC to pull low.

t3: CC deglitch time is done, HV sink channel is turned off, Fast Role Swap is detected and ALERT_L is pulled low.

t4: I²C read the FRS bit. ALERT_L keeps low and FRS flag keeps high unless FRS status is removed

(1. FRS_EN disable, 2. CC_FRS disable, 3. LV channel has already turned on).

t5: When VBUS drops below than V5V-40mV, V5V channel is enabling to drive VBUS

t6: FRS flag is pulled down and ALERT_L is pulled high after I²C read.

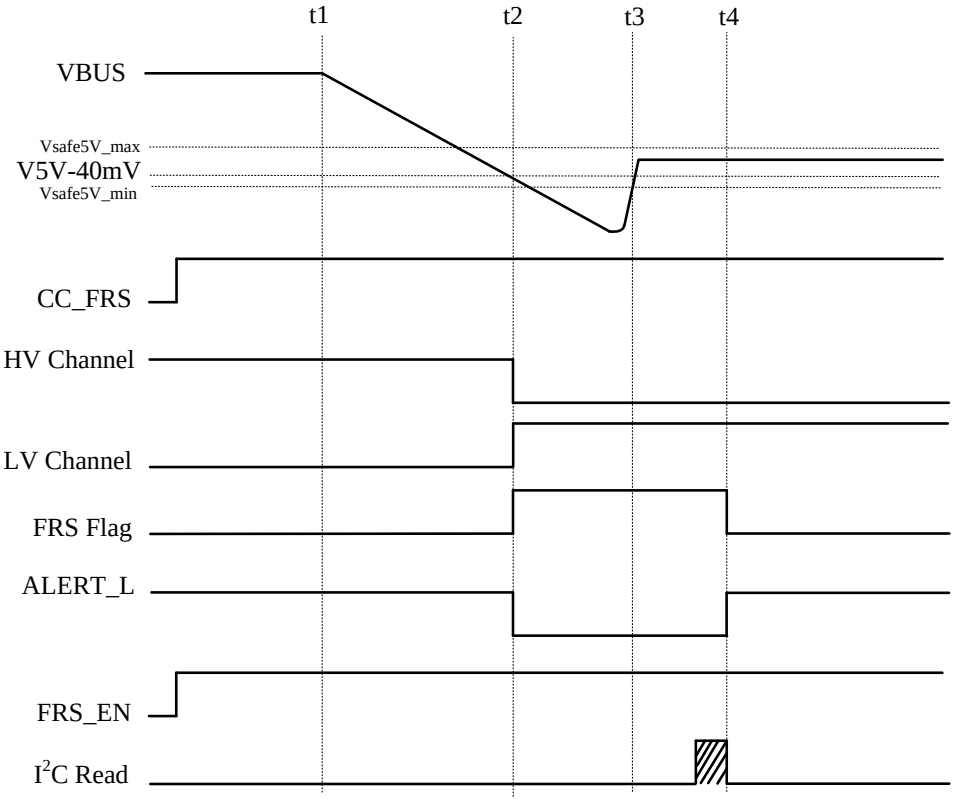


Figure 8. Timing Diagram on CC_FRS=1

t1: VBUS power supply is detached.

t2: When VBUS drops below than V5V-40mV, HV sink channel is turned off, then V5V channel is enabling to drive

VBUS. Fast Role Swap is detected and ALERT_L is pulled low.(This situation is applied for CC_FRS is disabled).

t3: VBUS back to Vsafe5V range. ALERT_L keeps low and FRS flag keeps high unless FRS has been read.

t4: FRS flag is pulled down and ALERT_L is pulled high after I²C read.

6. Smart Discharge Function

The SY6862B integrated smart discharge function. If SDSG is set to 1 and SY6862B works at source mode, VBUS will be auto discharge when UVLO, Channel shutdown, OCP, OVP, TSD. The discharge time is set by writing DSG_TIME[1:0]. The $R_{DS(ON)}$ of discharge FET is set by writing DSG_RON[1:0].

The SY6862B also can be worked at force discharge mode for VBUS. Once SDSG is set to 0, the discharge FET ON/OFF is only controlled by FDSG. When FDSG is 1, the discharge FET is on. When FDSG is 0, the discharge FET is off. The discharge FET $R_{DS(ON)}$ of discharge FET is set by writing DSG_RON[1:0].

7. I²C Busy

During channel transition or counting discharge time, the BUSY bit will be set high. When the busy bit is high, the I²C command will be ignored.

8. Over Current Protection

The SY6862B supports Current limit programming by I²C control at CHG/V5V power path. And the current limit of VCONN path is fixed at 660mA. The current limit of CHG/V5V channel is set by writing code to control register 1(0x01).

Bit 6-5 is CHG power path source and sink current limit control bit(Default:10).

00 = 1.25A

01 = 1.75A

10 = 3.3A

11 = 5.5A

Bit 4-3 is V5V power path source current limit control bit(Default:11).

00 = 1.25A

01 = 1.75A

10 = 2.25A

11 = 3.3A.

For V5V or VCONN channel, once the load current intends to exceed the current limit threshold, the gate of the pass switch is modulated to achieve constant output current. If the over current condition persists for a long time, the junction temperature may exceed 150°C, and over-temperature protection will shut down the part. Once the chip temperature drops below 130°C, the part will restart.

For CHG channel, once load current is over current limit threshold, the power path would be shut down after t_{OC}. Furthermore, once load current is greater than 2.7 times current limit threshold, the power path would be shut down directly.

9. Fault Flag(ALERT_L)

The ALERT_L pin is an open drain output to signal interrupts. The ALERT_L output is asserted (active low) when the over current of LV/HV channel continues to exceed t_{OC}. And the ALERT_L output is asserted directly when thermal shutdown protection, over voltage protection, reverse blocking, or fast role swap is triggered. The output remains asserted until all registers of the device are read by I²C control.

10. Over Voltage Protection

The SY6862B integrated over voltage protection for V5V and VBAT pin. When V5V exceeds 6V (typ.), the power FET of LV channel will be turned off to protect low voltage input stage during reverse block application, and ALERT_L is pulled low to indicate fault condition. When VBAT exceeds 6V(typ.), the VCONN1/2 switch will be disabled to protect low voltage input stage during reverse block application on CONN_CC1/2.

The SY6862B integrated over voltage protection for VCHG and VBUS pin for the HV power path, the power FET of HV channel will be turned off rapidly when VCHG or VBUS exceeds OVP_SET value.

11. Reverse Block Function

The SY6862B integrates reverse block function on CHG power path and V5V power path. Once the deviation voltage of OUT-IN exceeds 50mV, the reverse block function is triggered. The power FET will be shutdown in 1us block the reverse current flow from OUT to IN.

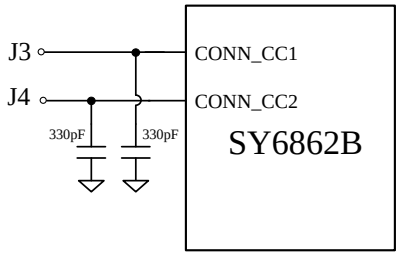
12. CC Line Capacitance

USB PD has a specification for the total amount of capacitance on CC lines, and the specification from section 5.8.6 of the USB PD Specification is given below in Table 1.

Name	Description	Min	Max	Unit	Comment
cReceiver	CC receiver capacitance	200	600	pF	The DFP or UFP system shall have capacitance within this range when not transmitting on the line.

Table1. USB PD cReceiver Specification

A 330pF ceramic capacitor is strongly recommended to be placed on the CC line.



13. CC Dead Battery Mode

The SY6862B exposes a 5.1k resister to GND on CONN_CCx when the device is unpowered. Once the power adaptor detects the pull-down resistor, it would apply 5V on the VBUS pin. As VBUS is exceeds UVLO, the CHG path would be turned on, thus the system is powered and could awake up from dead battery condition.

After system is wake up, PD controller could write CCx_BPS to 1 to take over CC line control for higher power delivery. Pls note once HOST_CCx is bypass to CONN_CCx, the pull down resister is removed, PD controller should also exposed a 5.1k resistor to keep VBUS present. Table 2 shows the CONN_CCx connection state results.

CCx_BPS	VCONNx	CONN_CCx STATE
0	0	Expose a Rd resistor
0	1	Connect to the VBAT
1	0	Connect to the Host_CCx
1	1	Connect to the VBAT

Table2. CONN_CCx Connection State

14. V5V Capacitor

In order to prevent the input voltage drooping during hot-plug events, a 1μF ceramic capacitors from V5V to GND is strongly recommended. However, higher capacitor values could reduce the voltage droop on the V5V further. Furthermore, a VBUS short will cause ringing on the input without the input capacitor. It could destroy the internal circuitry when the input transient exceeds the absolute maximum supply voltage even for a short duration.

15. VBUS Capacitor

A 1μF ceramic capacitor is recommended to be placed close to the IC and output connector to reduce voltage drop during load transient. Higher values of ceramic capacitor can be used for further reducing the drop during high current application.

There would be a high voltage spike during an un-expected high voltage plug into USB type C port. It is strongly recommended add a TVS of SYS12V20SLC on VBUS to GND to clamp the voltage spike lower than absolute voltage rating.

During high voltage application, VBUS may have a negative voltage as the resonance of leakage-inductance of cable wire and output cap. This negative voltage may lead IC work abnormal. It is recommended to add a schottky diode to clamp VBUS at a safe voltage range.

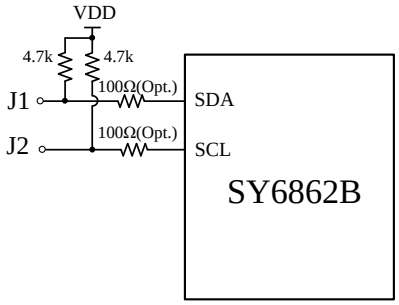
16. VCHG Capacitor

A 10μF or larger input ceramic capacitor is strongly recommended to be placed close to the IC. Furthermore, a VBUS short will cause ringing on the VCHG without the VCHG capacitor. It could destroy the internal circuitry when the VCHG transient exceeds the absolute maximum voltage rating even for a short duration.

The USB PD 3.0 specification defines sink bulk capacitance which shall not exceed 100μF so that the transient charging, or discharging, of the total bulk capacitance on VBUS can be accounted for during voltage transitions.

17. Signal Integrity

A 100Ω resister from SDA/SCL to J1/J2 is recommended to avoid potential signal integrity risk.



18. PCB Layout Guide

For best performance of the SY6862B, the following guidelines must be strictly followed:

1. Keep all VBUS traces as short and wide as possible and use at least 2-ounce copper for all VBUS traces.
2. Locate the output capacitor as close to the connectors as possible to lower impedance (mainly inductance) between the port and the capacitor and improve transient performance.
3. Input and output capacitors should be placed closed to the IC and connected to ground plane to reduce noise coupling.
4. The VBUS, CONN_CC1 and CONN_CC2 pins are exposed externally and adding a TVS each is necessary to prevent surge voltage.

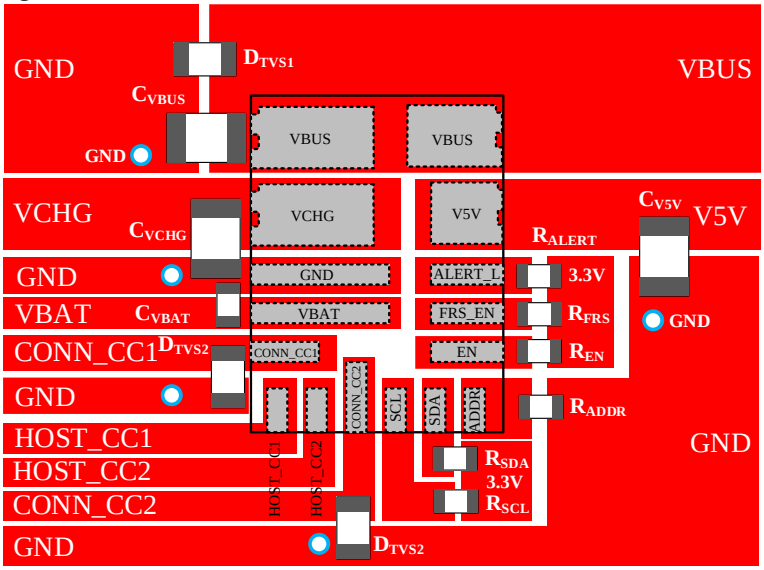
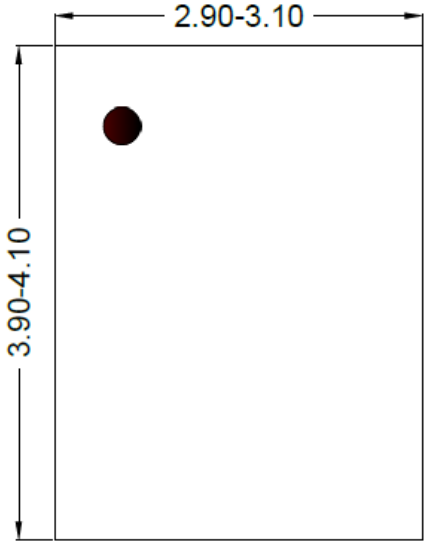
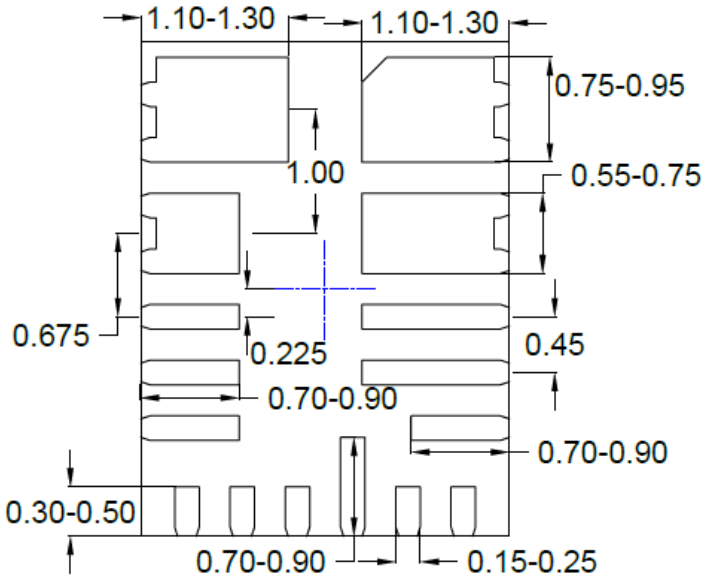


Fig.9 PCB Layout Suggestion

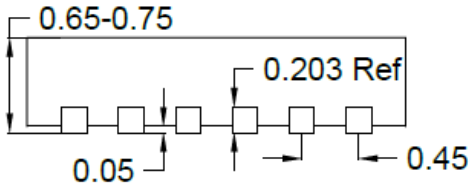
QFN3×4-16 Package Outline Drawing



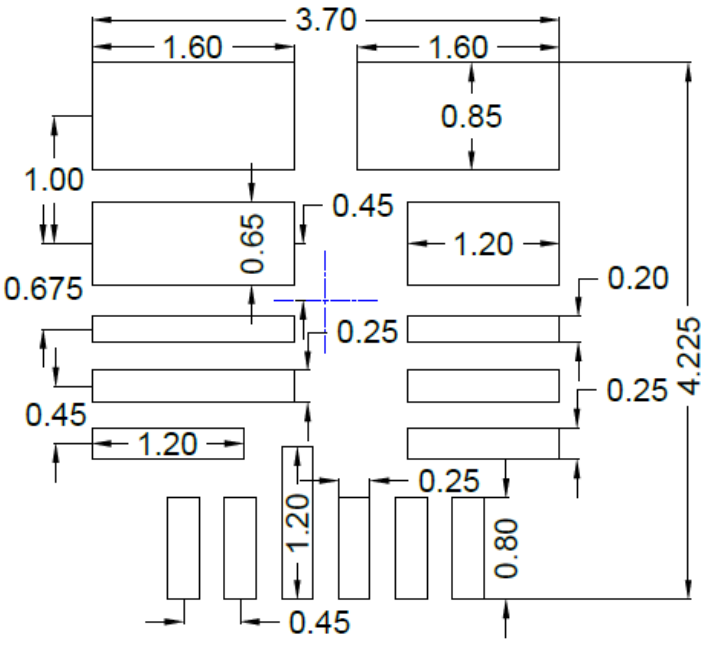
Top View



Bottom View



Side View



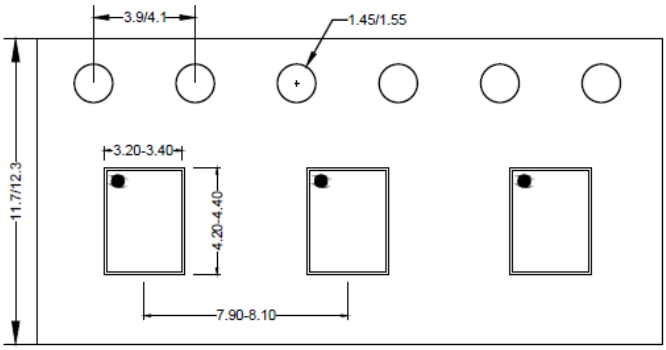
Recommended PCB layout
(Reference only）

Notes: 1, All dimension in millimeter and exclude mold flash & metal burr.
2, Center of PCB refers the chip body Center.

Taping & Reel Specification

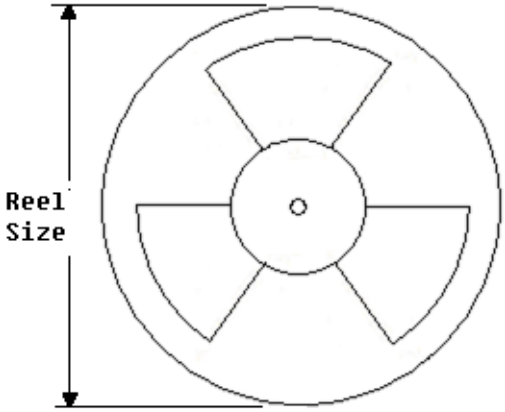
1. Taping orientation

QFN3×4



Feeding direction ⟶

2. Carrier Tape & Reel specification for packages



Package type	Tape width (mm)	Pocket pitch(mm)	Reel size (Inch)	Trailer length(mm)	Leader length (mm)	Qty per reel
QFN3×4	12	8	13"	400	400	5000

3. Others: NA

Revision History

The revision history provided is for informational purpose only and is believed to be accurate, however, not warranted. Please make sure that you have the latest revision.

Date	Revision	Change
Mar.22, 2022	Revision 1.0	1. Update the ON resistance (page 5~6); 2. Add Max. value of "On Resistance of CC Bypass" (page 6); 3. Add Note 4 in EC table (page 7).
Dec.23, 2021	Revision 0.9B	1. Update the schematic diagram (page 1); 2. Update the PCB Layout Guide (page 26)
Mar.18, 2021	Revision 0.9A	Delete "At sink mode, VCHG will be auto discharged when UVLO, Channel shutdown, OCP, OVP, TSD." in Smart Discharge Function Description. (page23)
Jan.21, 2021	Revision 0.9	Initial Release

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