

## Programmable High Current Overvoltage Protection Switch With Integrated Reverse Blocking FET

### General Description

The SY6880A/B is a programmable over voltage protection switch with high current capability to prevent damage to the downstream system with low voltage rating. It achieves wide input voltage range from  $2.5V_{DC}$  to  $28V_{DC}$ . Metal option is available for two different default OVP thresholds. Integrated reverse blocking FET prevents the leakage current from the output side to the input side when input power supply is removed. Extremely low power path resistance  $R_{PWPT}$  helps to reduce power loss during the normal operation. An open-drain indicator pin is opened to show the operation status of device. It integrates the over-temperature protection shutdown and auto-recovery with hysteresis to protect against over current events. This IC along with small CSP (2.0mmx1.8mm) footprint provides small PCB area application.

### Features

- $V_{IN}=2.5V$  to  $28V$ . Absolute Maximum  $V_{IN}=29V$
- Extremely Low Power Path Resistance  $R_{PWPT}$ 
  - $R_{PWPT}=38m\Omega$  typ.
- Programmable Over Voltage Threshold from +4V to +7V
- Metal Option for Different Default OVP Thresholds
  - SY6880A: 6.8V  $\pm 2.9\%$ ;
  - SY6880B: 5.825V  $\pm 3\%$ ;
- Open-drain Indicator Pin for Operation Status
- Surge Protection up to +80V
- Internal Soft-start to Prevent In-rush Current
- Thermal Shutdown Protection & Auto Recovery
- RoHS Compliant and Halogen Free
- Compact Package: CSP 2.0mmx1.8mm

### Ordering Information

SY6880 □(□□)□  
 └─┬─┬─┬─  
 Temperature Code  
 Package Code  
 Optional Spec Code

Ordering Number	Package type	Note
SY6880APGC	CSP2x1.8-12	----
SY6880BPGC	CSP2x1.8-12	----

### Applications

- Smart Phone
- Tablet PCs
- Mobile Device

### Typical Applications

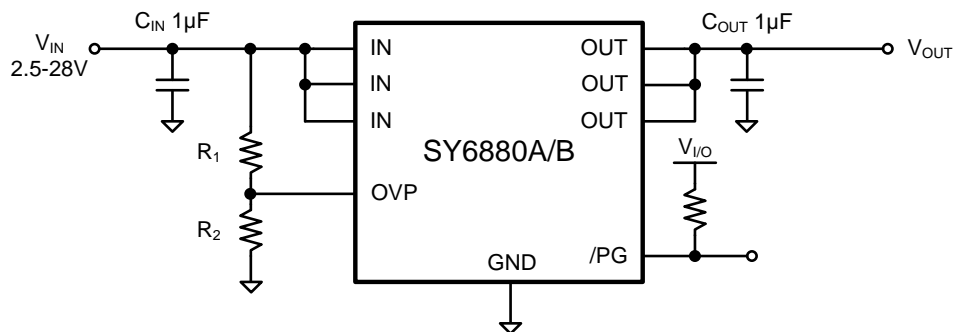
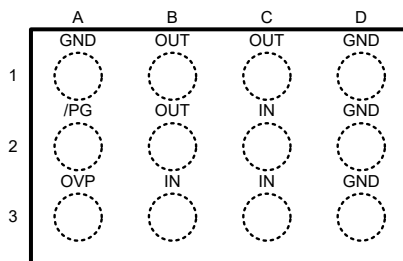


Figure1. Schematic Diagram

## Pinout (top view)



(CSP2×1.8-12)

Top mark: **XH**xyz for **SY6880A** (Device code: XH, x=year code, y=week code, z=lot number code)

**XI**xyz for **SY6880B** (Device code: XI, x=year code, y=week code, z=lot number code)

Pin Name	Pin Number	Pin Description
IN	B3, C2, C3	Power input pin. Connect the IN pins together. Decouple the high frequency noise by connecting at least a 0.1μF MLCC to the ground.
OUT	B1, B2, C1	Output voltage pin. Source side of the internal FET. Connect the OUT pins together for the normal operation.
OVP	A3	External OVP program pin. Connect the resistor divider to this pin to program the OVP threshold. Make sure $V_{OVP}$ is lower than the internal threshold; otherwise the internal default threshold is active. Pulling down this pin to the ground to disable the external program function.
/PG	A2	Open-drain indicator pin. /PG is pulled down when the input voltage is stable in the normal range between minimum $V_{IN}$ and $V_{OVP}$ . /PG is high impedance when thermal shutdown protection or over voltage protection occurs.
GND	A1, D1, D2, D3	Power ground pin.

## Block Diagram

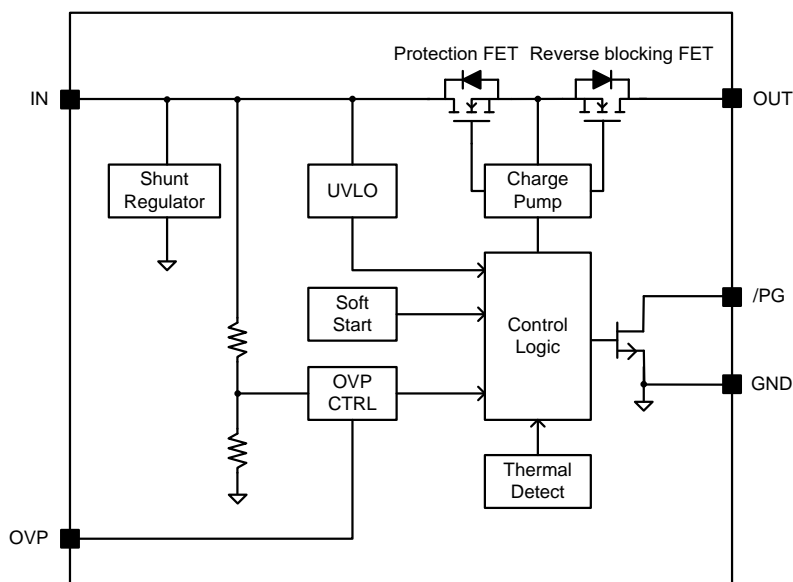


Figure2. Block Diagram



## Absolute Maximum Ratings (Note 1)

IN, OVP	29V
OUT	7V
/PG	6V
Continues IN, OUT Current	5A
Peak IN, OUT Current (10ms)	8A
Power Dissipation, $P_D$ @ $T_A = 25^\circ\text{C}$ , CSP	2.09W
Package Thermal Resistance (Note 2)	
$\theta_{JA}$	59.7°C/W
$\theta_{JC}$	8.97°C/W
Junction Temperature Range	150°C
Lead Temperature (Soldering, 10 sec.)	260°C
Storage Temperature Range	-65°C to 150°C

## Recommended Operating Conditions (Note 3)

IN, OVP	less than 29V
OUT	less than 7V
/PG	less than 6V
Continues IN, OUT Current	less than 5A
Peak IN, OUT current (10ms)	less than 8A
Junction Temperature Range	-40°C to 125°C
Ambient Temperature Range	-40°C to 85°C

## Electrical Characteristics

( $V_{IN} = 2.5V$  to  $28V$ ,  $C_{IN}=1\mu F$ ,  $C_{OUT}=1\mu F$ ,  $T_A = 25^\circ C$ , unless otherwise specified)

Parameter	Symbol	Test Conditions		Min	Typ	Max	Unit
Input Voltage Range	V <sub>IN</sub>			2.5		28	V
Input UVLO Threshold	V <sub>UVLO</sub>					2.4	V
UVLO Hysteresis	V <sub>HYS</sub>				0.1		V
Input Clamp Voltage	V <sub>INCLP</sub>	I <sub>IN</sub> =10mA			33		V
Bias Current	I <sub>BIAS</sub>	V <sub>IN</sub> =5V				100	μA
Internal Default OVP Threshold	V <sub>OVPD</sub>	Rising	SY6880A	6.6	6.8	7.0	V
			SY6880B	5.65	5.825	6.0	V
		Falling	SY6880A	6.5			V
			SY6880B	5.55			V
OVP Program Threshold	V <sub>OVPPT</sub>	SY6880A		1.22	1.26	1.30	V
		SY6880B		1.18	1.22	1.26	V
Programmable OVP Range	V <sub>OVPPR</sub>			4		7	V
Programmable OVP Active Threshold	V <sub>OVPPA</sub>			0.2		0.3	V
Resistance of Power Path	R <sub>PWPT</sub>	V <sub>IN</sub> =5V, I <sub>OUT</sub> =200mA, from IN to OUT			38	53	mΩ
Output Load Capacitance	C <sub>OUT</sub>	V <sub>IN</sub> =5V				1000	μF
OVP Pin Input leakage Current	I <sub>OVPLK</sub>	V <sub>OVP</sub> =V <sub>OVPPT</sub>		-100		100	nA
/PG Low Voltage	V <sub>PGL</sub>	V <sub>IO</sub> =3.3V, I <sub>SINK</sub> =1mA				0.4	V
/PG Leakage Current	V <sub>PGLK</sub>	V <sub>IO</sub> =3.3V, /PG high impedance		-1		1	μA
Deglitch Time	t <sub>DG</sub>	Time from 2.5V<V <sub>IN</sub> <V <sub>OVP</sub> to V <sub>OUT</sub> =10% of V <sub>IN</sub>			15		ms
Switch Turn-on Time	t <sub>ON</sub>	V <sub>IN</sub> =5V, R <sub>L</sub> =100, C <sub>OUT</sub> =100μF; V <sub>OUT</sub> =10% of V <sub>IN</sub> to 90% V <sub>IN</sub>			2		ms
Switch Turn-off Time	t <sub>OFF</sub>	V <sub>IN</sub> > V <sub>OVP</sub> to V <sub>OUT</sub> =80% V <sub>IN</sub> , R <sub>L</sub> =100, C <sub>OUT</sub> =100μF; V <sub>IN</sub> rising lower than 2V/us			2		μs
Thermal Shutdown Temperature	T <sub>SD</sub>				150		°C
Thermal Shutdown Hysteresis	T <sub>HYS</sub>				20		°C

**Note 1:** Stresses beyond the “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

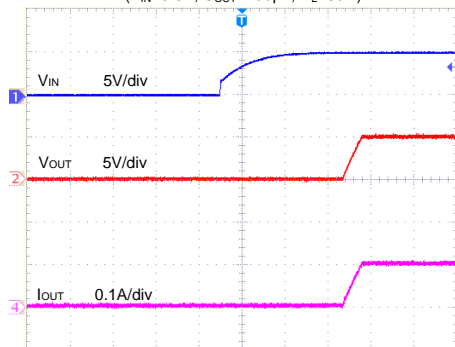
**Note 2:**  $\theta_{JA}$  is measured in the natural convection at  $T_A = 25^\circ C$  on a low effective four-layer thermal conductivity test board of JEDEC 51-3 thermal measurement standard.

**Note 3:** The device is not guaranteed to function outside its operating conditions.

## Typical Performance Characteristics

Power-up Response (SY6880A)

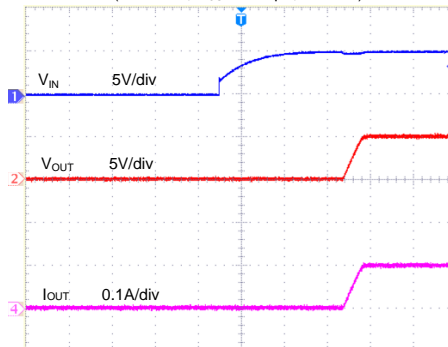
( $V_{IN}=0-5V$ ,  $C_{OUT}=100\mu F$ ,  $R_L=50\Omega$ )



Time (4ms/div)

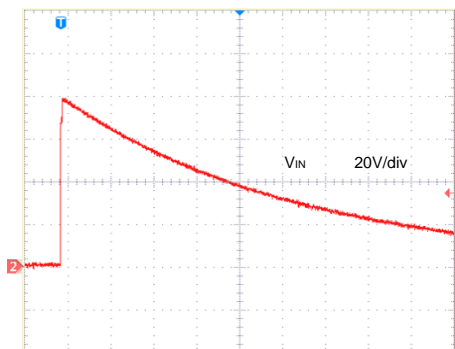
Power-up Response (SY6880A)

( $V_{IN}=0-5V$ ,  $C_{OUT}=1000\mu F$ ,  $R_L=50\Omega$ )



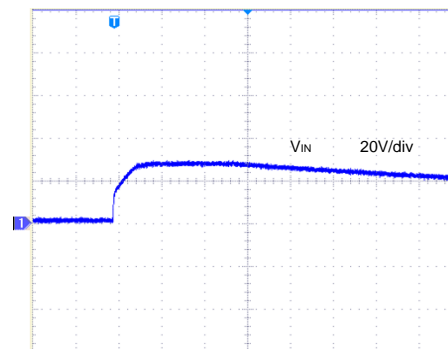
Time (4ms/div)

80V Surge Test Waveform Without SY6880A



Time (10μs/div)

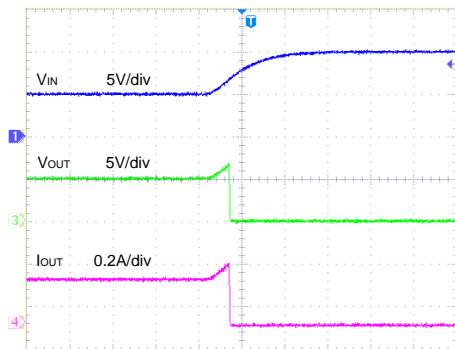
80V Surge Test Waveform With SY6880A



Time (10μs/div)

Over-voltage Fault Response (SY6880A)

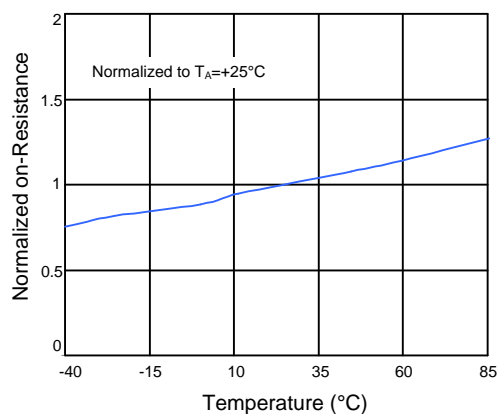
( $V_{IN}=5-10V$ )

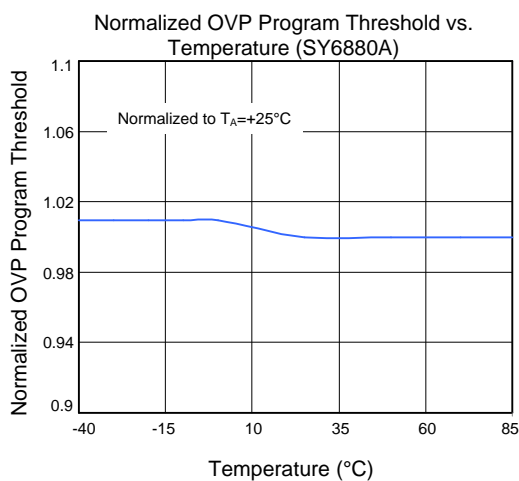
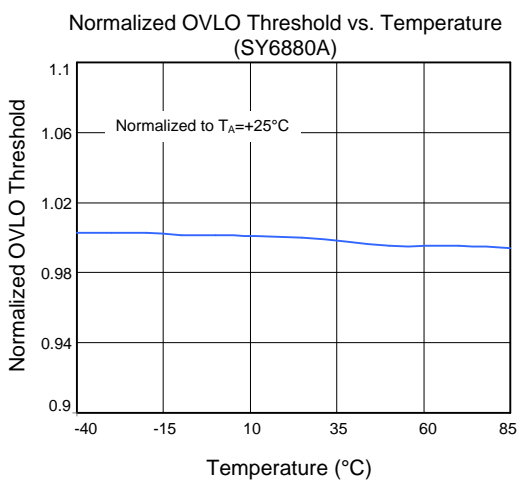
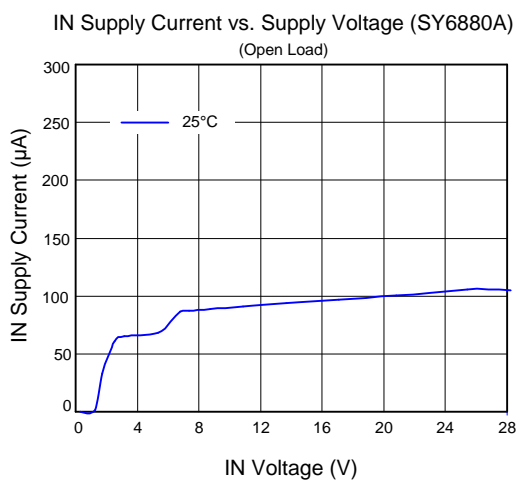
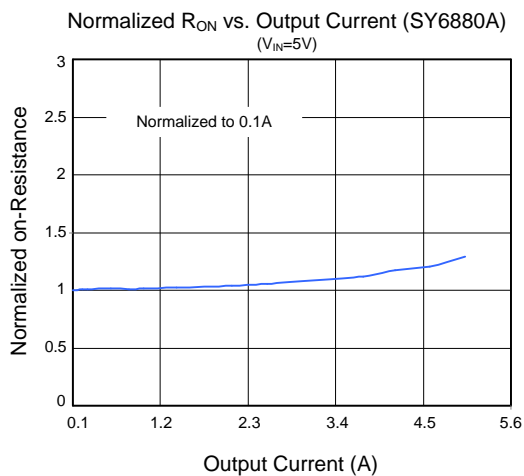
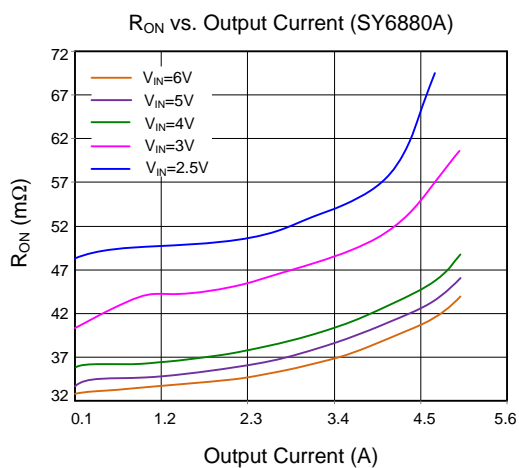


Time (1ms/div)

Normalized  $R_{ON}$  vs. Temperature (SY6880A)

( $V_{IN}=5V$ ,  $R_L=100\Omega$ )





## Applications Information

### IN Bypass Capacitor

For most applications, bypass IN to GND with a 0.1μF ceramic capacitor as close as possible to the device. If the power source has significant inductance due to long lead length, the device clamps the overshoot due to the LC tank circuit.

### OUT Output Capacitor

The slow turn-on time provides a soft-start function that allows the SY6880A/B to charge an output capacitor up to 1000μF without turning off due to an over current condition.

### Programmable OVP Adjustment Functionality

If OVP is connected to ground, the internal OVP comparator uses the internally set OVP value.

If an external resistor-divider is connected to OVP and the  $V_{OVP}$  exceeds the programmable OVP active threshold ( $V_{OVPPA}$ ), the internal OVP comparator reads the IN fraction fixed by the external resistor divider.  $R_1 = 1M\Omega$  is a good starting value for minimum current consumption.

Since  $V_{IN\_OVP}$ ,  $V_{OVPT}$  and  $R_1$  are known,  $R_2$  can be calculated from the following formula:

$$V_{IN\_OVP} = V_{OVPT} \times \left( 1 + \frac{R_1}{R_2} \right)$$

This external resistor-divider is completely independent from the internal resistor-divider.

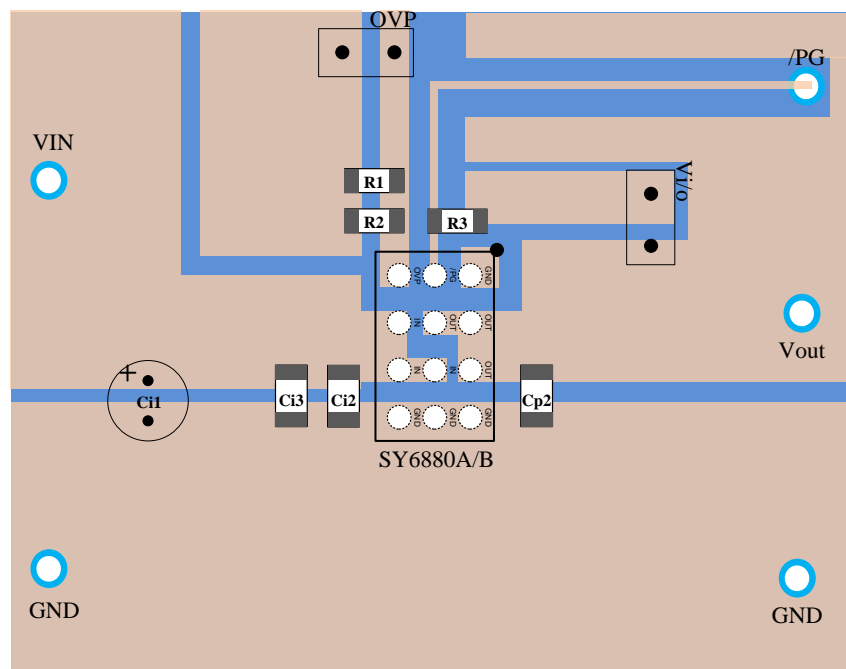
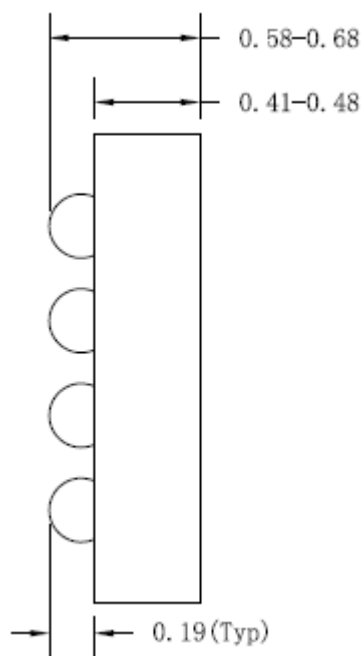
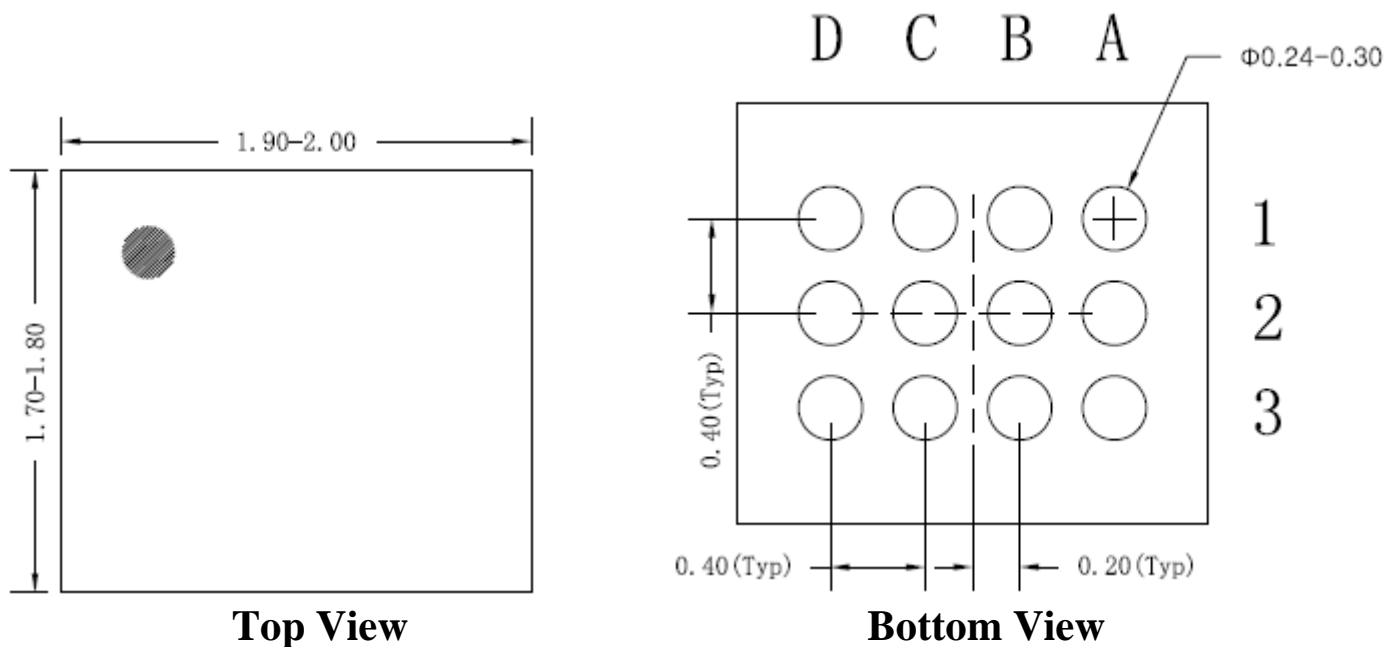


Figure3. PCB Layout Suggestion

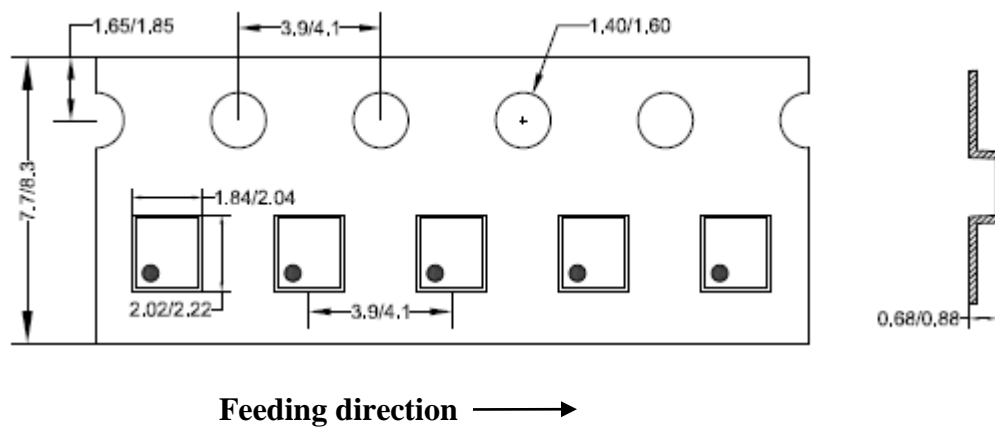
**CSP2.0 ×1.8-12 Outline Drawing**

**Side View**

**Notes:** All dimension in millimeter and exclude mold flash & metal burr

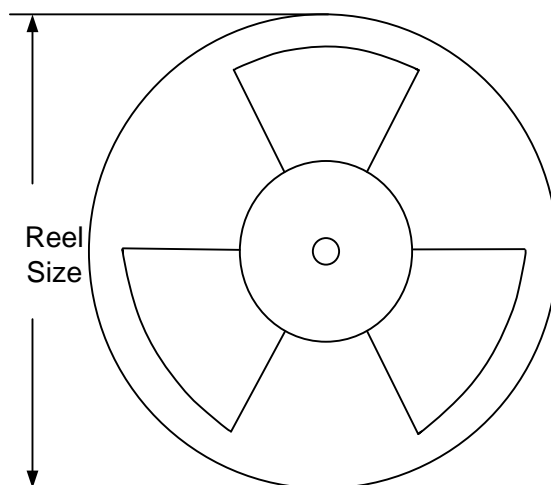


## Taping & Reel Specification

### 1. CSP2×1.8 taping orientation



### 2. Carrier Tape & Reel specification for packages



Package type	Tape width (mm)	Pocket pitch(mm)	Reel size (Inch)	Trailer length(mm)	Leader length (mm)	Qty per reel
CSP2.0×1.8	8	4	7"	400	400	3000

### 3. Others: NA

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