SY6881

Programmable 5A Overvoltage Protection Switch

General Description

SY6881 is a programmable over voltage protection switch with high current capability to prevent damage to the downstream system with low voltage rating. It achieves wide input voltage range from DC 2.5V to DC 28V. Extremely low power path resistance R_{PWPT} helps to reduce power loss during the normal operation. An open drain indicator pin is opened to show the operation status of device. It integrates the over-temperature protection shutdown and auto-recovery with hysteresis to protect against over current events. This IC along with small CSP (1.32mmx1.86mm) footprint provides small PCB area application.

Features

- Surge Protection IEC 61000-4-5 to +100V
- Extremely Low Power Path Resistance R_{PWPT}
  - R_{PWPT}=32mΩ typ.
- Programmable Over Voltage Threshold from +4V to +22V
- Default Over Voltage Threshold 6.8V
- Open Drain Indicator Pin for Operation Status
- Internal Soft Start to Prevent In-rush Current
- Thermal Shutdown Protection & Auto Recovery
- IEC61000-4-2 Air Discharge > 15KV
- IEC61000-4-2 Contact Discharge > 8KV
- RoHS Compliant and Halogen Free
- Compact Package: CSP 1.32mmx1.86mm

Ordering Information

SY6881 □(□□)□
- Temperature Code
- Package Code
- Optional Spec Code

Ordering Number	Package Type	Note
SY6881PTC	CSP1.32x1.86-12	

Applications

- Smart Phone
- Tablet PCs
- Mobile Device

Typical Application

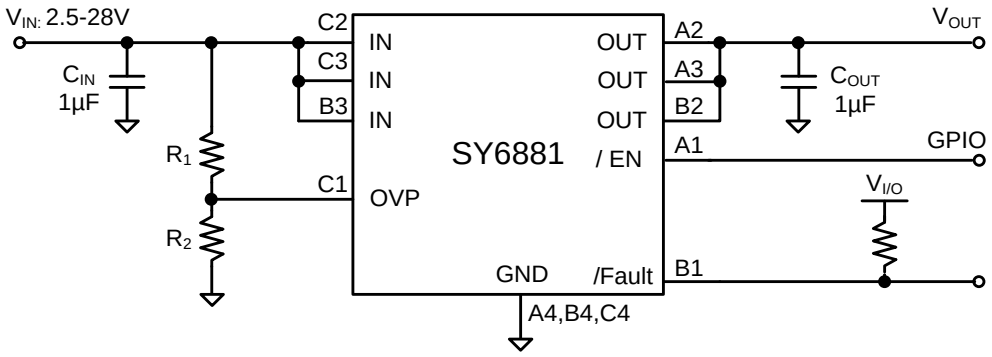
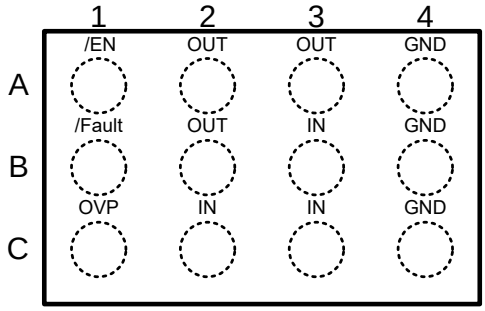


Figure1. Schematic Diagram

Pinout (top view)



(CSP1.32x1.86-12)

Top Mark: **Ntxyz**, **(**Device code: Nt; ***x=year code, y=week code, z= lot number code***)

Pin Name	Pin Number	Pin Description
IN	B3, C2, C3	Power input pin. Connect IN pin together. Decouple high frequency noise by connecting at least a 0.1μF MLCC to ground.
OUT	A2, A3, B2	Output voltage pin. Source side of the internal FET. Connect OUT pins together for normal operation.
OVP	C1	External OVP program pin. Connect resistor divider to this pin to program the OVP threshold. Make sure V_{OVP} is higher than the External OVP select threshold; otherwise the internal default OVP threshold is active. Pull down this pin to ground to disable external program function.
/Fault	B1	Open drain indicator pin. /Fault is pulled low when over voltage, thermal shutdown protection or other fault condition occurs. Otherwise, /Fault pin is high impedance.
GND	A4, B4, C4	Power ground pin.
/EN	A1	Pull low to enable SY6881. Do not leave it floating.

Block Diagram

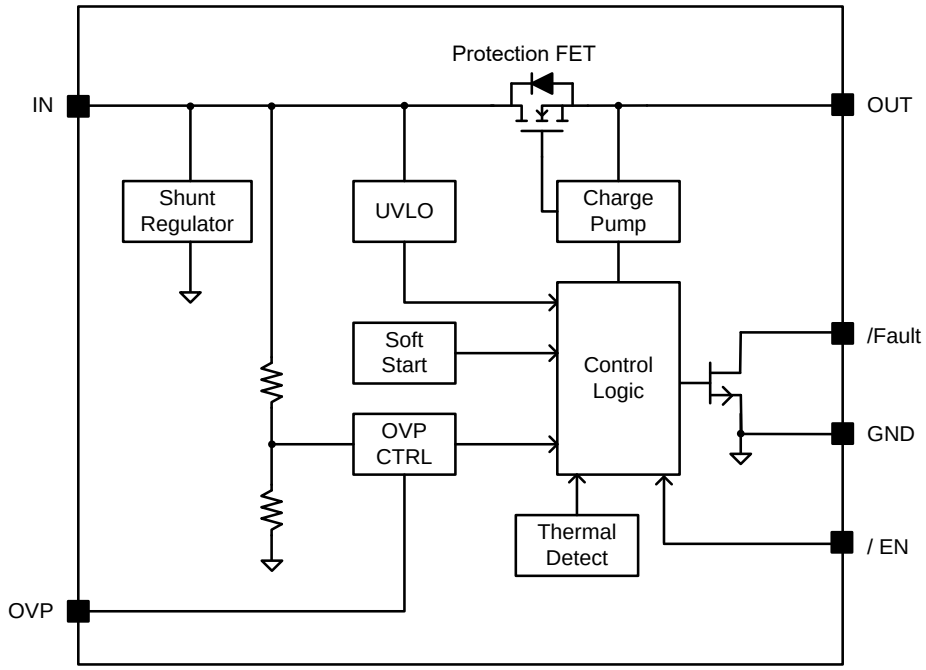


Figure2. Block Diagram

Absolute Maximum Ratings (Note 1)

IN, OVP, ---------- 29V
OUT ---------- IN + 0.3V
/Fault, /EN ---------- 29V
Continues IN, OUT Current ---------- 5A
Peak IN, OUT Current (10ms), ---------- 8A
Max Power Dissipation Under T_A=25°C ---------- 2.4W
Package Thermal Resistance (Note 2)
θ_{JA} ---------- 51.15°C/W
θ_{JC} ---------- 6.82°C/W
Junction Temperature Range ---------- 150°C
Lead Temperature (Soldering, 10 sec.) ---------- 260°C
Storage Temperature Range ---------- -65°C to 150°C

Recommended Operating Conditions (Note 3)

IN ---------- 2.5V to 28V
Junction Temperature Range ---------- -40°C to 125°C
Ambient Temperature Range ---------- -40°C to 85°C

Electrical Characteristics

(V_{IN} = 2.5V to 28V, C_{IN}=1μF, C_{OUT}=1μF, T_A = 25°C, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Shutdown Input Current	I_{SD}	V_{IN}=5V, /EN=5V, V_{OVP}=0V		3		μA
Input Voltage Range	V_{IN}		2.5		28	V
Input UVLO Threshold	V_{UVLO}				2.4	V
UVLO Hysteresis	V_{HYS}			0.1		V
Input Clamp Voltage	V_{INCLP}	I_{IN}=10mA		33		V
Bias Current	I_{BIAS}	V_{IN}=5V			100	μA
OVP Current	I_{OVP}	V_{OVP}=3V, V_{IN}=5V, V_{OUT}=0V			100	μA
Internal Default OVP Threshold	V_{OVPD}	Rising	6.5	6.75	7.0	V
		Falling	6.4			V
OVP Program Threshold	V_{OVPPT}		1.22	1.26	1.30	V
External OVP Select Threshold	V_{OVP_SELECT}			0.3	0.35	V
/EN High Threshold	V_{ENH}		1.2			V
/EN Low Threshold	V_{ENL}				0.4	V
Programmable OVP range	V_{OVPPR}		4		22	V
Resistance of power path	R_{PWPT}	V_{IN}=5V, I_{OUT}=200mA, from IN to OUT		32	39	mΩ
Output Load Capacitance	C_{OUT}	V_{IN}=5V			1000	μF
/Fault Low Voltage	V_{FAL}	V_{IN}=5V， I_{SINK}=1mA			0.4	V
/Fault Leakage Current	I_{FAL}	V_{IN}=5V，V_{FAL}=3.3V，/Fault high impedance			1	μA
Deglitch Time	t_{DG}	V_{IN}=5V, time from 2.5V<V_{IN}<V_{OVP} to V_{OUT}=10% of V_{IN}		12		ms
Switch Turn-On Time	t_{ON}	V_{IN}=5V, R_L=100, C_{OUT}=100μF; V_{OUT}=10% of V_{IN} to 90% V_{IN}		1.3		ms
Switch Turn-Off Time	t_{OFF}	V_{OVP}>1.2V to V_{OUT} stop rising		0.1		μs
Thermal Shutdown Temperature	T_{SD}			150		°C
Thermal Shutdown Hysteresis	T_{HYS}			20		°C

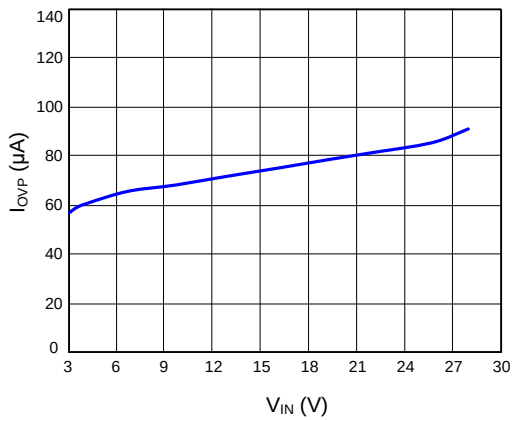
Note 1: Stresses beyond the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: θ_{JA} is measured in the natural convection at T_A = 25°C on Silergy test board.

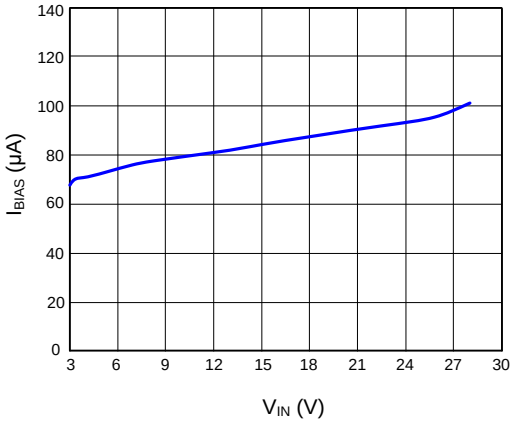
Note 3: The device is not guaranteed to function outside its operating conditions.

Typical Performance Characteristic

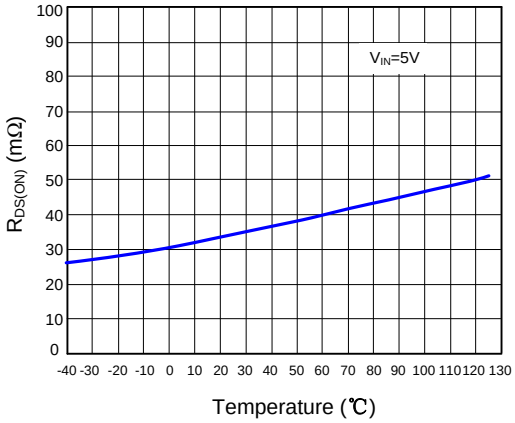
OVP Current vs. Input Voltage



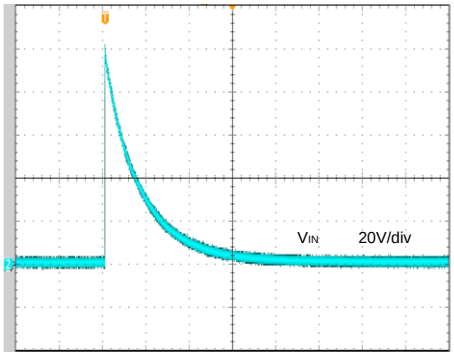
Bias Current vs. Input Voltage



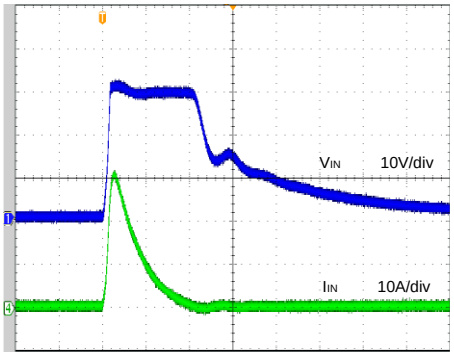
$R_{DS(ON)}$ vs. Temperature



100V Surge Test Waveform without SY6881

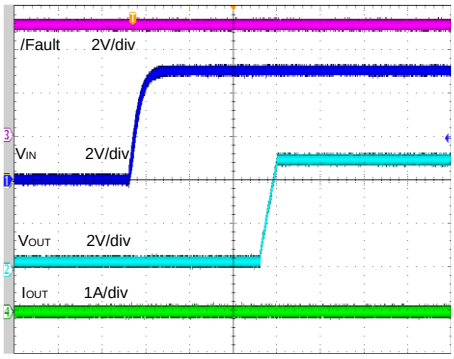


100V Surge Test Waveform with SY6881



Startup from V_{IN}

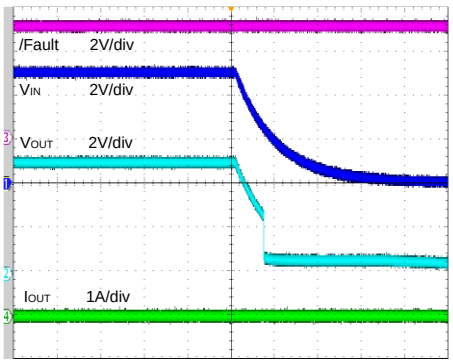
(V_{IN}=5V, Null Load)



Time (4ms/div)

Shutdown from V_{IN}

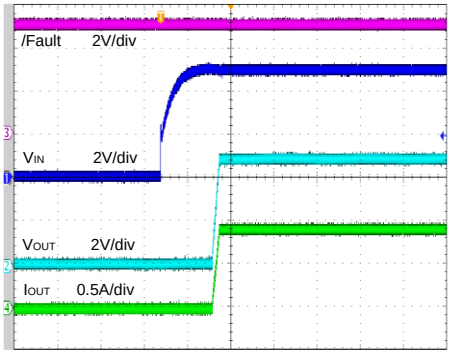
(V_{IN}=5V, Null Load)



Time (100ms/div)

Startup from V_{IN}

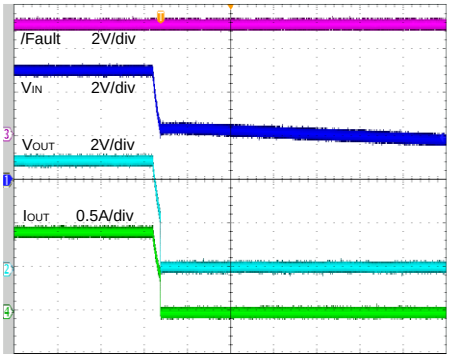
(V_{IN}=5V, I_{OUT}=1A)



Time (10ms/div)

Shutdown from V_{IN}

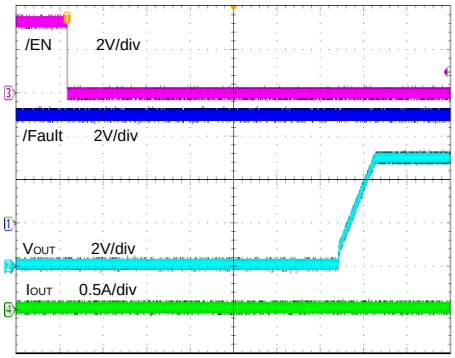
(V_{IN}=5V, I_{OUT}=1A)



Time (10ms/div)

Startup from /EN

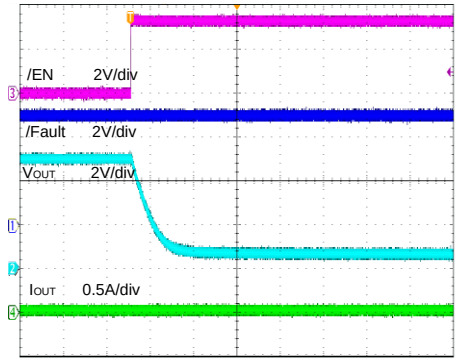
(V_{IN}=5V, Null Load)



Time (2ms/div)

Shutdown from /EN

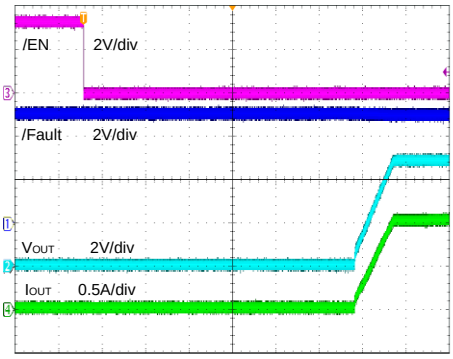
(V_{IN}=5V, Null Load)



Time (400μs/div)

Startup from /EN

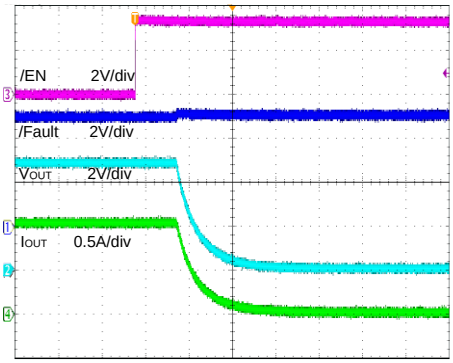
(VIN=5V, I_{OUT}=1A)



Time (2ms/div)

Shutdown from /EN

(V_{IN}=5V, I_{OUT}=1A)



Time (10μs/div)

Applications Information

Input Capacitor

For most applications, bypass V_{IN} to GND with a 1µF ceramic capacitor as close as possible to the device. If the power source has significant inductance due to long lead length, the device clamps the overshoot due to LC tank circuit.

Output Capacitor

The slow turn-on time provides a soft-start function that allows the SY6881 to charge an output capacitor up to 1000µF without turning off due to an over current condition when V_{IN}=5V.

Programmable OVP Adjustment Functionality

If OVP is connected to ground, the internal OVP comparator uses the internally set OVP value.

If an external resistor-divider is connected to OVP and V_{OVP} exceeds the External OVP Select Threshold, V_{OVP_SELECT}, the internal OVP comparator reads the IN fraction fixed by the external resistor divider. R1= 1MΩ is a good starting value for minimum current consumption.

Since V_{IN_OVP}, V_{OVPPT}, and R1 are known, R2 can be calculated from the following formula:

$$V_{IN\_OVP} = V_{OVPPT} \times \left(1 + \frac{R1}{R2}\right)$$

This external resistor-divider is completely independent from the internal resistor-divider.

On-The-Go(OTG) Functionality

During OTG operation, the SY6881 is initially disabled and the power FET's bulk diode is forward biased. The bulk diode represents ~0.7V drop across the device, which remains until the input voltage increases past 2.5V, when the device is fully enabled. While the device is disabled and the body diode is forward biased, the max DC current through the diode is 1.8A. This current is limited by the thermal performance of the device (0.7V×1.8A=1.36W). This current should be transient; the /EN pin must be pulled Low to ensure the device fully enables. The transient should not exceed the RC time constant of the input and output capacitors.

At the system level, over-voltage and current protection should be provided outside the SY6881.

PCB Layout Guide

For best performance of the SY6881, the following guidelines must be strictly followed:

1) Keep all power traces as short and wide as possible and use at least 2 ounce copper for all power traces (especially GND).

2) Place a ground plane under all circuitry to lower both resistance and inductance and improve DC and transient performance.

3) Locate the output capacitor as close to the connectors as possible to lower the impedance (mainly inductance) between the port and the capacitor and improve transient performance.

4) Input and output capacitors should be placed close to the IC and connected to the ground plane to reduce noise coupling.

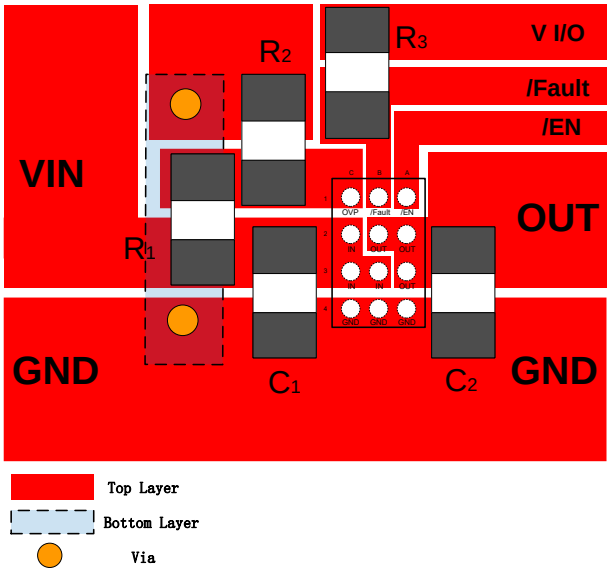
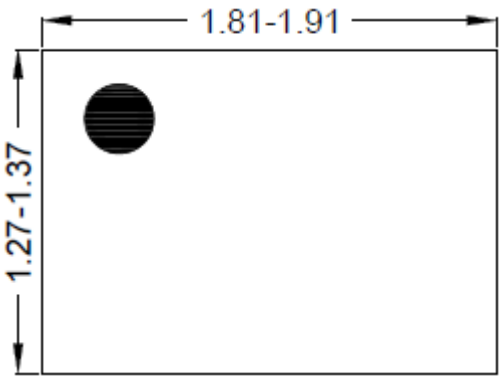
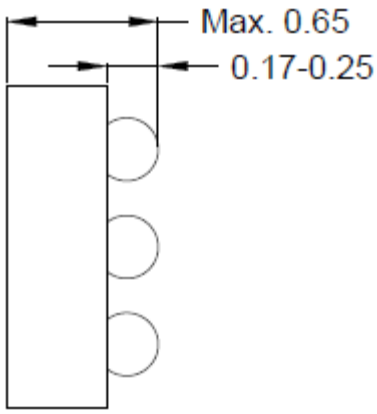


Figure3. PCB Layout Suggestion

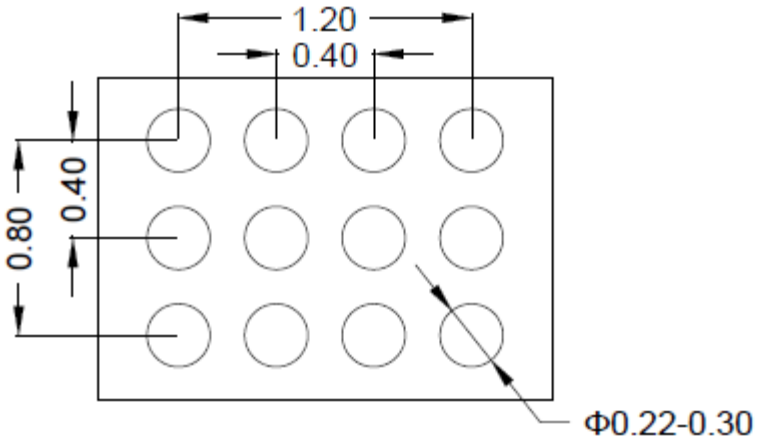
CSP1.32×1.86-12 Package Outline Drawing



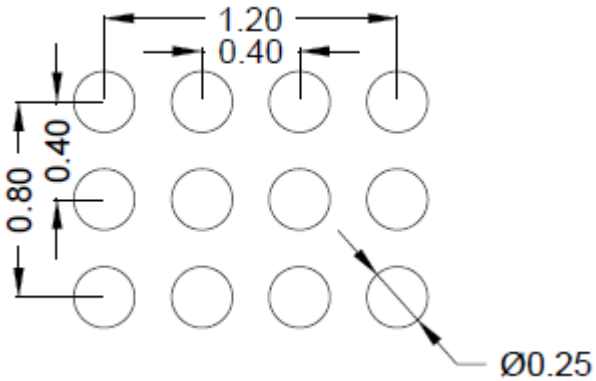
Top view



Side view



Bottom view



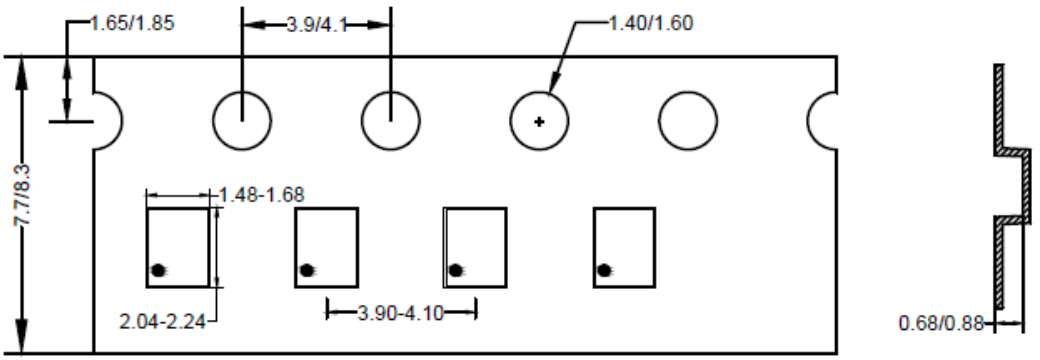
Recommended PCB layout (Reference only)

Notes: **All dimension in millimeter and exclude mold flash & metal burr.**

Taping & Reel Specification

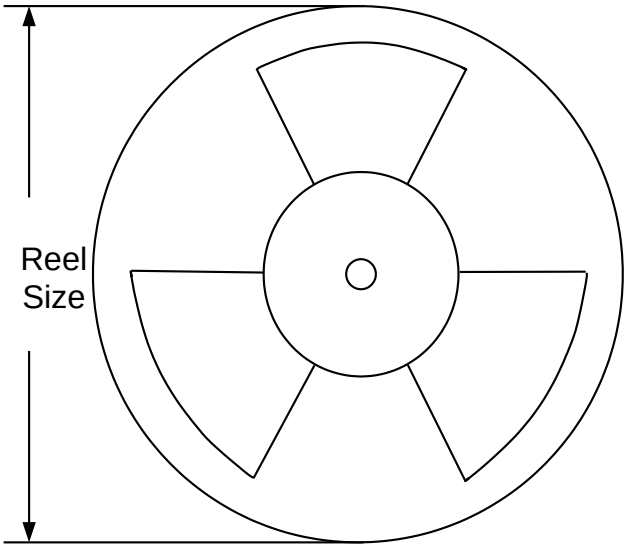
1. Taping orientation

CSP1.32×1.86



Feeding direction ⟶

2. Carrier Tape & Reel specification for packages



Package types	Tape width (mm)	Pocket pitch(mm)	Reel size (Inch)	Trailer length(mm)	Leader length (mm)	Qty per reel
CSP1.32×1.86	8	4	7"	400	160	3000

3. Others: NA

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