SY50272B

AC Input Buck Regulator

General Description

The SY50272B is an AC input Constant Voltage buck regulator. Its target applications are home appliances and auxiliary power supplies.

SY50272B integrates 650V MOSFET to decrease physical volume, adopts HV start-up circuit.

SY50272B adopts multi-off time control to realize quasi constant switching frequency and large duty cycle.
It uses peak current mode control and enters burst mode at light load to minimize power dissipation.

SY50272B include OCP, OVP and OTP functions.

Features

- 650V MOSFET Integrated
- High Voltage Start up Circuit Integrated
- 50mW No Load Power Consumption
- Multi-off Time Control
- Minimum External Components
- Over Temperature Protection(OTP)
- Output Over Voltage Protection(OVP)
- Compact Package: DIP8

Applications

- Home Appliances and White Goods
- Auxiliary Power Supplies

Recommended operating output power	
Products	V_{OUT}=12V (Open Frame)
SY50272B	4.3W

Typical Application

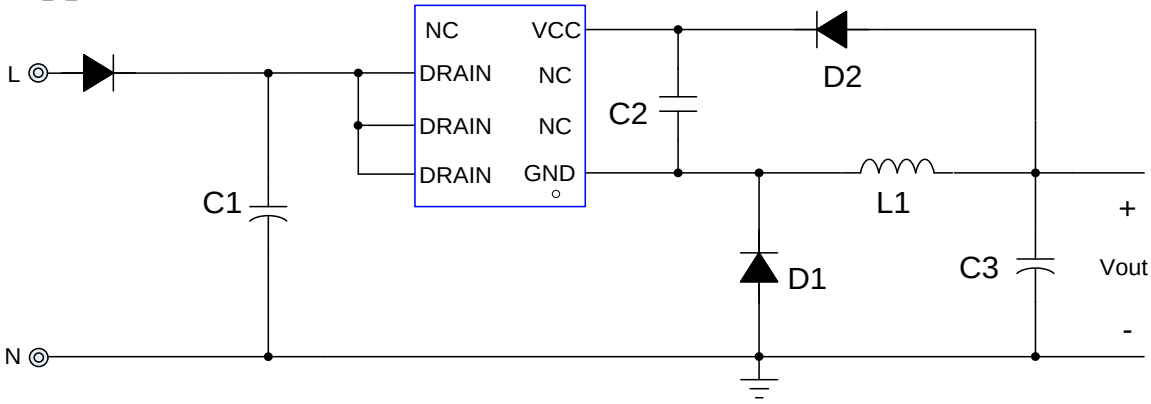
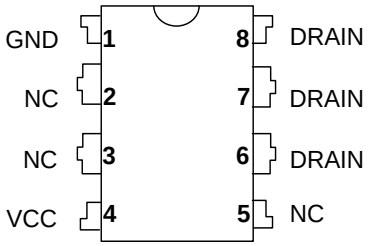


Fig.1 Typical Application Circuit

Ordering Information

SY50272□(□□)□
- Temperature Code
- Package Code
- Optional Spec Code



DIP8

Ordering Number	Package	Top Mark
SY50272BAGC	DIP8	CCYxyz

x=year code, y=week code, z= lot number code

Pinout (top view)

Pin number	Pin Name	Pin Description
1	GND	IC ground pin.
2.3	NC	No connection.
4	VCC	Power supply pin and voltage sense pin. Connect a ceramic capacitor between VCC and GND pin.
5	NC	No connection.
6.7.8	DRAIN	Internal power MOSFET drain pin.

Absolute Maximum Ratings (Note 1)

VCC ---------- -0.3V~20V
DRAIN ---------- 650V
DRAIN Pulse Current (Pulse=100us) ----------1.6A
Power Dissipation, @ T_A = 25°C DIP8 ---------- 1.5W
Package Thermal Resistance (Note 2)
DIP8, θ_{JA} ---------- 83°C/W
DIP8, θ_{JC} ---------- 36°C/W
Maximum Junction Temperature ---------- 150°C
Lead Temperature (Soldering, 10 sec.) ---------- 260°C
Storage Temperature Range ---------- -65°C to 150°C

Recommended Operating Conditions

VCC ---------- 12V
Junction Temperature Range ---------- -40°C to 125°C
Ambient Temperature Range ---------- -40°C to 85°C

Electrical Characteristics

(T_A = 25°C unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Power Supply Section						
VCC Turn-on Threshold	V_{VCC_ON}		10.4	11	11.6	V
VCC Turn-off Threshold	V_{VCC_OFF}		5	5.5	6	V
HV Current Source Enable Threshold	V_{VCC_MIN}			V_{VCC_OFF}+1		V
Start up Current	I_{CHARGE}		1.4	1.8	2.2	mA
Operating Current	I_{VCC}	V_{IN}=373V,I_{OUT}=0.3A,L=600μH		2		mA
Quiescent Current	I_Q	V_{VCC}=13V	300	440	560	μA
Current Sense Section						
Current Limit	I_{ISEN_LIM}		0.61	0.72	0.83	A
V_{VCC} Control Section						
VCC OVP Voltage Threshold	V_{VCC_OVP}		14	14.6	15.2	V
VCC Voltage Reference	V_{VCC_REF}		11.64	12	12.36	V
Integrated MOSFET Section						
BV of HV MOSFET	V_{BV}	V_{GS}=0V, I_{DS}=250μA	650			V
MOSFET on Resistance	R_{ON}	V_{GS}=10V, I_{DS}=0.5A		11.5		Ω
Driver Section						
Max ON Time	T_{ON_MAX}		16	24	32	μs
Min ON Time	T_{ON_MIN}			350		ns
Oscillator Section						
Normal Frequency	F_{Normal}	V_{IN}=127V,I_{OUT}=0.3A,L=600μH		37		kHz
		V_{IN}=373V,I_{OUT}=0.3A,L=600μH		39		kHz
Thermal Section						
Thermal Shutdown Temperature	T_{SD}			150		°C

Note 1: Stresses beyond the "Absolute Maximum Ratings" may cause perm anent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: θ_{JA} is measured in the natural convection at T_A = 25°C on a low effective single layer thermal conductivity test board of JEDEC 51-3 thermal measurement standard. Test condition: Device mounted on 2" x 2" FR-4 substrate PCB, 2oz copper, with minimum recommended pad on top layer and thermal vias to bottom layer ground plan

Block Diagram

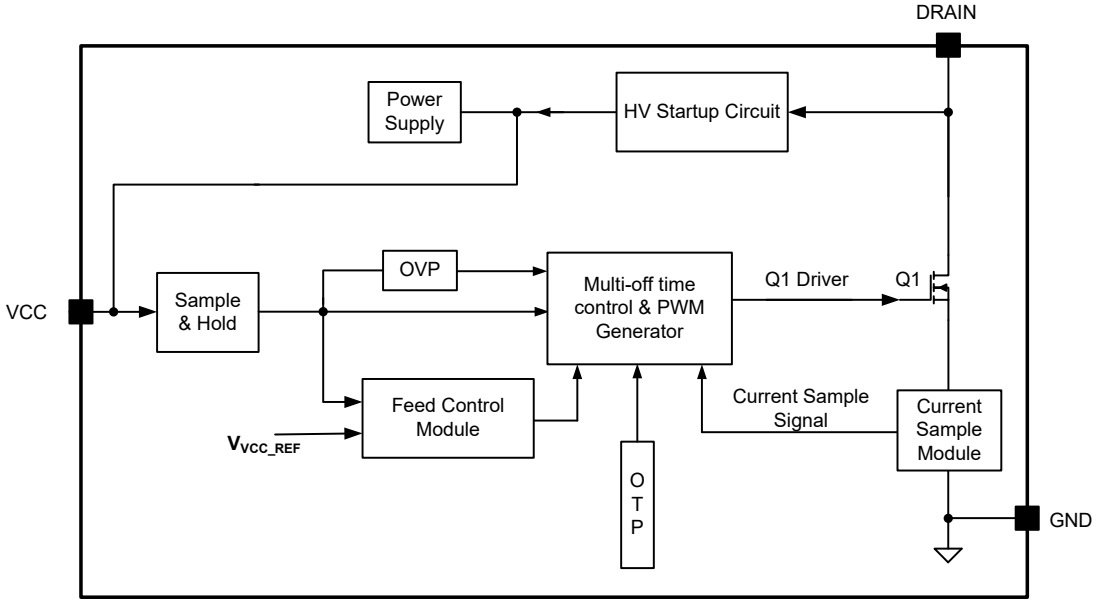


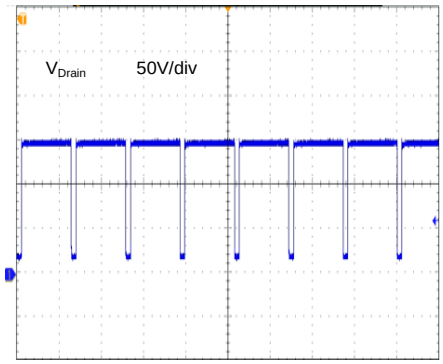
Fig.2 Block diagram

Typical Performance Characteristics

(Test condition: input voltage: 90~264Vac; output spec: 12Vdc_0.36A; Ambient temperature: 25±5 ℃; Ambient humidity: 65±25 %.)

Steady States

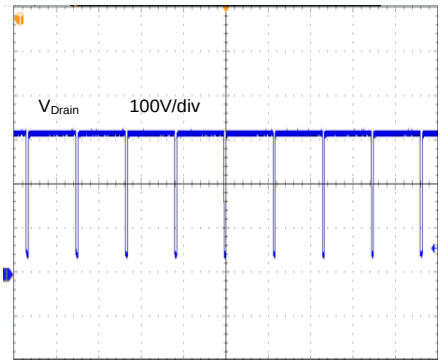
(V_{IN}=115$V_{(AC)}$, full load)



Time (20μs/div)

Steady States

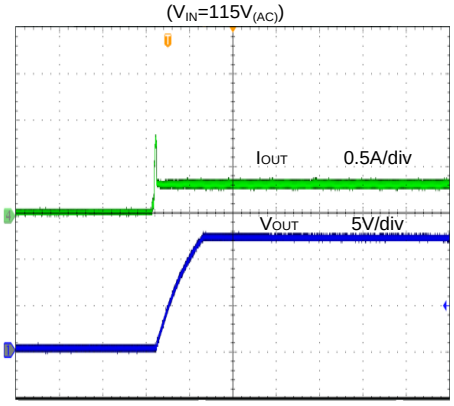
(V_{IN}=230$_{(AC)}$, full load)



Time (20μs/div)

Startup

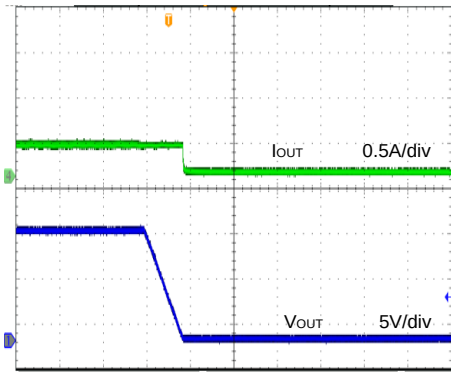
(V_{IN}=115$V_{(AC)}$)



Time (20ms/div)

Shutdown

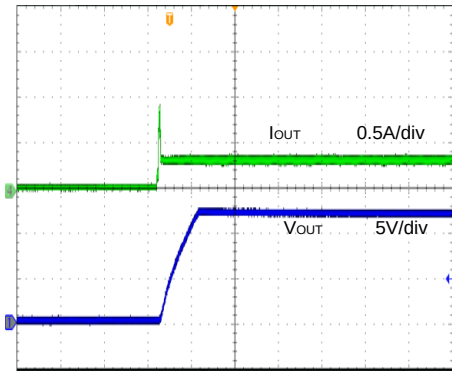
(V_{IN}=115$V_{(AC)}$)



Time (20ms/div)

Startup

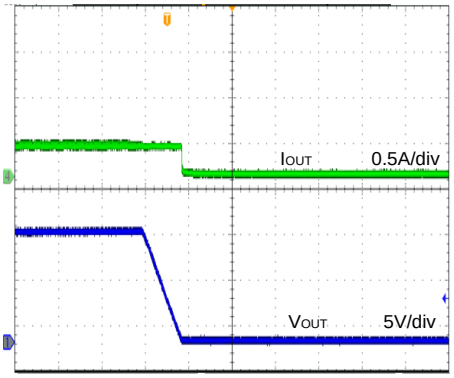
(V_{IN}=230$V_{(AC)}$)



Time (20ms/div)

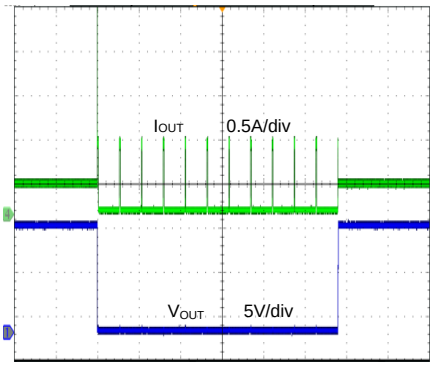
Shutdown

(V_{IN}=230$V_{(AC)}$)



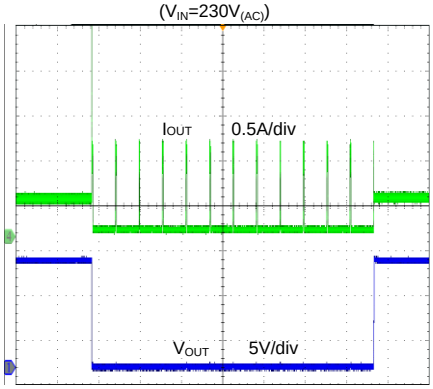
Time (20ms/div)

Short Circuit Protection
(V_{IN}=115$V_{(AC)}$)



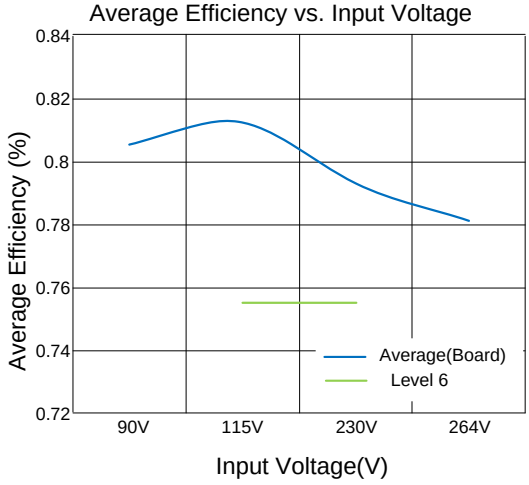
Time (1s/div)

Short Circuit Protection
(V_{IN}=230$V_{(AC)}$)



Time (1s/div)

Average Efficiency vs. Input Voltage



Operation Principles

Start-up Operation and Under Voltage Lockout

After AC supply is powered on, the rectified BUS voltage ramps up. The capacitor across VCC and GND pins, C_{VCC}, is charged up by the BUS voltage through a internal HV startup circuit. When VCC voltage reaches V_{VCC_ON}, the IC starts switching and the internal high voltage regulator turns off.

The IC stops switching when the V_{VCC} drops blow V_{VCC_MIN}. To reduce the power loss under short circuit condition, SY50272B adopts the smart UVLO strategy. A digital counter is adopted to slow down the restart frequency. If V_{VCC} drop to V_{VCC_MIN}, the internal PWM switching is stop, UVLO flag signal will be set and V_{VCC} will be charged to V_{VCC_ON} again by HV current source. When V_{VCC} has reached V_{VCC_MIN}, the counter will plus 1. Initial number of the counter is 0, and when the counter has reached number 4, UVLO flag signal will be reset, then the V_{VCC} drop to V_{VCC_OFF}. Meanwhile, IC will try to start up with soft start process. The timing diagram is shown as Fig.3.

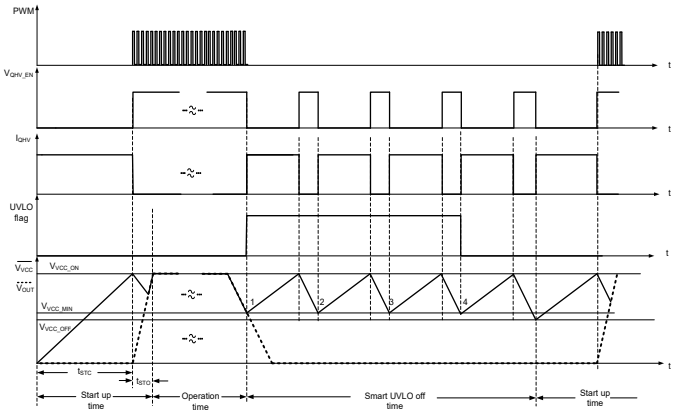


Fig.3 timing diagram of startup and UVLO off

Output Voltage Sample

SY50272B samples the V_{OUT} by V_{Dmain} and $V_{Dsample}$. The relationship between V_{VCC} and V_{OUT} can be described as: $V_{VCC} = V_{OUT} + V_{Dmain} - V_{Dsample}$

V_{OUT} is the output voltage, V_{Dmain} is the forward voltage drop of the main power diode, $V_{Dsample}$ is the forward voltage drop of the sample diode. The circuit diagram of output voltage feedback is shown in Fig.4.

Generally, forward voltage drop varies with forward current. So V_{Dmain} varies with load current, but $V_{Dsample}$ keeps constant when load current varies, as a result, V_{VCC} cannot precisely represent V_{OUT}. So SY50272B adopts a internal compensated strategy to optimize the load regulation of V_{OUT}.

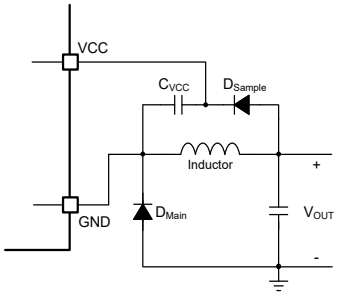


Fig. 4 circuit diagram of output voltage sample

Multi-off time control(MOT)

SY50272B adopts multi-off time control to achieve quasi constant switching frequency and large duty cycle. Multi-off time control is consist of fix off time control and multi-state control.

The fix off time of PWM is decided by a current source I_t, a capacitor and the reference.

To ensure the switching frequency of circuit is between 28k and 42k, and max duty cycle is above 0.6, multi-state control strategy is adopted. When the Ton varies, the Toff is changed. The logic diagram is shown in Fig.5.

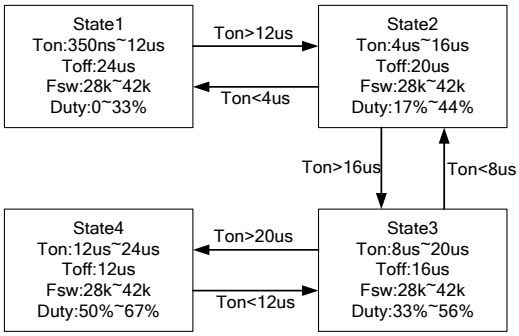


Fig.5 logic diagram of multi-state control

Sleep Mode in Light Load

To improve the light load efficiency, the burst mode control is adopted in SY50272B.
As load decreases, the peak current of MOSFET I_{PK} will decrease as well. When I_{PK} falls below a threshold current represented by I_{SLEEP_IN}(typical 1/6 times of I_{ISEN_LIM}), IC will enter sleep mode. Under sleep mode, IC will shut down most of internal circuit to further reduce power consumption by IC.

Due to the closed loop control, I_{PK} will rise again. When I_{PK} rises above a threshold current represented by I_{SLEEP_EXIT}(typical 1/5 times of I_{ISEN_LIM}), IC will exit sleep mode, and resume PWM switching again. The threshold current I_{SLEEP_EXIT} is a little higher than I_{SLEEP_IN}.

To optimize the over voltage protection, the minimum switching frequency will be reduced to 1k, and the peak current will be reduced to I_{SLEEP_IN}. The timing diagram of burst mode is shown in Fig.6.

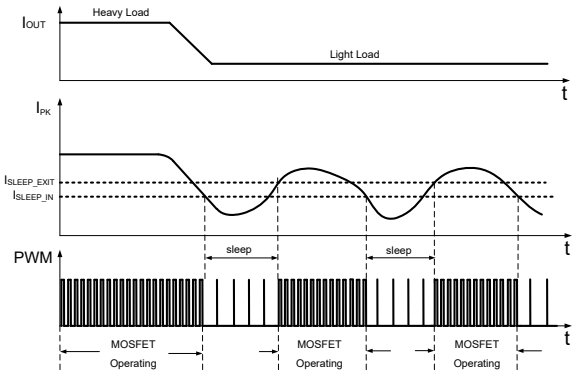


Fig.6 timing diagram of burst mode

Over Current Protection (OCP)

As the circuit operate at start up condition or output short condition, and the output voltage is shorted to zero. When the MOSFET conduct, the inductor current will rise $\Delta I_1 = \frac{(V_{IN} - 0) * t_{ON}}{L}$ in a switching period, when the power diode conduct, the inductor current will fall $\Delta I_2 = \frac{(V_{D\_F} + 0) * t_{OFF}}{L}$ in a switching period. If the current rise value ΔI_1 is larger than current fall value ΔI_2, the current will rise and the inductor will be statured, then the circuit will be damaged.

V_{IN} is the input voltage, t_{ON} is MOSFET conducting time, V_{D_F} is the forward voltage drop of power diode, t_{ON} is power diode conducting time. L is inductor value.

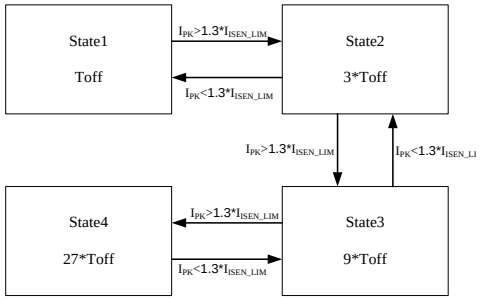


Fig. 7 logic diagram of over current protection

To resolve the problem, the OCP strategy is adopted. When peak current of MOSFET I_{PK} exceeds OCP current threshold (typical 1.3times of I_{ISEN_LIM}), the off time will be changed to 3 times of previous off time. The logic diagram is shown in Fig.7.

At start up condition, when I_{PK} exceeds OCP current threshold, the timing diagram of inductor current is shown in Fig.8.

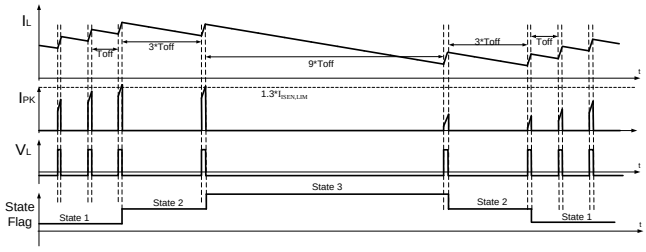


Fig. 8 timing diagram of inductor current

Over Voltage Protection (OVP)

SY50272B will monitor the V_{VCC}, if the V_{VCC} is above V_{VCC_OVP}, IC will shut down the gate pulse till IC restart.

Over Temperature Protection (OTP)

To prevent any thermal damage, SY50272B shuts down switching when its junction temperature exceed T_{SD}. When the junction temperature drops T_{OTP_HYS}, IC will restart.

Power design

Typical application specification:

Products	Input range	Output	Temperature rise
SY50272B	90Vac~264Vac	12V/0.3A	41℃
	90Vac~264Vac	12V/0.36A	56℃

The test is operated in natural cooling condition at 25 ℃ ambient temperature.

Inductor Design Considerations

The design rules are as followed:

(a) Compute inductor value L

Consider the thermal performance during all input range, define the ripple coefficient of inductor current as 133%.

I_{OUT}=0.36A , then $\Delta I=1.33*I_{OUT}$=0.48A

In the range, the IC operation in state1 of MOT in most periods, then the T_{OFF} is 24uS.

$$L=\frac{12V*24\mu}{0.48A}=600\mu$$

(b) Compute maximum current of inductor

Because of the OCP function, the maximum current of inductor will be limited to 1.3times of I_{ISEN_LIM}. So the saturation current of inductor should be designed as below:

$I_{MAX}=1.3*I_{ISEN\_LIM}=1.3*0.72A=0.963A$

(c) Preset the maximum magnetic flux ΔB

$\Delta B=0.3T$

(d) Compute turns N

$$N=\frac{L*I_{MAX}}{A_e*\Delta B}=\frac{600\mu*0.963A}{A_e*0.3}$$

A_e is the cross sectional area of core. Once the A_e is confirmed, the turns of inductor winding can be calculated.

Layout Considerations

(a) To achieve a good EMI performance and to reduce the line frequency voltage ripples, the output of the bridge rectifier should be connected to the BUS line capacitor first, then to the switching circuit.

(b) The circuit loop of all switching circuit should be kept as small as possible, which include: bus cap, SY50272B, power diode, inductor and output cap.

(c) The circuit loop of power supply should be kept as small as possible. The bias supply capacitor should be close to the VCC pin.

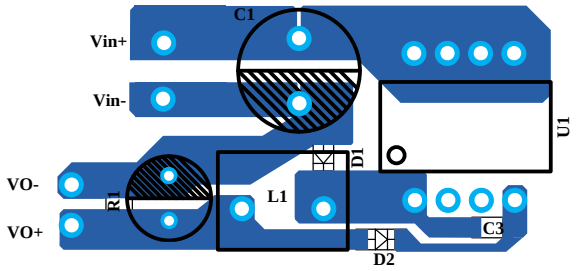


Fig.9 Layout example of Key Part

Figure 10 shows a typical application example of 12V, 360mA non-isolated power supply using.

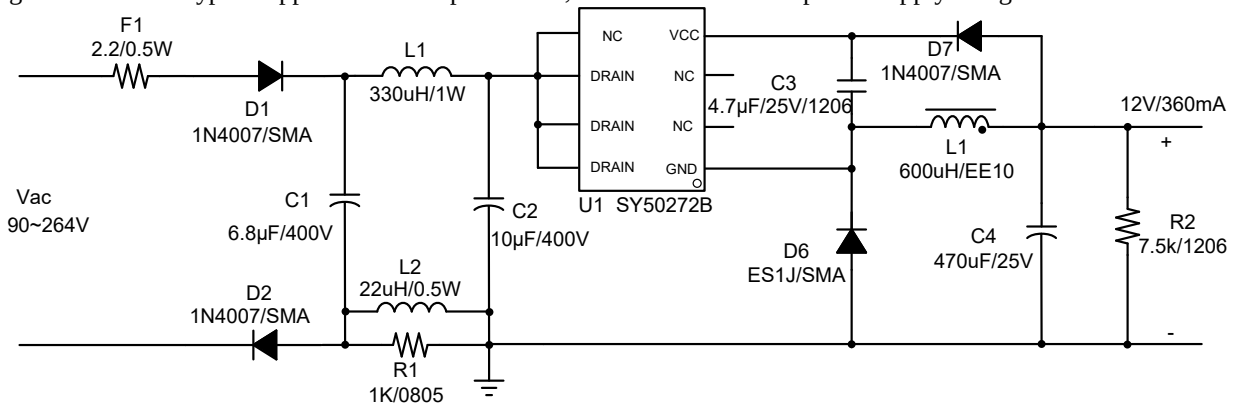
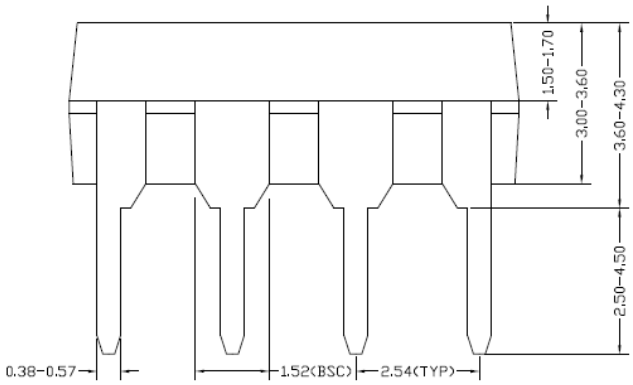


Figure 10 Typical Application at 12V, 360mA

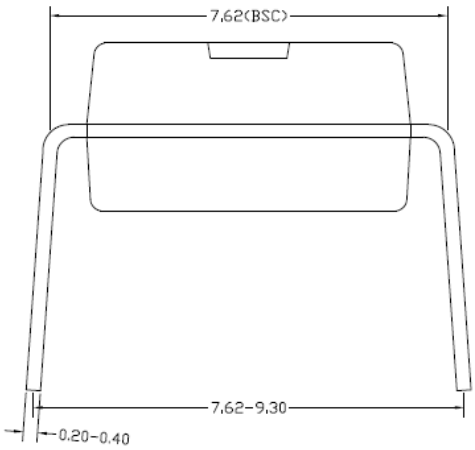
Design Notice

1. The ES1J is recommended to use for power diode.
2. To achieve better startup and sampling performance, the 4.7uF capacitor value is recommended for VCC cap.
3. To optimize the thermal performance, the pin5 of SY50272B could be connected to pin6~8.
4. To simplify the layout, the pin 2/pin 3 could be connected to pin1 or pin4.

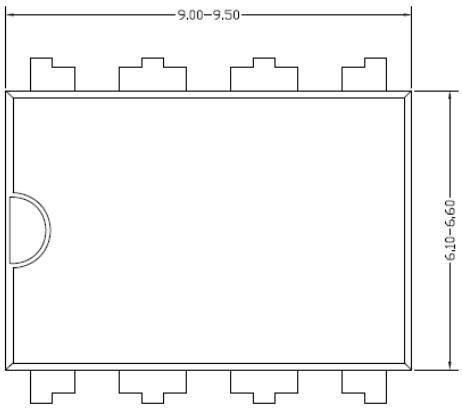
DIP8 Package Outline



Side view A



Side view B



Top view

Notes: **All dimension in millimeters and exclude mold flash & metal burr**

Revision History

The revision history provided is for informational purpose only and is believed to be accurate, however, not warranted. Please make sure that you have the latest revision.

Date	Revision	Change
September 5, 2023	Revision 0.9B	Update the Ron.
September1st, 2020	Revision 0.9A	Page8: Temperature rise revise.
December 31,2019	Revision 0.9	Initial Release

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