# SY5040

## CCM+QR Mode SSR Flyback Controller

## General Description

The SY5040 is a peak current mode SSR Flyback controller that combines CCM and QR mode together to minimize transformer size and achieve high efficiency. Under low line and heavy load condition, the SY5040 works under CCM, while under high line or medium load condition, it works under QR mode (valley switching). The SY5040 adopts frequency fold-back control when the load decreases to achieve the high average efficiency. When the load decreases to very light level, the SY5040 will enter burst mode and the switching frequency is fixed to 25kHz to avoid audible noise.

The SY5040 also provides comprehensive and reliable protections including brownout protection, output OVP, external OTP, OLP, VCC OVP, internal OTP, etc.

The SY5040 is available with a compact SOT23-6 package.

## Features

- Rated Switching Frequency: 65kHz
- CCM+QR Combined Operating Mode
- Frequency Fold Back and Burst Mode Control
- Minimum Switching Frequency Limited to 25kHz
- $F_{SW}$ Modulation to Reduce EMI Noise
- Programmable Brownout Protection by ZCS Pin
- Programmable Output OVP by ZCS Pin
- Programmable External OTP by CS Pin
- OLP, VCC OVP, Internal OTP
- Secondary Diode Short Circuit Protection
- OCP Compensation over Universal Input Range
- Low Start up Current: <4μA
- Gate Drive Capability: 210mA/420mA(source/sink)
- Internal Soft Start Process
- RoHS Compliant and Halogen Free
- Compact Package: SOT23-6

## Applications

- AC/DC Power Supply
- Note Book Adapter
- LCD TV
- Auxiliary Power Supply

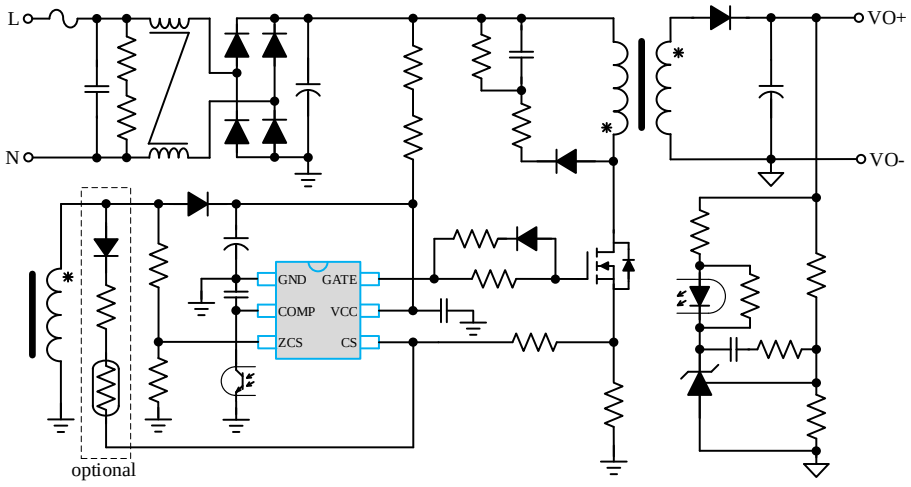


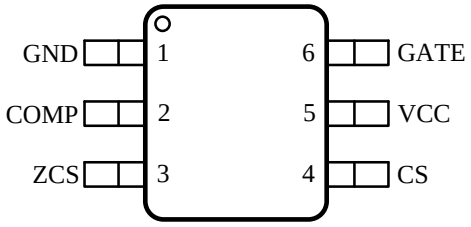

*Fig. 1. Typical Application Circuit*

## Ordering Information

| Ordering Part Number | Package type | Top Mark |
|---|---|---|
| SY5040ABC | SOT23-6 RoHS-Compliant and Halogen-Free | Ya xyz |

***x = year code, y = week code, z = lot number code***

## Pinout (top view)




## Pin Description

| Pin No | Pin Name | Pin Description |
|---|---|---|
| 1 | GND | Ground pin |
| 2 | COMP | This pin is connected to an opto-coupler for output voltage feed back |
| 3 | ZCS | Multi-function including valley detecting, brownout protection and output OVP |
| 4 | CS | Primary peak current sense pin, also used for external OTP |
| 5 | VCC | Power supply pin |
| 6 | GATE | Gate drive pin |

## Block Diagram

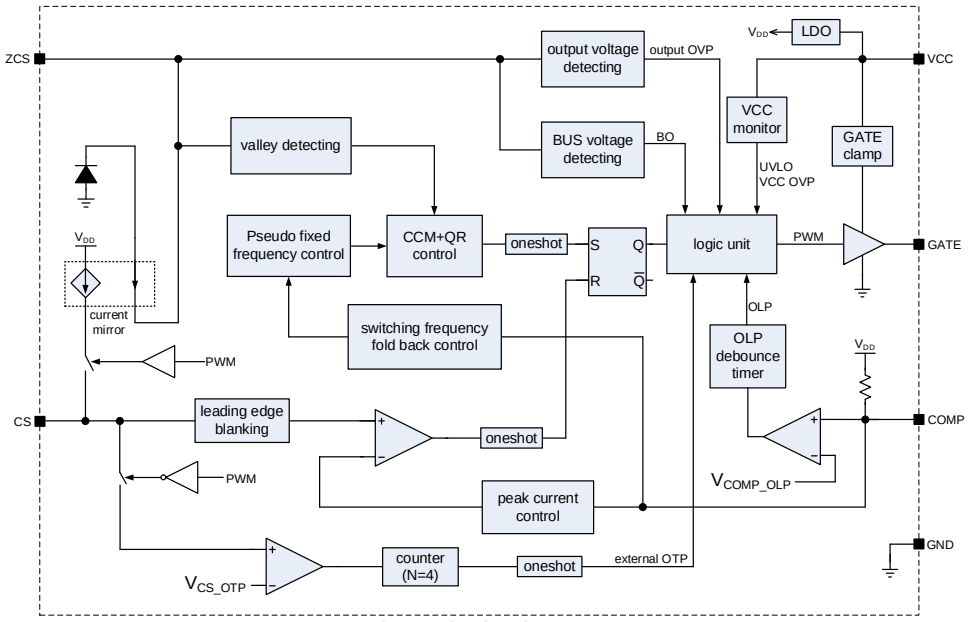



*Fig.2 Block Diagram*

## Absolute Maximum Ratings

| Parameter (Note 1) | Min | Max | Unit |
|---|---|---|---|
| VCC | -0.3 | 34 | V |
| GATE | -0.3 | 15 | |
| CS, COMP, ZCS | -0.3 | 3.6 | |
| Supply Current $I_{VCC}$ | | 20 | mA |
| Junction Temperature, Operating | -45 | 150 | °C |
| Lead Temperature (Soldering, 10 sec.) | | 260 | |
| Storage Temperature Range | -65 | 150 | |
| Dynamic CS Negative Current in 1us Duratio | | -2 | mA |
| Dynamic CS Negative Voltage in 1us Duration | | -0.7 | V |
| Dynamic ZCS Negative Current in 20us Duration | | -2 | mA |
| Dynamic ZCS Negative Voltage in 20us Duration | | -0.7 | V |

## Thermal Information

| Parameter (Note 2) | Min | Max | Unit |
|---|---|---|---|
| $\theta_{JA}$ Junction-to-ambient Thermal Resistance | | 125 | °C/W |
| $\theta_{JC}$ Junction-to-case Thermal Resistance | | 60 | |
| PD Power Dissipation TA = 25°C | | 1.1 | W |

## Recommended Operating Conditions

| Parameter | Min | Max | Unit |
|---|---|---|---|
| VCC | 12 | 27 | V |
| Junction Temperature Range | -40 | 125 | °C |
| Ambient Temperature Range | -40 | 105 | °C |

## Electrical Characteristics

($V_{VCC}$ = 12V (Note 3), $T_A$ = 25°C unless otherwise specified)

| Parameter | | Symbol | Test Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| VCC Pin | Turn-on Threshold | $V_{VCC\_ON}$ | | 20 | 21.5 | 23 | V |
| | Turn-off Threshold | $V_{VCC\_OFF}$ | | 8 | 9 | 10 | V |
| | OVP Threshold | $V_{VCC\_OVP}$ | | 27.7 | 29.7 | 31.7 | V |
| | Current Sink under Over Voltage Condition | $I_{VCC\_OVP}$ | $V_{VCC}$=$V_{CC\_OVP}$+0.1V | | 11 | | mA |
| | Start Up Current | $I_{VCC\_ST}$ | $V_{VCC}$=18V | | 2.6 | 4 | μA |
| | Operating Current | $I_{VCC\_OPT}$ | $C_L$=1nF, $F_{SW}$=65kHz | | 1.9 | | mA |
| | Quiescent Current | $I_{VCC\_Q}$ | Under sleep mode | | 200 | 270 | μA |
| | Current Sink under Fault Condition | $I_{VCC\_FAULT}$ | | 0.8 | 1 | 1.3 | mA |
| CS Pin | Maximum Peak Current Sense Voltage | $V_{CS\_MAX}$ | | 0.92 | 0.97 | 1.03 | V |
| | Primary OCP Threshold | $V_{CS\_OCP}$ | | 1.24 | 1.31 | 1.38 | V |
| | Leading Edge Blanking Time | $T_{CS\_LEB}$ | | | 470 | | ns |
| | External OTP Threshold | $V_{CS\_OTP}$ | | 0.94 | 1 | 1.06 | V |
| | OCP Compensation Current | $I_{CS\_OCPC}$ | $I_{ZCS}$=500μA | 90 | 105 | 120 | μA |
| | | | $I_{ZCS}$=400μA | | 90 | | μA |
| | | | $I_{ZCS}$=300μA | | 64 | | μA |
| | | | $I_{ZCS}$=200μA | | 36 | | μA |
| | CS Pin Short Circuit Protection Threshold | $V_{CS\_SCP}$ | | | 100 | | mV |
| | CS Pin Short Circuit Detecting Blanking Time | $T_{CS\_SCP\_BLK}$ | | | 3.5 | | μs |
| ZCS Pin | Output OVP Threshold | $V_{ZCS\_OVP}$ | | 1.9 | 2 | 2.1 | V |
| | Blanking Time for $V_{OUT}$ Sense after $V_{GATE}$ Jumps from High to Low | $T_{VOSEN\_BLK}$ | | 1.6 | 2.6 | 3.6 | μs |
| | Brown Out Threshold Current | $I_{BO}$ | | 90 | 100 | 110 | μA |
| | Hysteresis for Brown In | $I_{BO\_HYS}$ | | | 10 | | μA |
| | Brown Out Debounce Time | $T_{BO\_DBC}$ | | 55 | 90 | 125 | ms |
| Switching Frequency | Rated Switching Frequency | $F_{SW\_RATE}$ | | 60 | 65 | 70 | kHz |
| | Minimum Switching Frequency | $F_{SW\_MIN}$ | | 20 | 25 | 30 | kHz |
| | Frequency Modulation Amplitude | $F_{SWMOD\_AMP}$ | $V_{COMP}$=1.8V, CCM | | ±6.5 | | kHz |
| | Frequency Modulation Period | $T_{SWMOD}$ | | | 4 | | ms |
| COMP | Internal Pull-up Voltage | $V_{COMP\_PU}$ | | | 2.7 | | V |
| | Internal Pull-up Resistor | $R_{COMP\_PU}$ | | | 20 | | kΩ |

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| COMP | Threshold to Enter Sleep Mode | $V_{COMP\_INSLEEP}$ | $V_{COMP}$ falling down | 0.25 | 0.3 | 0.35 | V |
| | Threshold to Exit Sleep Mode | $V_{COMP\_EXSLEEP}$ | $V_{COMP}$ rising up | 0.37 | 0.42 | 0.47 | V |
| | OLP Threshold | $V_{COMP\_OLP}$ | | 2.0 | 2.25 | 2.5 | V |
| | OLP Debounce Time | $T_{OLP\_DBC}$ | | 55 | 90 | 125 | ms |
| GATE Pin | Gate Clamp Voltage | $V_{GATE\_CLAMP}$ | $V_{VCC}$=20V | | 14 | | V |
| | Maximum Source Current | $I_{SOURCE\_MAX}$ | $C_L$=10nF | | 210 | | mA |
| | Maximum Sink Current | $I_{SINK\_MAX}$ | $C_L$=10nF | | 420 | | mA |
| | Maximum ON Time | $T_{ON\_MAX}$ | | | 13 | | μs |
| Internal OTP | Internal OTP Threshold | $T_{OTP}$ | | | 140 | | °C |
| | Hysteresis | $T_{HYS}$ | | | 15 | | °C |
| Soft Start | Soft Start Time | $T_{SS}$ | | | 7 | | ms |

**Note 1**: Stresses beyond the “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

**Note 2**: $\theta_{JA}$ is measured in the natural convection at $T_A$ = 25°C on a low effective single layer thermal conductivity test board of JEDEC 51-3 thermal measurement standard. Test condition: Device mounted on “2 x 2” FR-4 substrate PCB, 2oz copper, with minimum recommended pad on top layer and thermal via to bottom layer ground plane.

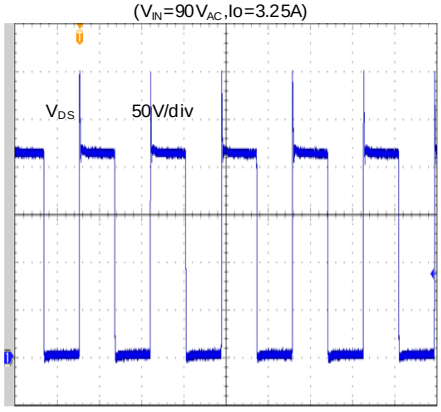
**Note 3**: Increase VCC pin voltage gradually higher than $V_{VCC\_ON}$ voltage then turn down to 12V.

# Typical Performance Characteristics

(Test condition: $V_{IN}$: 90~264Vac; output spec: 20Vdc_3.25A; output cable: 18AWG_1.8m; $T_A$=25±5 ℃)

Steady States

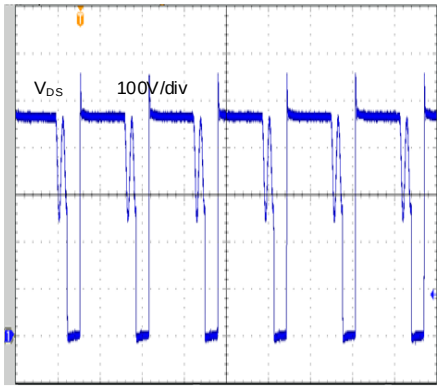
($V_{IN}$=90$V_{AC}$,Io=3.25A)




Time (10μs/div)

Steady States

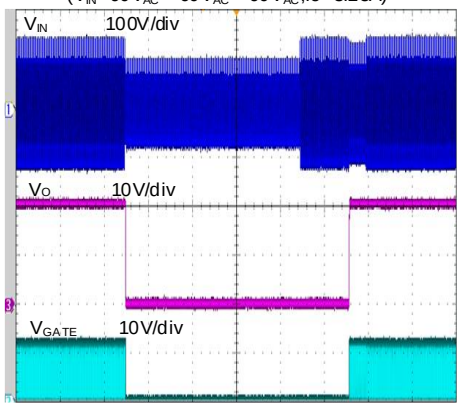
($V_{IN}$=264$V_{AC}$,Io=3.25A)




Time (10μs/div)

Brown Out Protection

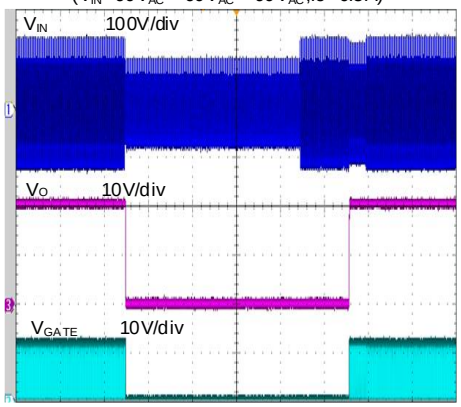
($V_{IN}$=90$V_{AC}$→60$V_{AC}$→90$V_{AC}$,Io=3.25A)




Time (1s/div)

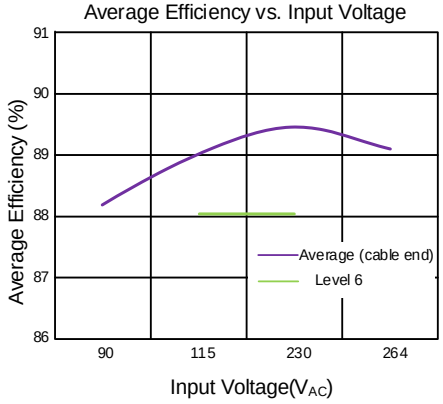
Brown Out Protection

($V_{IN}$=90$V_{AC}$→60$V_{AC}$→90$V_{AC}$,Io=0.5A)




Time (1s/div)

Average Efficiency vs. Input Voltage



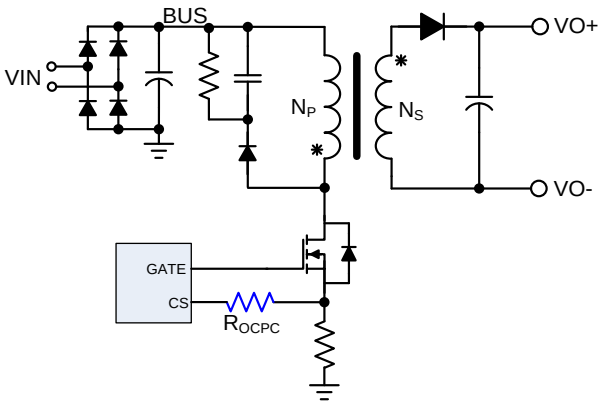
# Detailed Description

## CCM+QR Operating Principle

The SY5040 adopts the mixed control method that combines CCM and QR mode together. Under low input voltage and heavy load condition, it will operate under CCM. Under high input voltage or medium load condition, it will operate under QR mode. Due to this control method, the optimized efficiency and transformer size can be achieved.

## OCP Compensation

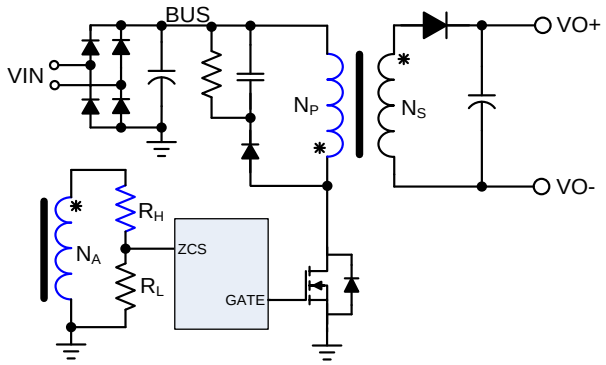
Generally, OCP level under low input voltage condition is lower than that under high input voltage condition. The SY5040 adopts OCP compensation function to make the variation of OCP level over universal input voltage range to be smaller. The compensation is achieved by adding a resistor $R_{OCPC}$ between CS pin and peak current sense resistor. The larger $R_{OCPC}$ is, the lower OCP level under high input voltage will be. This compensation resistor $R_{OCPC}$ will be adjusted by customers for their specified power converter design.




## Programmable Brown Out Protection

The SY5040 will sense the BUS voltage by ZCS pin and programmable brown out protection can be achieved. When the primary side power MOS is turned on, the ZCS pin will be internal clamped to 0V, since the voltage on auxiliary winding (negative) is proportional to BUS voltage, the current flow out of ZCS pin will be proportional to BUS voltage. The SY5040 will compare the current flow out of ZCS pin with an internal reference current (typical 100uA), if the current flow out of ZCS pin is lower than the reference current, a timer will begin to count, and when the timer elapse, brown out protection will be triggered, the IC will stop switching and enter auto-recovery mode. During the Vin start-up, when the VCC rises to $V_{CC\_ON}$ threshold, the GATE pin will turn on primary MOS for a short duration (~2us) and the IC will identify if the input voltage is above brown in level (110uA). Only when brown in condition is meet, the IC will start normal operating, otherwise, the IC will stop switching and enter auto-recovery mode. The upper resistor of the ZCS pin resistor divider which is connected between auxiliary winding will set input brown out protection level. Input voltage brown out level (RMS) is calculated as below equation:

$$V_{IN\_BO} = \frac{I_{BO}}{\sqrt{2}} \cdot \frac{N_P}{N_A} \cdot R_H$$

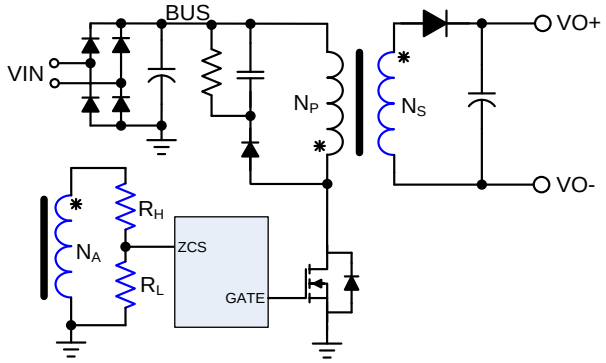



## Programmable Output OVP

The SY5040 will sense output voltage by ZCS pin and programmable output OVP can be achieved. When the primary power MOS is turned off, the voltage on auxiliary winding will be proportional to output voltage. The ZCS pin will sense the output voltage by a resistor divider connected between auxiliary winding. When the ZCS pin voltage rises above OVP threshold $V_{ZCS\_OVP}$, the IC will stop switching and enter auto-recovery mode. The output OVP threshold is calculated as below:

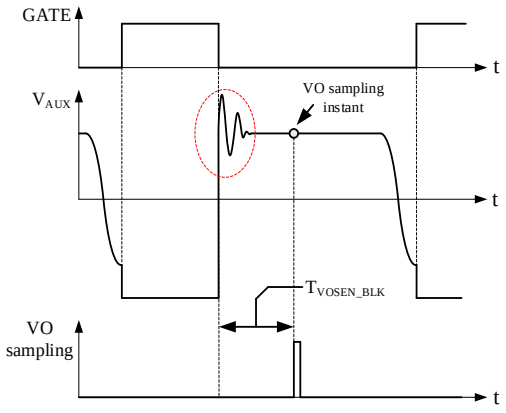
$$V_{O\_OVP} = V_{ZCS\_OVP} \cdot \frac{N_S}{N_A} \cdot \frac{R_H + R_L}{R_L}$$

Note: The upper resistor $R_H$ should be determined firstly according to input brown out level set point, and then the lower resistor $R_L$ of ZCS pin resistor divider is calculated according to above equation.




When the primary power MOS is turned off, there will be a parasitic resonance on auxiliary winding voltage as shown in below figure. To avoid the false trigger of output OVP by the parasitic resonance, a blanking time ($T_{VOSEN\_BLK}$) is adopted after primary power MOS is turned off. The SY5040 only samples

the auxiliary winding voltage after the blanking time elapse, so reliable output OVP can be achieved. It is recommended that the parasitic resonant time should be decayed to very small level within 1.5us after primary power MOS is turned off.



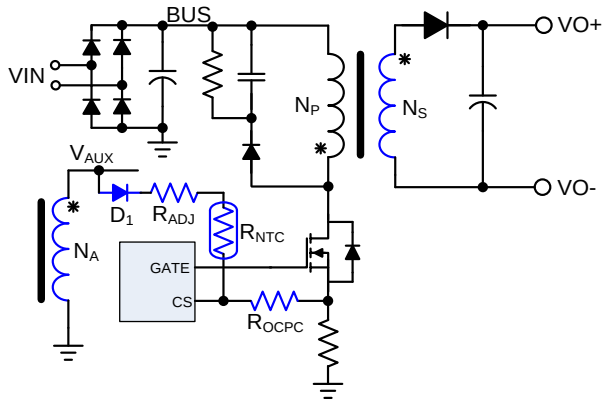

## Programmable External OTP

The SY5040 can achieve programmable external OTP through the CS pin. When the primary MOS is turned off, the voltage on auxiliary winding will be proportional to output voltage. Since the output voltage is a constant value under steady state, the voltage on auxiliary winding is also a nearly constant value. It will be used as a reference voltage. A NTC resistor and the OCP compensation resistor $R_{OCPC}$ will form a voltage divider (peak current sense resistor is very small and is neglected). Under the normal temperature, the NTC resistor is very large, and the CS pin voltage will be low level. When NTC's temperature rises, the NTC resistor becomes smaller and smaller, the CS pin voltage will become higher and higher. If the CS pin voltage is higher than OTP threshold $V_{CS\_OTP}$, and last for 4 consecutive switching cycles, the external OTP will be triggered. The IC will stop switching and enter auto-recovery mode. Resistance of NTC resistor at external OTP set point is calculated as below equation:

$$R_{NTC(OTP)} = R_{OCPC} \cdot \left(\frac{\frac{N_A}{N_S} \cdot V_O - V_{D1}}{V_{CS\_OTP}} - 1\right) - R_{ADJ}$$

Where $V_{CS\_OTP}$ is CS pin OTP threshold (typical=1.0V), $R_{ADJ}$ is used to fine tune external OTP threshold.

Note: OCP compensation resistor $R_{OCPC}$ should be firstly determined according to OCP level over 90V~264V input range. Then the external OTP parameter is calculated according to above equation. It is recommended that diode D1 should be a small signal switching diode such as 1N4148, BAV21, etc




## Secondary Diode Short Circuit Protection

Under the secondary diode short circuit condition, when the primary power MOS is turned on, the primary current will increase with very high di/dt rate. After CS pin leading edge blanking time elapse, primary peak current signal $V_{CS}$ will rise above 0.97V (maximum peak current limit level under normal condition). The SY5040 defines an OCP threshold $V_{CS\_OCP}$, when $V_{CS}$ rises above $V_{CS\_OCP}$ after leading edge blanking time elapse, and last for 4 consecutive switching cycles, secondary diode short circuit protection will be triggered, IC will stop switching and enter auto-recovery mode.

## OLP

When the over load condition happens, COMP pin voltage will be pulled up to high level, and the primary peak current will reach the maximum value. The SY5040 will compare COMP pin voltage with an OLP threshold, when $V_{COMP}$ is higher than the OLP threshold, a timer will begin to count, and if $V_{COMP}$ is continuously higher than OLP threshold which result in OLP timer elapse, the SY5040 will stop switching and enter auto-recovery mode.

## VCC OVP

Under abnormal conditions, such as opto-coupler open circuit, VCC pin voltage may rise to a very high level. To avoid IC damage caused by VCC pin over voltage condition, the SY5040 adopts an internal OVP threshold $V_{VCC\_OVP}$, when $V_{VCC}$ exceeds $V_{VCC\_OVP}$ threshold, the SY5040 will stop switching and enter auto-recovery mode.

## Internal OTP

The SY5040 monitors die temperature in normal operating mode. Once die temperature rises above internal OTP threshold, IC will stop switching and enter auto-recovery mode.

# Power Supply Design Guide

## BUS Capacitor Calculation

Generally, the bulk capacitor $C_{BUS}$ is selected according to below rules:

1~2uF per watt (input power)

$$C_{BUS\_MIN} = (1.0 \cdot P_{IN})\,uF$$

$$C_{BUS\_MAX} = (2.0 \cdot P_{IN})\,uF$$

## Minimum BUS Voltage Calculation

The minimum BUS voltage appears when the input voltage $V_{IN}$ is the lowest and the output current reaches the rated value.

Minimum BUS voltage at rated output power is calculated as:

$$V_{BUS\_MIN} = \sqrt{2 \cdot V_{IN\_MIN}^{\ 2} - \frac{P_O \cdot (1 - K_{CH})}{\eta \cdot C_{BUS} \cdot f_0}}$$

Where $K_{CH}$ is BUS capacitor charge coefficient (generally $K_{CH}$ is set to 0.2~0.3), is converter efficiency, and $f_0$ is frequency of AC input.

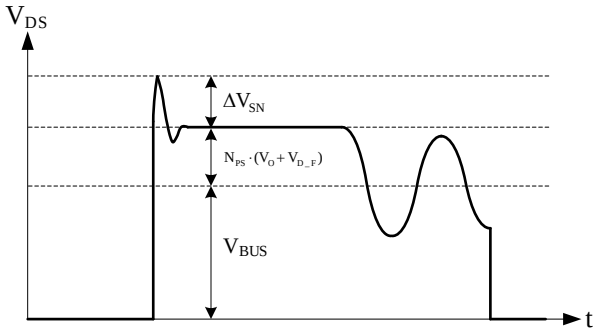
### Transformer Parameter Calculation

**1) Primary/Secondary Turns Ratio: $N_{PS}$**

$N_{PS}$ is limited by the voltage stress of primary power MOSFET:

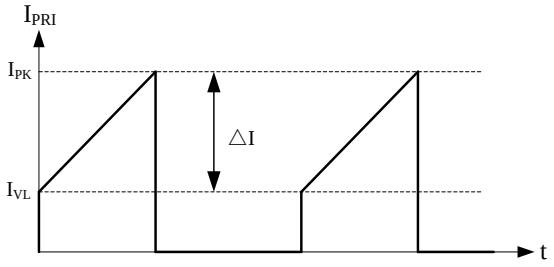
$$N_{PS} \le \frac{V_{MOS\_BR} \cdot K_{DR} - \sqrt{2} \cdot V_{IN\_MAX} - \Delta V_{SN}}{V_O + V_{D\_F}}$$

Where $V_{MOS\_BR}$ is the breakdown voltage of primary MOSFET; $K_{DR}$ is $V_{DS}$ de-rating factor of power MOS; $V_{D\_F}$ is forward voltage drop of secondary rectification diode; $\Delta V_{SN}$ is voltage spike during primary MOS turn off instant.




**2) Primary Inductance: $L_M$**

Transformer primary inductance is related with primary current ripple. Generally, primary side current ripple is defined as shown in below figure. And current ripple factor is defined as below equation:




$$K_{RP} = \frac{0.5 \cdot \Delta I}{I_{PK} - 0.5 \cdot \Delta I}$$

$K_{RP}$<1: CCM

$K_{RP}$=1: DCM (QR mode)

Generally, to get the optimized transformer size and efficiency for universal input application, under low input and full load condition, CCM operating is selected, while under high input and full load condition, QR mode is selected.

Based on design experience, under the lowest input and full load condition, it is recommended to choose $K_{RP}$ between 0.3~0.5 for optimized performance. And for an initial start, $K_{RP}$=0.4 is selected. Once $K_{RP}$ is selected, primary inductance of transformer is calculated as equation below:

$$L_M = \frac{V_{BUS\_MIN}^{\ 2} \cdot D_{MAX}^{\ 2} \cdot \eta}{2 \cdot P_O \cdot f_{SW} \cdot K_{RP}}$$

Where $f_{SW}$ is rated switching frequency (65kHz), $I_O$ is rated output current, is converter efficiency. $D_{MAX}$ is maximum duty cycle at $V_{BUS\_MIN}$ and rated output power, and $D_{MAX}$ is calculated as below equation:

$$D_{MAX} = \frac{N_{PS} \cdot (V_O + V_{D\_F})}{V_{BUS\_MIN} + N_{PS} \cdot (V_O + V_{D\_F})}$$

**3) Turns of Primary Winding: $N_P$**

**(a)** Select the magnetic core type, identify the effective cross-sectional area $A_E$

**(b)** Preset the maximum magnetic flux density $B_{MAX}$ at rated output power

$$B_{MAX} = 0.22T \sim 0.28T$$

**(c)** Calculate maximum primary peak current $I_{PK}$ at rated output power:

$$I_{PK} = \frac{V_O \cdot I_O \cdot (1 + K_{RP})}{V_{BUS\_MIN} \cdot D_{MAX} \cdot \eta}$$

**(d)** Calculate primary turns: $N_P$

$$N_P = \frac{L_M \cdot I_{PK}}{B_{MAX} \cdot A_E}$$

Where $A_E$ is effective cross-sectional area of core

**4) Turns of Secondary Winding: $N_S$**

$$N_S = \frac{N_P}{N_{PS}}$$

**5) Turns of Auxiliary Winding: $N_A$**

Before the calculate auxiliary turns, VCC supply voltage $V_{CC(AUX)}$ by auxiliary winding should be predefined first. Generally, $V_{CC(AUX)}$ is set to 14V~18V, then auxiliary turns is calculated as:

$$N_A = \frac{V_{CC(AUX)} \cdot N_S}{V_O}$$

**Peak Current Sense Resistor Calculation**

Maximum peak current appears under minimum BUS voltage and maximum load condition (OCP point); maximum peak current is calculated as:

$$I_{PK\_MAX} = \frac{V_O \cdot I_O \cdot K_{OCP} \cdot (1+K_{RP})}{V_{BUS\_MIN} \cdot D_{MAX} \cdot \eta}$$

Where $K_{OCP}$ is OCP proportion, $K_{OCP}$ is generally set to 120%~130%.

After the maximum primary peak current has been calculated, the peak current sense resistor $R_{CS}$ can be easily derived by equation below:

$$R_{CS} = \frac{V_{CS\_MAX}}{I_{PK\_MAX}}$$

Where $V_{CS\_MAX}$ is the maximum allowed peak current sense voltage (typical=0.97V).

Note: Customer may need to fine tune current sense resistor according to the converter OCP point. If OCP point is larger than target level, $R_{CS}$ should be tuned a little larger; If OCP point is smaller than target level, $R_{CS}$ should be tuned a little smaller.

**Secondary Diode Selection**

Under the conditions of the maximum BUS voltage and maximum output voltage, the reverse voltage of secondary rectification diode will reach the maximum level. The maximum value of diode reverse voltage (ignore voltage spike when primary MOS is turned on) is calculated as equation below:

$$V_{D\_R\_MAX} = \frac{\sqrt{2} \cdot V_{IN\_MAX}}{N_{PS}} + V_{O\_OVP}$$

Where $V_{IN\_MAX}$ is maximum AC input voltage (RMS), $N_{PS}$ is the primary/secondary turns ratio of the transformer and $V_{O\_OVP}$ is output OVP threshold, which is predefined by customer.

Maximum instantaneous forward current is calculated as equation below:

$$I_{D\_PK\_MAX} = I_{PK\_MAX} \cdot N_{PS}$$

Where $I_{PK\_MAX}$ is the maximum primary peak current at $V_{BUS\_MIN}$ and OCP point.

Average forward current of diode is

$$I_{D\_AVG\_MAX} = I_O \cdot K_{OCP}$$

Where $I_O$ is rated output current, and $K_{OCP}$ is OCP proportion to rated output current.

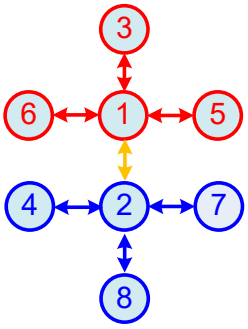
# Layout Considerations

A proper PCB design must follow the below guidelines:

(a) To achieve a good EMI performance and to reduce the line frequency voltage ripples, the output of the bridge rectifier should be connected to the BUS line capacitor first, then to the switching circuit.

(b) The circuit loop of all switching circuit should be kept as small as possible: primary power loop, secondary power loop and auxiliary power loop.

(c) The connection of primary ground is recommended as:




Ground ①: Ground of BUS capacitor

Ground ②: Ground of bias supply capacitor

Ground ③: Ground of auxiliary winding

Ground ④: Ground of ZCS pin divider resistor

Ground ⑤: Ground of primary side Y capacitor

Ground ⑥: Ground of current sense resistor.

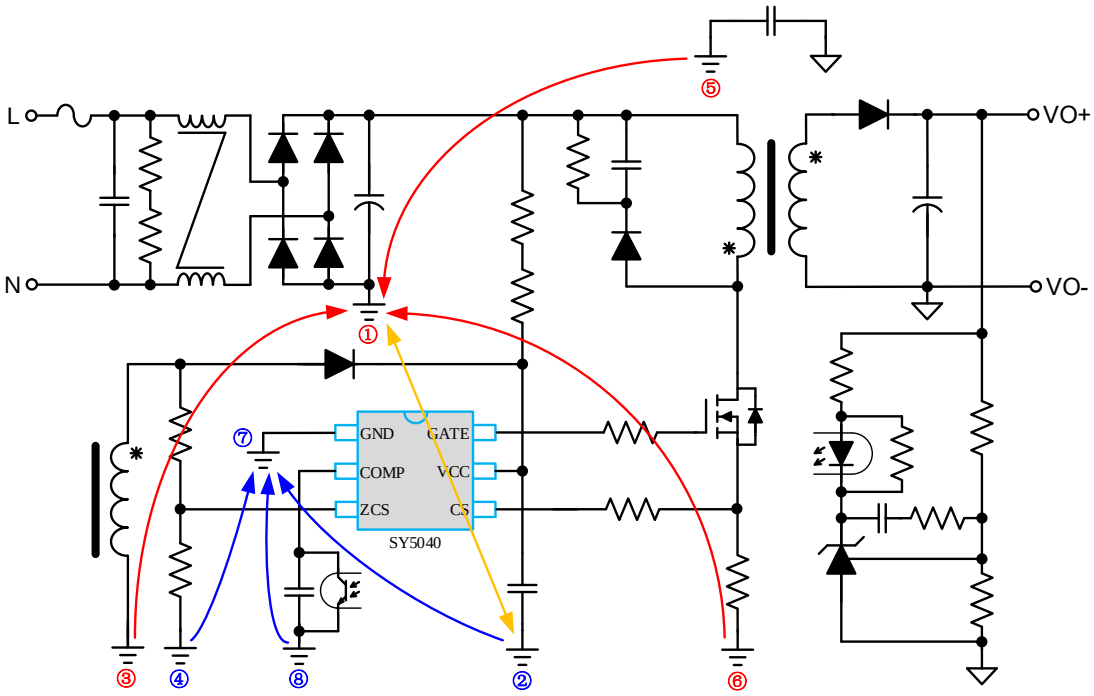
Ground ⑦: Ground of controller IC.

Ground ⑧: Ground of receiver of opto-coupler.

(d) Bias supply trace should be connected to the bias supply capacitor first and then to the GND pin. The bias supply capacitor should be put right beside the IC.

(e) The switching loop formed by 'Source pin – current sense resistor – GND pin' should be kept as small as possible.

(f) The resistor divider connected to ZCS pin is recommended to be put close to the IC.



# Design Example

A design example of typical application is shown below step by step.

**Input/Output specification**

| Parameter | Symbol | Value |
|---|---|---|
| Input voltage range | $V_{IN}$ | 90V~264V |
| Rated output power | $P_O$ | 45W |
| Rated output voltage | $V_O$ | 20V |
| Output OVP level | $V_{O\_OVP}$ | 24V |
| Rated output current | $I_O$ | 2.25A |
| OCP proportion | $K_{OCP}$ | 120% |

**Preset Parameter**

| Parameter | Symbol | Value |
|---|---|---|
| Break down voltage of power MOS | $V_{MOS\_BR}$ | 650V |
| $V_{DS}$ de-rating factor of power MOS | $K_{DR}$ | 90% |
| Spike on $V_{DS}$ during power MOS turn off | $\Delta V_{SN}$ | 100V |
| Converter efficiency | | 88% |
| Primary current ripple factor at $V_{BUS\_MIN}$ & rated output power | $K_{RP}$ | 0.4 |
| BUS capacitor charge coefficient | $K_{CH}$ | 0.2 |
| Secondary diode forward voltage drop | $V_{D\_F}$ | 0.5V |
| Input brown out protection level (RMS) | $V_{IN\_BO}$ | 70V |
| Transformer effective cross-sectional area (RM10) | $A_E$ | 98 $mm^2$ |

## 1) BUS Capacitor Selection

Calculate input power at rated output power

$$P_{IN}=\frac{P_O}{\eta}=\frac{45}{88\%}=51.14W$$

Minimum BUS capacitor: $C_{BUS\_MIN}=1.0\times 51.14=51.14uF$

Maximum BUS capacitor: $C_{BUS\_MAX}=2.0\times 51.14=102.28uF$

Select BUS capacitor: $C_{BUS}=82uF$

## 2) Minimum BUS Voltage Calculation

BUS capacitor charge coefficient: $K_{CH}$=0.2

$$V_{BUS\_MIN}=\sqrt{2\cdot V_{IN\_MIN}^{\ 2}-\frac{P_O\cdot(1-K_{CH})}{\eta\cdot C_{BUS}\cdot f_0}}=\sqrt{2\cdot 90^2-\frac{45\cdot(1-0.2)}{88\%\cdot 82u\cdot 50}}=79V$$

## 3) Transformer Design

(a)Calculate primary/secondary turns ratio: $N_{PS}$

$$N_{PS}\le\frac{V_{MOS\_BR}\cdot K_{DR}-\sqrt{2}V_{IN\_MAX}-\Delta V_{SN}}{V_O+V_{D\_F}}=\frac{650\cdot 0.9-\sqrt{2}\cdot 264-100}{20+0.5}=5.5$$

$N_{PS}$ is selected to: $N_{PS} = 5$

(b) Calculate maximum duty cycle: $D_{MAX}$

$$D_{MAX} = \frac{N_{PS} \cdot (V_O + V_{D\_F})}{V_{BUS\_MIN} + N_{PS} \cdot (V_O + V_{D\_F})} = \frac{5 \cdot (20 + 0.5)}{79 + 5 \cdot (20 + 0.5)} = 56.5\%$$

(c) Calculate primary inductance: $L_M$

$$L_M = \frac{V_{BUS\_MIN}^{\ 2} \cdot D_{MAX}^{\ 2} \cdot \eta}{2 \cdot V_O \cdot I_O \cdot f_{SW} \cdot K_{RP}} = \frac{79^2 \cdot 56.5\%^2 \cdot 88\%}{2 \cdot 20 \cdot 2.25 \cdot 65 \cdot 1000 \cdot 0.4} = 749.2uH$$

Select $L_M = 750uH$

(d)Calculate primary peak current at rated output power:

$$I_{PK} = \frac{V_O \cdot I_O \cdot (1 + K_{RP})}{V_{BUS\_MIN} \cdot D_{MAX} \cdot \eta} = \frac{20 \cdot 2.25 \cdot (1 + 0.4)}{79 \cdot 56.5\% \cdot 88\%} = 1.60A$$

(e)Calculate primary winding turns: $N_P$

Transformer core effective cross-sectional area: $A_E = 98 \cdot 10^{-6} m^2$

Maximum allowed flux density: $B_{MAX} = 0.27T$

$$N_P = \frac{L_M \cdot I_{PK}}{B_{MAX} \cdot A_E} = \frac{750u \cdot 1.6}{0.27 \cdot 98 \cdot 10^{-6}} = 45.35$$

Select primary winding turns: $N_P$=45

(f) Calculate secondary winding turns: $N_S$

$$N_S = \frac{N_P}{N_{PS}} = \frac{45}{5} = 9$$

Select secondary winding turns: $N_S$=9

(g) Calculate auxiliary winding turns: $N_A$

VCC supply voltage from auxiliary winding is set to: $V_{CC(AUX)}$=16V

$$N_A = \frac{V_{CC(AUX)} \cdot N_S}{V_O} = \frac{16 \cdot 9}{20} = 7.2$$

Select auxiliary winding turns: $N_A$=7

(h) If other transformer core type is selected, then recalculate (e)~(g).

**4) Current Sense Resistor Calculation:**

$$I_{PK\_MAX} = \frac{V_O \cdot I_O \cdot K_{OCP} \cdot (1 + K_{RP})}{V_{BUS\_MIN} \cdot D_{MAX} \cdot \eta} = \frac{20 \cdot 2.25 \cdot 120\% \cdot (1 + 0.4)}{79 \cdot 56.5\% \cdot 88\%} = 1.92A$$

$$R_{CS} = \frac{V_{CS\_MAX}}{I_{PK\_MAX}} = \frac{0.97}{1.92} = 0.505\Omega$$

**5) Secondary Diode Selection**

(a)Maximum reverse voltage calculation:

$$V_{D\_R\_MAX} = \frac{\sqrt{2} \cdot V_{IN\_MAX}}{N_{PS}} + V_{O,OVP} = \frac{\sqrt{2} \cdot 264}{5} + 24 = 98.7V$$

Considering the voltage spike, reverse voltage rating of the diode is recommended to be 120V~150V.

(b)Maximum instantaneous forward current:

$$I_{D\_PK\_MAX} = N_{PS} \cdot I_{PK\_MAX} = 5 \cdot 1.92 = 9.6A$$

(c)Maximum average forward current:

$$I_{D\_AVG\_MAX} = I_O \cdot K_{OCP} = 2.25 \cdot 120\% = 2.7A$$

**6) Calculate ZCS Pin Resistor Divider**

(a)Firstly, calculate upper resistor: $R_H$

Predefined input voltage browns out protection level: $V_{IN\_BO}$=70V

$$R_H = \frac{\sqrt{2} \cdot V_{IN\_BO}}{I_{BO}} \cdot \frac{N_A}{N_P} = \frac{\sqrt{2} \cdot 70}{100u} \cdot \frac{7}{45} = 154k\Omega$$

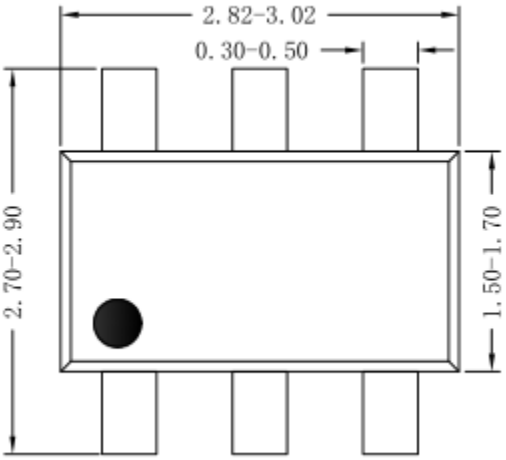
Select $R_H$=150k

(b) After $R_H$ is determined, then calculate lower resistor: $R_L$

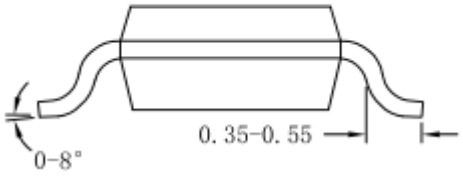
$$R_L = \frac{1}{\frac{V_{O\_OVP}}{V_{ZCS\_OVP}} \cdot \frac{N_A}{N_S} - 1} \cdot R_H = \frac{1}{\frac{24}{2} \cdot \frac{7}{9} - 1} \cdot 150k = 18k\Omega$$

Select $R_L$=18 k

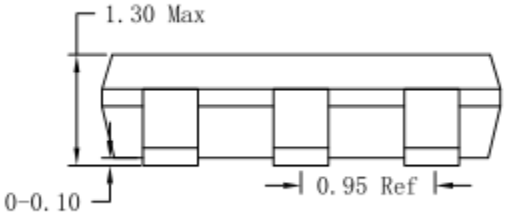
# SOT23-6 Package Outline & PCB Layout Design



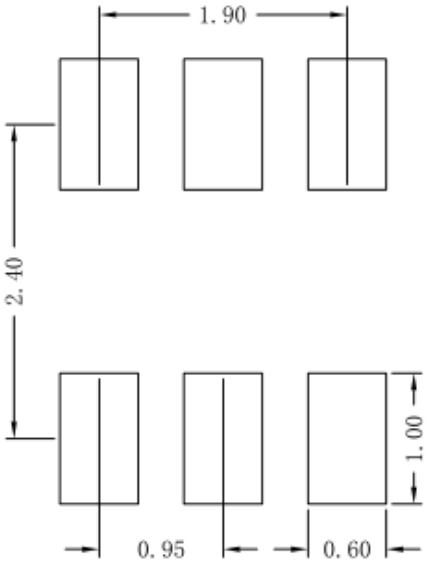

Top View




Side View




Side View

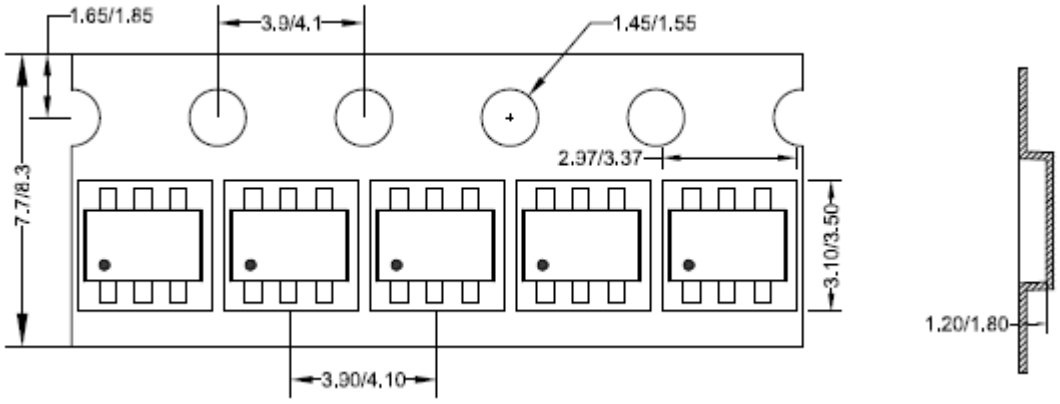



Recommended Pad Layout

**Notes:** **All dimension in millimeter and exclude mold flash & metal burr.**

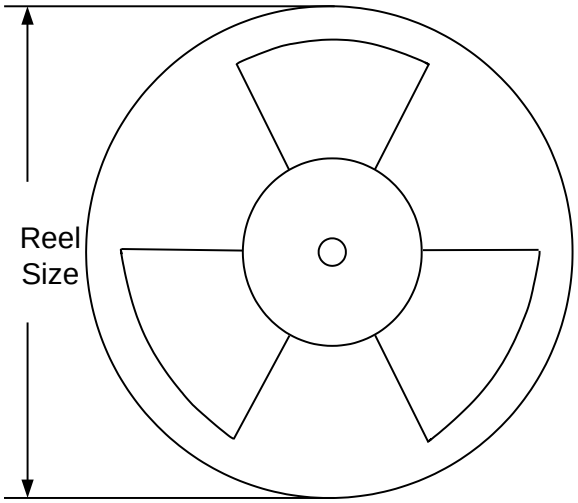
# Taping & Reel Specification

## 1. Taping orientation for packages（SOT23-6）




**Feeding direction** ⟶

## 2. Carrier Tape & Reel specification for packages




| Package type | Tape width (mm) | Pocket pitch(mm) | Reel size (Inch) | Trailer length(mm) | Leader length (mm) | Qty per reel |
|---|---|---|---|---|---|---|
| SOT23-6 | 8 | 4 | 7" | 280 | 160 | 3000 |

# Revision History

The revision history provided is for informational purpose only and is believed to be accurate, however, not warranted. Please make sure that you have the latest revision.

| Date | Revision | Change |
|---|---|---|
| June 21, 2024 | Revision 1.0A | 1, Add dynamic ZCS/CS pin negative voltage/current capability;<br>2, Add the specification for ISEN pin short circuit protection(VCS_SCP, TCS_SCP_BLK) in EC table |
| August 7, 2019 | Revision 0.9 | Initial Release |

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