SY50433B

Flyback Regulator
With Primary Side CV/CC Control
for High Input Voltage Application

General Description

SY50433B is a single stage Flyback regulator targeting at high input voltage applications. It integrates 900V MOSFET to decrease physical volume. Both the output current and voltage are sensed by primary side signal process. SY50433B operates in quasi-resonant mode and adaptive PWM/PFM control for highest average efficiency. In addition, SY50433B integrates fast internal HV start up circuit to minimize no-load loss and external components. A special OVP function of VREG pin has been integrated in SY50433B to prevent the output voltage from raising too high with light load during strong magnetic field test.

Features

- Integrated 900V MOSFET
- Very Tight Primary Side CV/CC Regulation
- Quasi-resonant Mode and PWM/PFM Control for Higher Average Efficiency
- Internal CC/CV Loop Compensation
- Low Start Up Current: 5μA Max
- HV Start Up Circuit to Reduce No-load Loss
- Maximum Switching Frequency Limitation 125kHz
- VREG OVP Function for Strong Magnetic Field Test
- Reliable Protections for OCP,SCP,VCCOVP,VSEN SCP, OTP
- Compact Package: SSOP10

Ordering Information

SY50433□(□□)□
- Temperature Code
- Package Code
- Optional Spec Code

Ordering Number	Package type	Note
SY50433BFHC	SSOP10	----

Applications

- Power Supply for STB Home Appliances, Smart Power Meter and Other Appliances with High AC Input Voltage

Recommended operating output power	
Products	85~450Vac
SY50433B	7W

Typical Applications

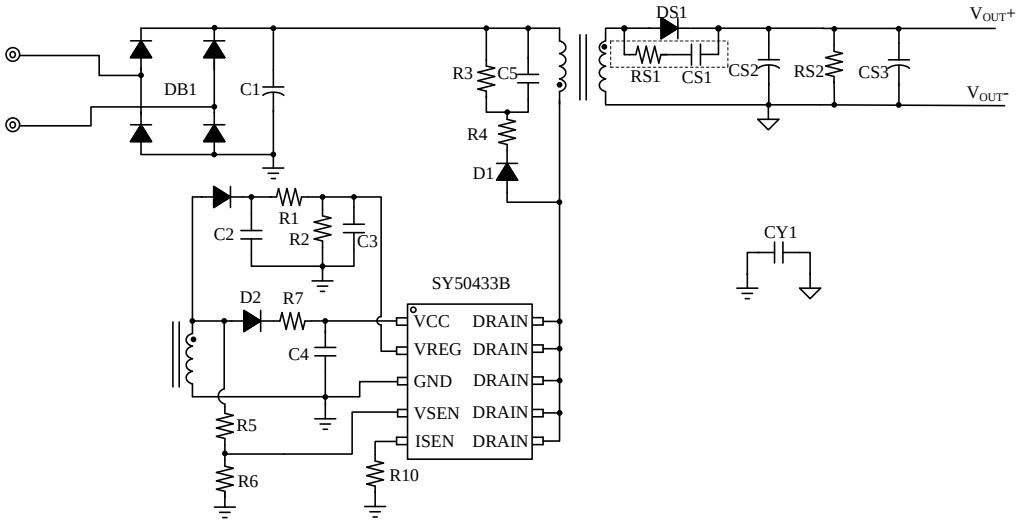
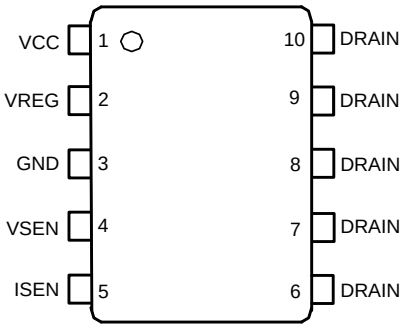


Fig.1 Schematic Diagram

Pinout (top view)



(SSOP10)

Top Mark: CLL*xyz* (device code: CLL, ***x=year code, y=week code, z= lot number code*****)**

Pin	Name	Description
1	VCC	Power supply pin.
2	VREG	Aux-winding voltage detection pin. Connect this pin to a voltage sensing circuit (shown in fig.1) to prevent the output voltage from raising too high with light load during strong magnetic field test.
3	GND	Ground pin.
4	VSEN	Inductor current zero-crossing detection pin. This pin receives the auxiliary winding voltage by a resistor divider and detects the inductor current zero crossing point.
5	ISEN	Current sense pin. Connect this pin to the source of the primary switch.
6~10	DRAIN	Drain of the internal power MOSFET.

Absolute Maximum Ratings (Note 1)

VCC---------- -0.3V~25V
VREG---------- -0.3V~3.3V
ISEN----- ---------- -0.3V~3.6V
VSEN---------- -0.3V~V_{VCC}+0.3V
DRAIN---------- 900V
Power Dissipation, @ TA = 25°C SSOP10 ---------- 1.1W
Package Thermal Resistance (Note 2)
SSOP10, θ_{JA} ---------- 125°C/W
SSOP10, θ_{JA} ---------- 60°C/W
Junction Temperature Range ---------- -45°C to 150°C
Lead Temperature (Soldering, 10 sec.) ---------- 260°C
Storage Temperature Range ---------- -65°C to 150°C

Recommended Operating Conditions (Note 3)

VCC---------- 10V~17V
ISEN---------- 0V~1V
Junction Temperature Range ---------- -40°C to 125°C
Ambient Temperature Range ---------- -40°C to 105°C

Block Diagram

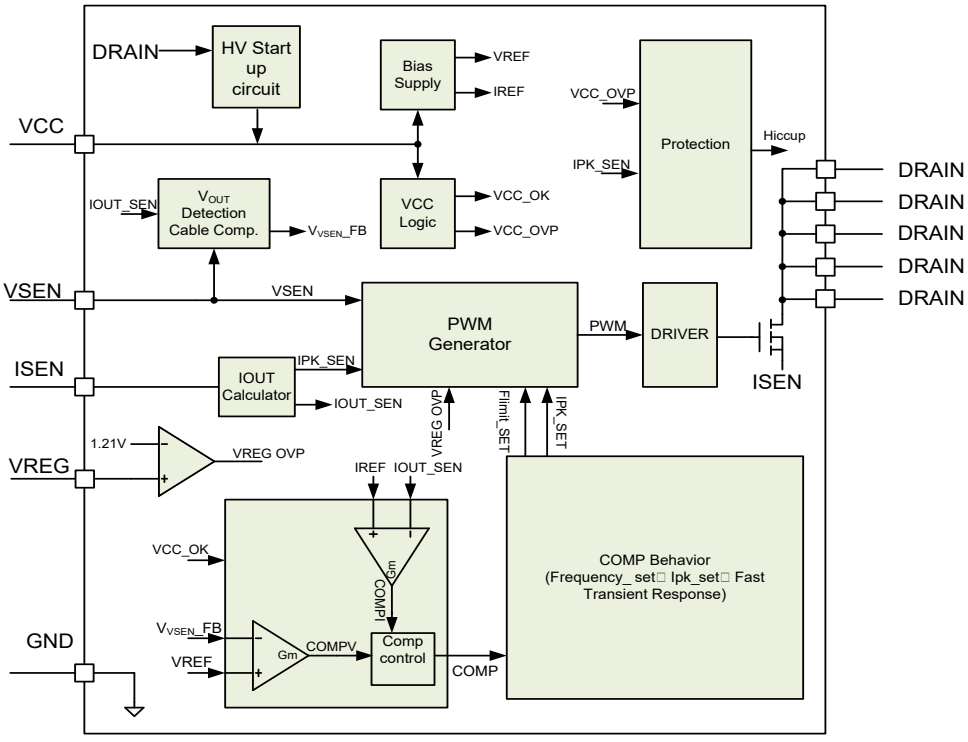


Fig.2 Block Diagram

Electrical Characteristics

(V_{CC} = 12V (Note 3), T_A = 25°C unless otherwise specified)

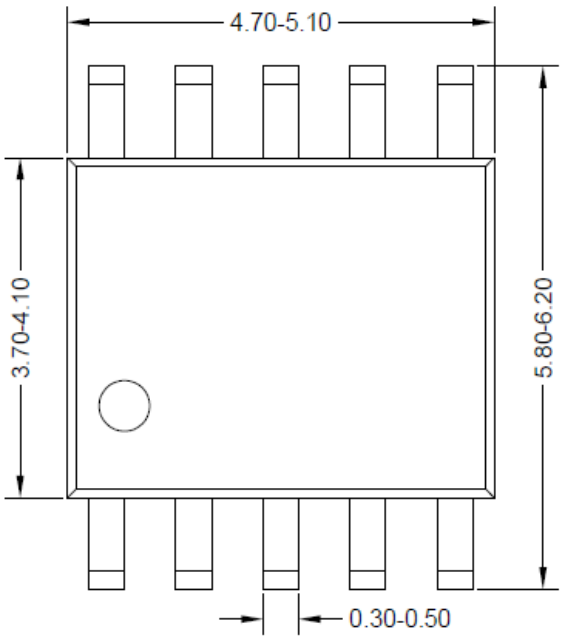
Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Power Supply Section						
VCC Operating Range	V_{VCC_RANGE}		8.5		21	V
VCC Turn-on Threshold	V_{VCC_ON}		19.4	21	22.6	V
VCC Turn-off Threshold	V_{VCC_OFF}		6.6	7.6	8.6	V
VCC OVP Voltage	V_{VCC_OVP}			24		V
Start Up Current	I_{ST}	$V_{VCC}<V_{VCC\_OFF}$		2.3	5	μA
Operating Current	I_{VCC}	f=100kHz		1.5		mA
Quiescent Current	I_Q	f=2kHz	200	350	500	μA
Discharge Current in OVP Mode	I_{VCC_OVP}	V_{VCC}=12V		5		mA
Internal HV Start Up VCC Charge Current	$I_{HV\_STARTUP}$			0.35		mA
Current Feedback Modulator Section						
Internal Reference Voltage for Output Current	V_{REF}		0.411	0.42	0.429	V
VREG Pin Section						
VREG Pin OVP Voltage Threshold	V_{VREG_OVP}		1.1	1.21	1.3	V
ISEN Pin Section						
Current Limit Voltage	V_{ISEN_LIM}		0.9	1	1.1	V
VSEN Pin Section						
Internal Reference Voltage	V_{REFV}		1.238	1.25	1.262	V
Integrated MOSFET Section						
Breakdown Voltage	V_{BV}	V_{GS}=0V,I_{DS}=250μA	900			V
Static Drain-Source On-Resistance	R_{DSON}	V_{GS}=12V, I_{DS}=0.1A T_A=25°C		13.4		Ω
Drain Current Continuous	I_{DS}	T_A=25°C			0.35	A
Switching Section						
Max ON Time	T_{ON_MAX}			18		μs
Min ON Time	T_{ON_MIN}			350		ns
Max OFF Time	T_{OFF_MAX}		450	550	700	μs
Min OFF Time	T_{OFF_MIN}		1.2	1.7	2.2	μs
Maximum Switching Frequency	F_{MAX}		95	120	145	kHz
Thermal Section						
Thermal Shutdown Temperature	T_{SD}			150		°C
Thermal Shutdown Recovery Hysteresis				30		°C

Note 1: Stresses beyond the "Absolute Maximum Ratings" may cause perm anent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

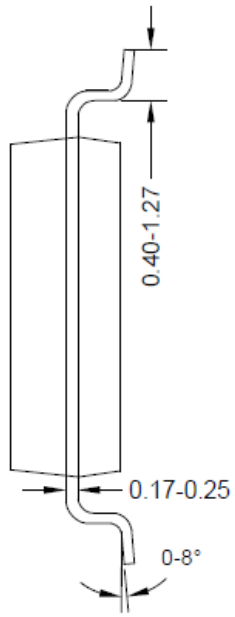
Note 2: θ_{JA} is measured in the natural convection at T_A = 25°C on a low effective single layer thermal conductivity test board of JEDEC 51-3 thermal measurement standard. Test condition: Device mounted on "2 x 2" FR-4 substrate PCB, 2oz copper, with minimum recommended pad on top layer and thermal vias to bottom layer ground plane.

Note 3: Increase VCC pin voltage gradually higher than V_{VCC_ON} voltage then regulated to 12V.

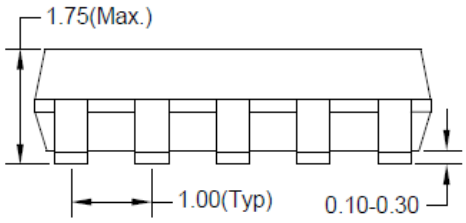
SSOP10 Package Outline Drawing



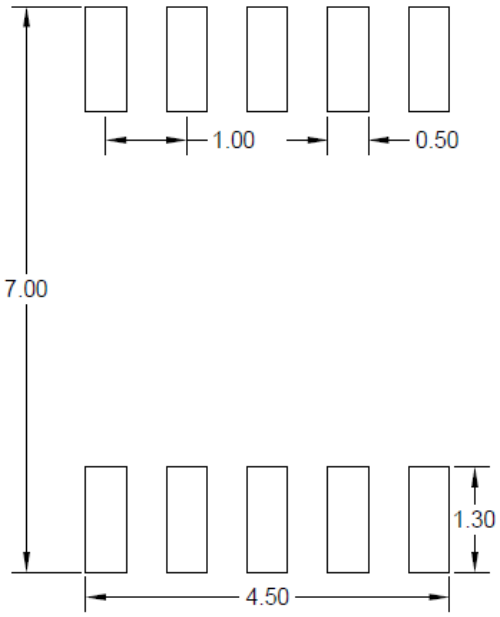
Top view



Side view



Front view



Recommended PCB layout

(Reference only)

Notes: **All dimension in millimeter and exclude mold flash & metal burr.**