SA52106

Six Half-Bridge Driver with SPI control

General Description

The SA52106 is a six half-bridge motor driver solution for automotive, industrial and other mechatronic applications. All the functions can be programmed through a serial data interface.

The SA52106 provides internal shutdown functions with a fault output (SO pin) for over current protection, open load detection, short circuit protection, under voltage lockout, over voltage lockout and thermal shutdown. A low-power sleep mode is also provided. The device is packaged in QFN5*5-24 with exposed pad.

Ordering Information

SA52106 □(□□)□

- Temperature Code
- Package Code
- Optional Spec Code

Ordering Number	Package type	Note
SA52106VAA	QFN5x5-24	

Features

- Six Half-Bridge Drivers
- 0.55A Output Current per Channel
- Low Power Mode
- Compatible with 5V/3.3V System
- Serial Data Interface, up to 5MHz
- Fault Reporting
- PWM Capable Outputs for Frequency 80Hz, 100Hz and 200Hz with 8-bit Duty Cycle Resolution
- Internal over Current Protection, Short Circuit Protection, Open Load Detection, under Voltage Lockout, over Voltage Lockout and Thermal Shutdown
- AEC-Q100 Qualified
- QFN5×5-24 Package

Applications

- Automotive
- Industrial
- HVAC
- DC brush motor

Typical Application

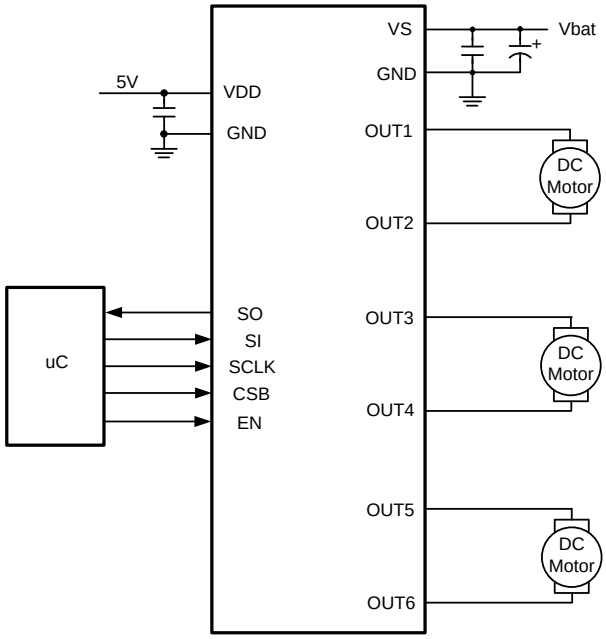
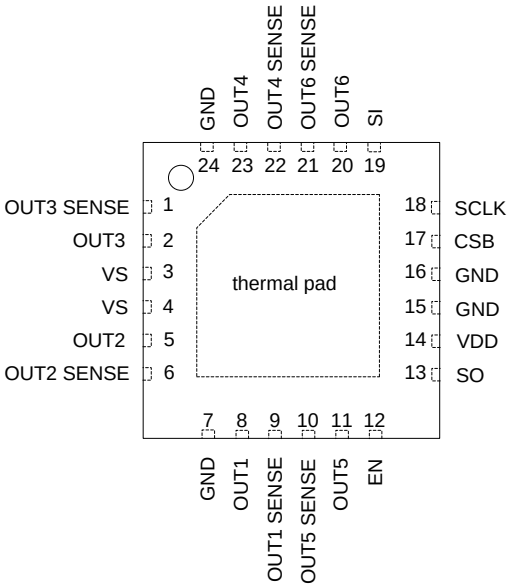


Figure1. Typical Application Circuit

Pin out (Top View)



(QFN5×5-24)

Top Mark: EAY*xyz* (device code: **EAY**, ***x=year code, y=week code, z= lot number code)***

Pin Description

Name	Number	Description
OUT3 SENSE	1	Only for testability in final test. It is recommended to connect to the pin OUT3
OUT3	2	Half-bridge Output 3.
VS	3,4	Power supply for internal high side output drivers.
OUT2	5	Half-bridge Output 2.
OUT2 SENSE	6	Only for testability in final test. It is recommend to connect to the pin OUT2
OUT1	8	Half-bridge Output 1.
OUT1 SENSE	9	Only for testability in final test It is recommended to connect to the pin OUT1
OUT5 SENSE	10	Only for testability in final test It is recommended to connect to the pin OUT5
OUT5	11	Half-bridge Output 5.
EN	12	Enable. Logic high enables the IC. Internal pull down.
SO	13	Serial data output. 16 bit serial communications output.
VDD	14	Power supply for internal logic.
GND	7,15,16,24	Ground. Internal connection to lead frame.
CSB	17	Chip select Bar. Active low serial port operation.
SCLK	18	Serial Clock. Clock input for use with SPI communication.
SI	19	Serial input. 16 bit serial communications input.
OUT6	20	Half-bridge Output 6.
OUT6 SENSE	21	Only for testability in final test It is recommended to connect to the pin OUT6
OUT4 SENSE	22	Only for testability in final test It is recommended to connect to the pin OUT4
OUT4	23	Half-bridge Output 4.

Block Diagram

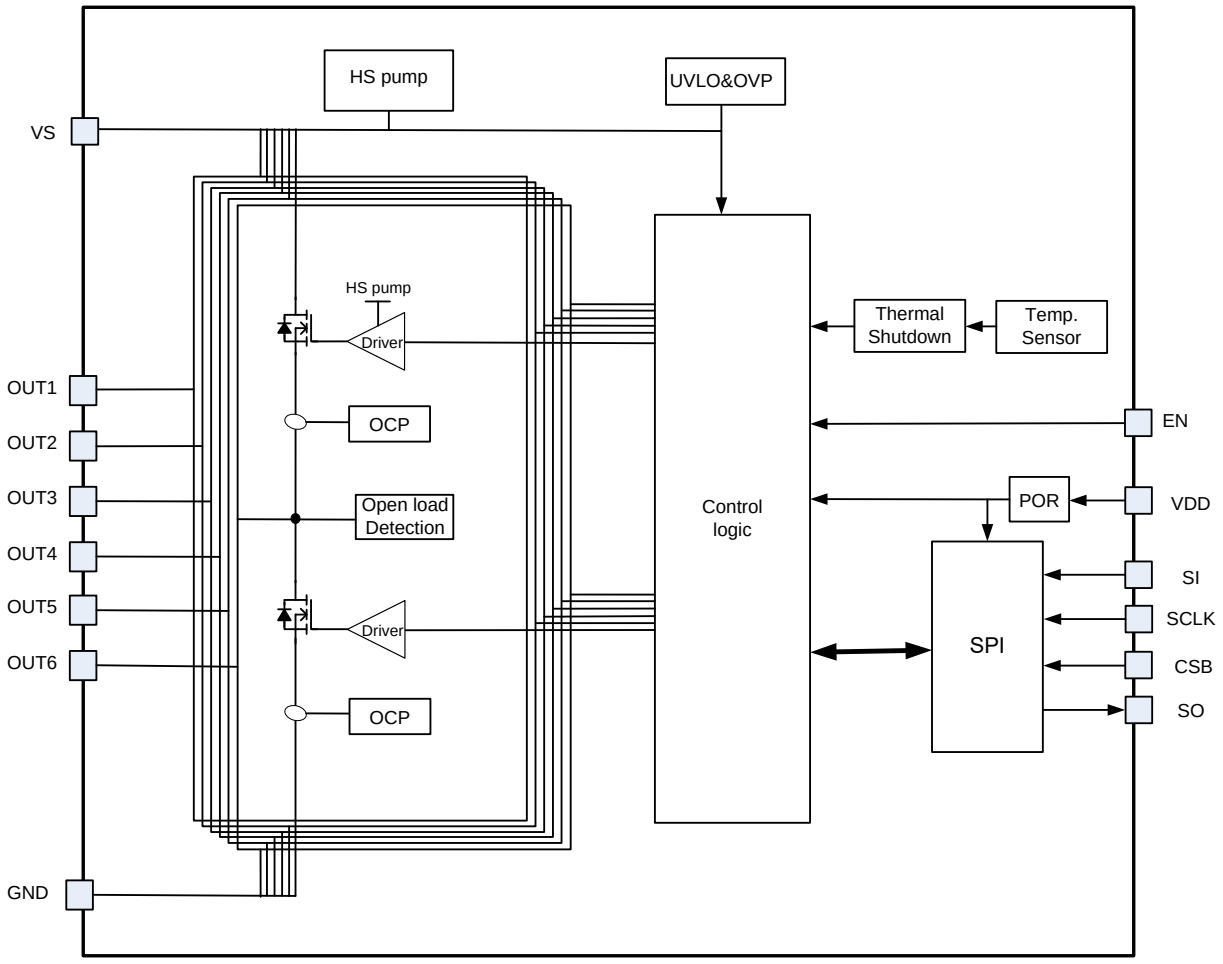


Figure3. SA52106 Block Diagram

Absolute Maximum Ratings (Note 1)

VS (DC) ---------- -0.3V to 40V
OUTx(DC)---------- -0.3V to 40V
Digital pin (SI, SCLK, CSB, SO, EN) ---------- -0.3V to 7V
VDD---------- -0.3V to 7V
Junction Temperature (T_J) ---------- -40°C to +150°C
Storage Temperature ---------- -55°C to +150°C
QFN5x5-24 Package Thermal Resistance (Note 2)
θ_{JA} ---------- 24°C/W
$\theta_{JC\ TOP}$ ---------- 15°C/W

Recommended Operating Conditions

VS ---------- 5.5V to 25V
VDD ---------- 3.15V to 5.25V
Digital pin ---------- -0.3V to 5.5V
DC Output Maximum Current (Note 3) ---------- 0.55A
Junction Temperature Range ---------- -40°C to 125°C

Electrical Characteristics

(-40°C <T_A < 125°C, 5.5V< VS <25V, 3.15V<VDD<5.25V, EN=VDD, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Power Supplies						
VS Operation Voltage	V_{VS}		5.5		25	V
VS Operating Supply Current	I_{VS}	EN=VDD, 5.5V< VS <25V No Load		2.5	5	mA
VS Sleep Mode Current	I_{VS_SLEEP}	VS =13.2V, VDD=0V, No Load		0.3	2	μA
VS Undervoltage Lockout Voltage	V_{UVLO_FALL}	VS Falling	3.7	4.1	4.4	V
	V_{UVLO_HYS}		100		400	mV
VS Overvoltage Protection	V_{OVP_RISE}	VS Rising	26	28	30	V
	V_{OVP_HYS}		2	2.5	3	V
VDD Operation Voltage	V_{VDD}		3.15		5.25	V
VDD Power on Reset Threshold	V_{POR_ON}			2.8	3	V
VDD Power off Reset Threshold	V_{POR_OFF}			2.55	2.8	V
VDD Operating Supply Current	I_{VDD}	EN=CSB=VDD, SI=SCLK=0V		1.8	3	mA
VDD Sleep Mode Current	I_{VDD_SLEEP}	CSB=VDD, EN=SI=SCLK=0V		0.8	1.7	μA
Logic Level Input(EN, SI, SCLK, CSB)						
Input Low Voltage	V_{IL}				0.6	V
Input High Voltage	V_{IH}		2			
Input Pull-down Resistance (EN, SI, SCLK)	R_{PDX}	EN=SI=SCLK=5V	50	125	250	kΩ
Input Pull-up Resistance (CSB)	R_{PUCSB}	CSB=0V	50	125	250	kΩ
Input capacitance	C_{CAPINX}	(Note4)			15	pF
Logic Level Output(SO)						
Output Low Voltage	V_{OL}	Iout=-1.6mA			0.1	V
Output High Voltage	V_{OH}	Iout=1mA	VDD -0.4			V
Tri-state Leakage Current	I_{SOLK}	CSB=5V	-1		1	μA
Tri-state Output Capacitance	C_{SO}	CSB=VDD, 0V<VDD<5.25V, (Note4)			15	pF
Power MOSFETs						
High Side MOSFETs on Resistance	$R_{DS(ON)}$	Iout=-500mA VS=13.2V		0.75	1.6	Ω
Low Side MOSFETs on Resistance		Iout=500mA VS=13.2V		0.7	1.5	
Source Leakage Current	I_{source_LC}	OUTx=0V, VS=36V, VDD=5V,	-5			μA
		OUTx=0V, VS=13.2V, VDD=5V,	-1			μA
Sink Leakage Current	I_{sink_LC}	OUTx=36V, VS=36V, VDD=5V,			5	μA
		OUTx=13.2V, VS=13.2V, VDD=5V,			1	μA
Protections						
Thermal Warning Temperature	T_{WARN}		120	140	170	°C
Thermal Warning Hysteresis	T_{WARN_HYS}			20		°C
Thermal Shutdown Temperature	T_{SD}		150	165	200	°C
Thermal Shutdown Hysteresis	T_{HYS}			20		°C
Over Current Shutdown Threshold(Source)	I_{OCSO}	VDD=5V, VS=13.2V	-1.8	-1.2	-0.8	A
Over Current Shutdown Threshold (Sink)	I_{OCSI}	VDD=5V, VS=13.2V	0.8	1.2	1.8	A
Over Current Shutdown Delay Time	t_{oc}	VDD=5V, VS=13.2V	10	25	50	μs
Open Load Detection Threshold (Low-Side)	I_{UL_L}	VDD=5V, VS=13.2V	3	8	15	mA
Open Load Detection Delay Time	t_{UL}	VDD=5V, VS=13.2V	2000	3000	4000	μs
Open Load Detection Threshold (High-Side)	I_{UL_H}	VDD=5V, VS=13.2V	3	8	15	mA
Difference Between Shutdown and Limit Current	$I_{LIM}\_I_{OC}$	VDD=5V, VS=13.2V	0	0.5	1	A
Driver Timing						
High Side Turn on Time	t_{HON}	VS=13.2V, Rload=39Ω		5	13	μs
High Side Turn off Time	t_{HOFF}	VS=13.2V, Rload=39Ω		3	6	μs
Low Side Turn on Time	t_{LON}	VS=13.2V, Rload=39Ω		6.5	13	μs
Low Side Turn off Time	t_{LOFF}	VS=13.2V, Rload=39Ω		2	6	μs
High Side Rise Time	t_{HR}	VS=13.2V, Rload=39Ω		4	8	μs
High Side Fall Time	t_{HF}	VS=13.2V, Rload=39Ω		2	4	μs
Low Side Rise Time	t_{LR}	VS=13.2V, Rload=39Ω		1	3	μs
Low Side Fall Time	t_{LF}	VS=13.2V, Rload=39Ω		1	3	μs
Non-overlap Time	t_{HOFF_LON}	High side turn off to low side turn on, During PWM Mode; VS=13.2V (Note4)	1.5			μs
	t_{LOFF_HON}	Low side turn off to High side turn on, During PWM Mode; VS=13.2V (Note4)	1.5			μs

Serial Peripheral Interface

(-40°C <T_A < 125°C, 5.5V< V_S <25V, 3.15V<VDD<5.25V, EN=VDD, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
SCLK Frequency	f_{CLK}	VDD=5V (Note4)			5	MHz
		VDD=3.15V (Note4)			2	
SCLK High Time	t_{CLKH}	(Note4)	85			ns
SCLK Low Time	t_{CLKL}	(Note4)	85			ns
SCLK Setup Time	t_{CLK_ST}	(Note4)	85			ns
SI Setup Time	t_{SI_ST}	(Note4)	50			ns
SI Hold Time	t_{SI_HD}	(Note4)	50			ns
CSB Setup Time	t_{CS_ST}	(Note4)	100			ns
CSB High Time	t_{CSH}	(Note4)	5			μs
SO Enable after CS Falling Edge	t_{SOEN}	VDD=5V, (Note4)			200	ns
SO Disable after CS Rising Edge	t_{SODIS}	VDD=5V, (Note4)			200	ns
SO Rise Time	t_{SOR}	C_{load}=40pF, (Note4)		10	25	ns
SO Fall Time	t_{SOF}	C_{load}=40pF, (Note4)		10	25	ns
SO Valid Time	t_{SOV}	C_{load}=40pF, SCLK rise to SO 50%, (Note4)		20	50	ns
EN Low Valid Time	t_{ENL}	VDD=5V, EN going low 50% to OUTx turning off 50%	10			μs
EN High to SPI Valid	t_{enh_SPIV}	(Note4)			100	μs

Note 1: Stresses listed as the above "Absolute Maximum Ratings" may cause permanent damage to the device. These are for stress ratings. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied.

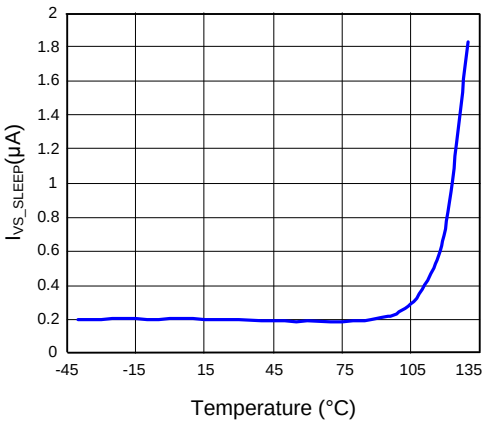
Note 2: θ_{JA} is measured in the natural convection at T_A = 25°C on high-effective four-layer thermal conductivity test board following JESD51-5, -7.

Note 3: Power dissipation and thermal limits must be observed.

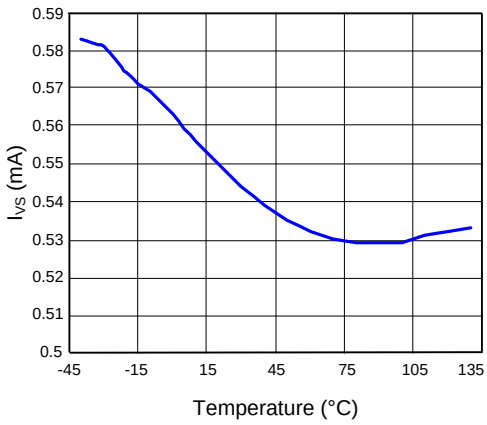
Note 4: Guaranteed by design.

Typical Performance Characteristics

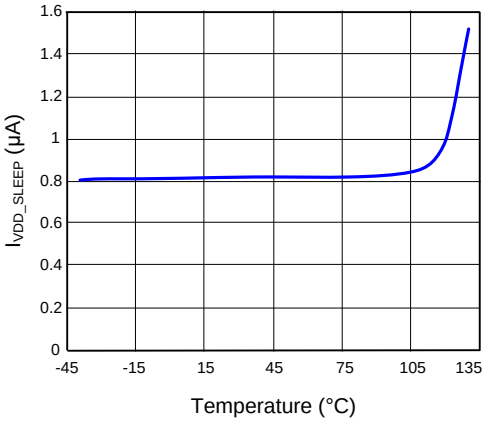
VS Sleep Mode Current
(VS=13.2V)



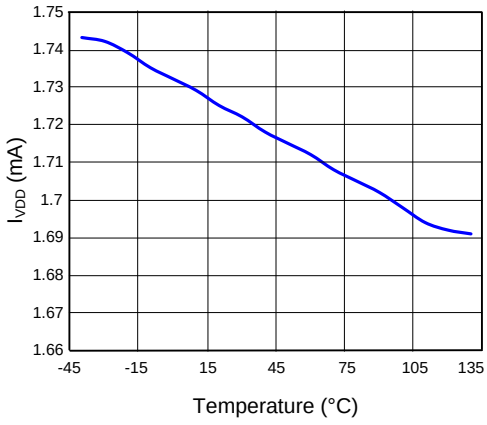
VS Operating Supply Current
(VS=13.2V)



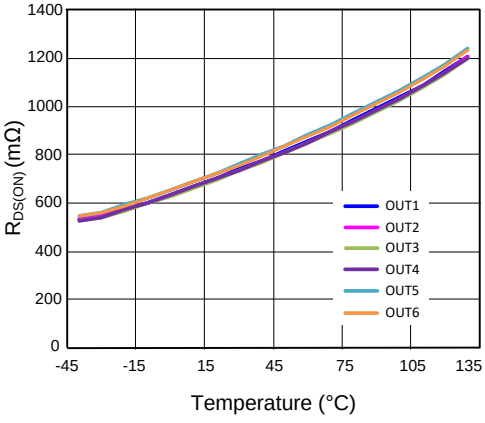
VDD Sleep Mode Current
(VS=13.2V)



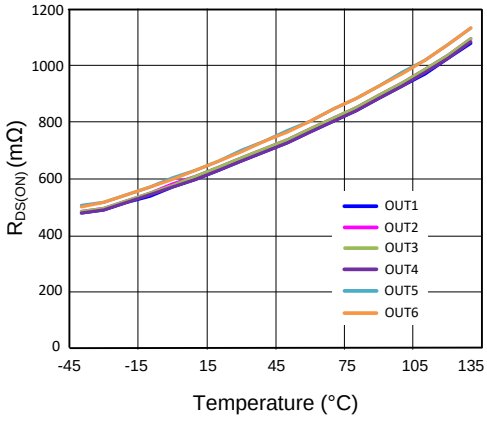
VDD Operating Supply Current
(VS=13.2V)



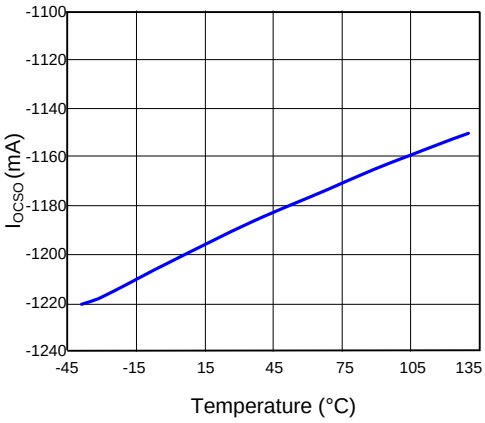
High Side MOSFETs on Resistance
(VS = 13.2V)



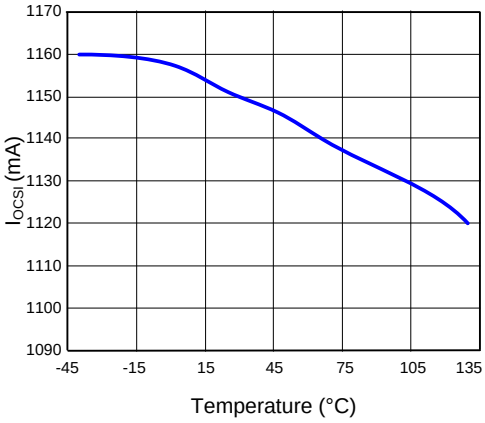
Low Side MOSFETs on Resistance
(VS = 13.2V)



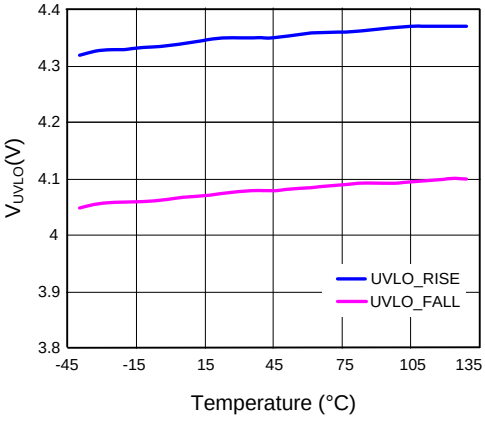
High Side MOSFETs Over Current Limit
(VS=13.2V)



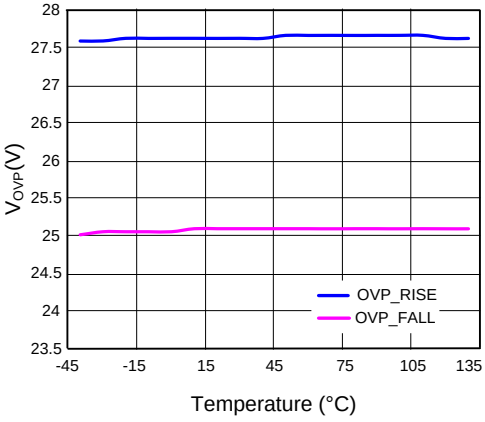
Low Side MOSFETs Over Current Limit
(VS=13.2V)



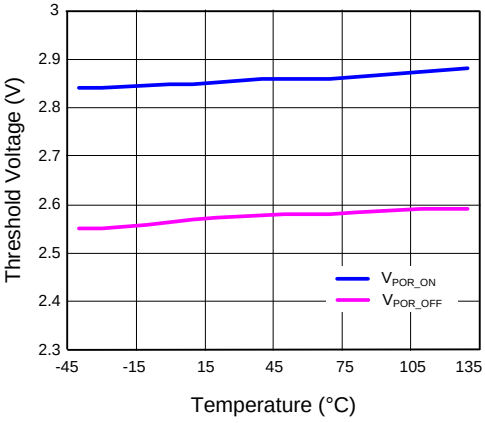
VS Undervoltage Lockout
(VDD=5V)



VS Overvoltage Protection
(VDD=5V)

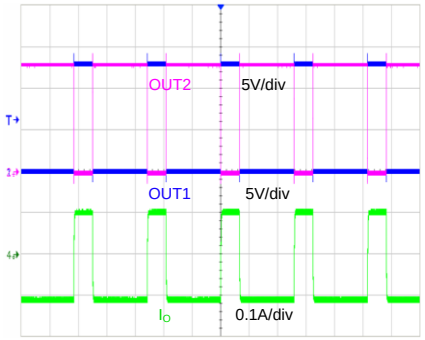


VDD Power-on-reset and VDD Power-off-reset
(VS=13.2V)



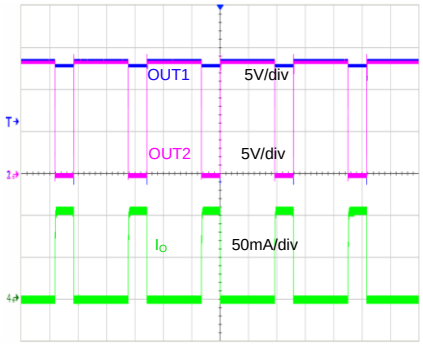
Operation Waveform

Active Free-wheeling
(VS=13.2V Io=100mA Duty=25% Frequency=80Hz)



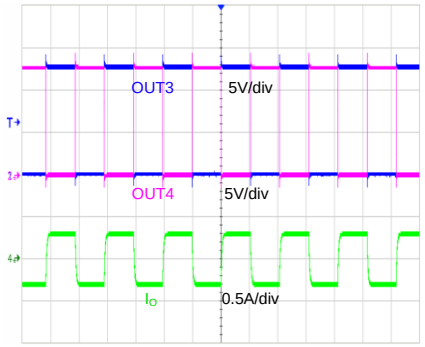
Time (5ms/div)

Passive Free-wheeling
(VS=13.2V Io=100mA Duty=25% Frequency=80Hz)



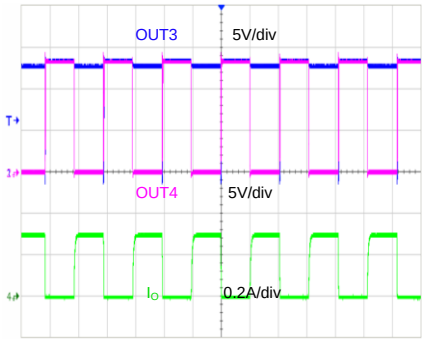
Time (5ms/div)

Active Free-wheeling
(VS=13.2V Io=300mA Duty=50% Frequency=100Hz)



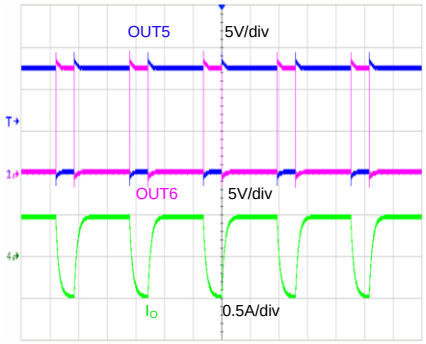
Time (5ms/div)

Passive Free-wheeling
(VS=13.2V Io=300mA Duty=50% Frequency=100Hz)



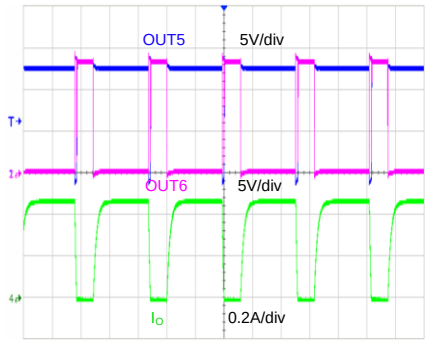
Time (5ms/div)

Active Free-wheeling
(VS=13.2V Io=500mA Duty=75% Frequency=200Hz)



Time (2ms/div)

Passive Free-wheeling
(VS=13.2V Io=500mA Duty=75% Frequency=200Hz)



Time (2ms/div)

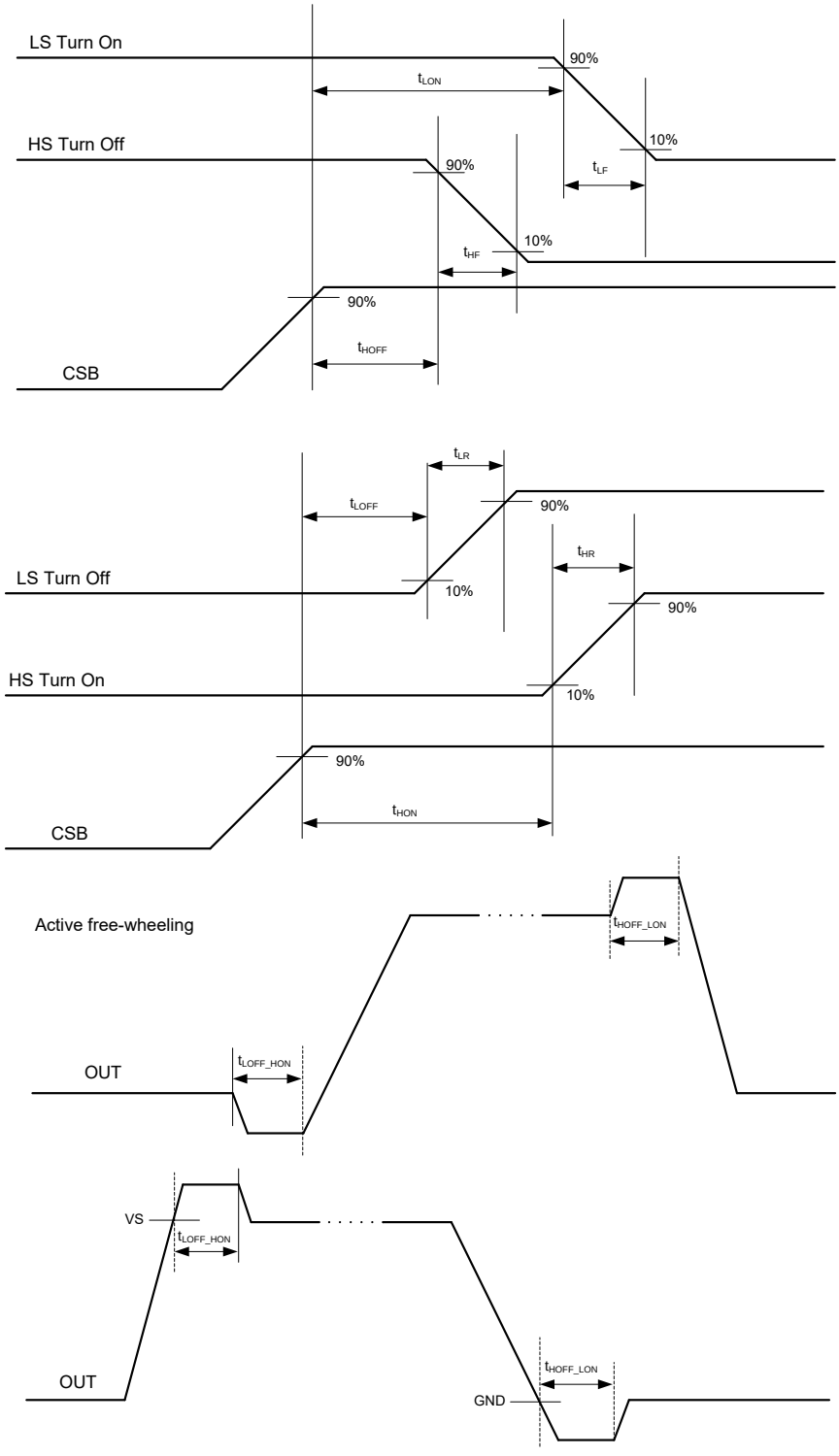


Figure4. Driver Timing

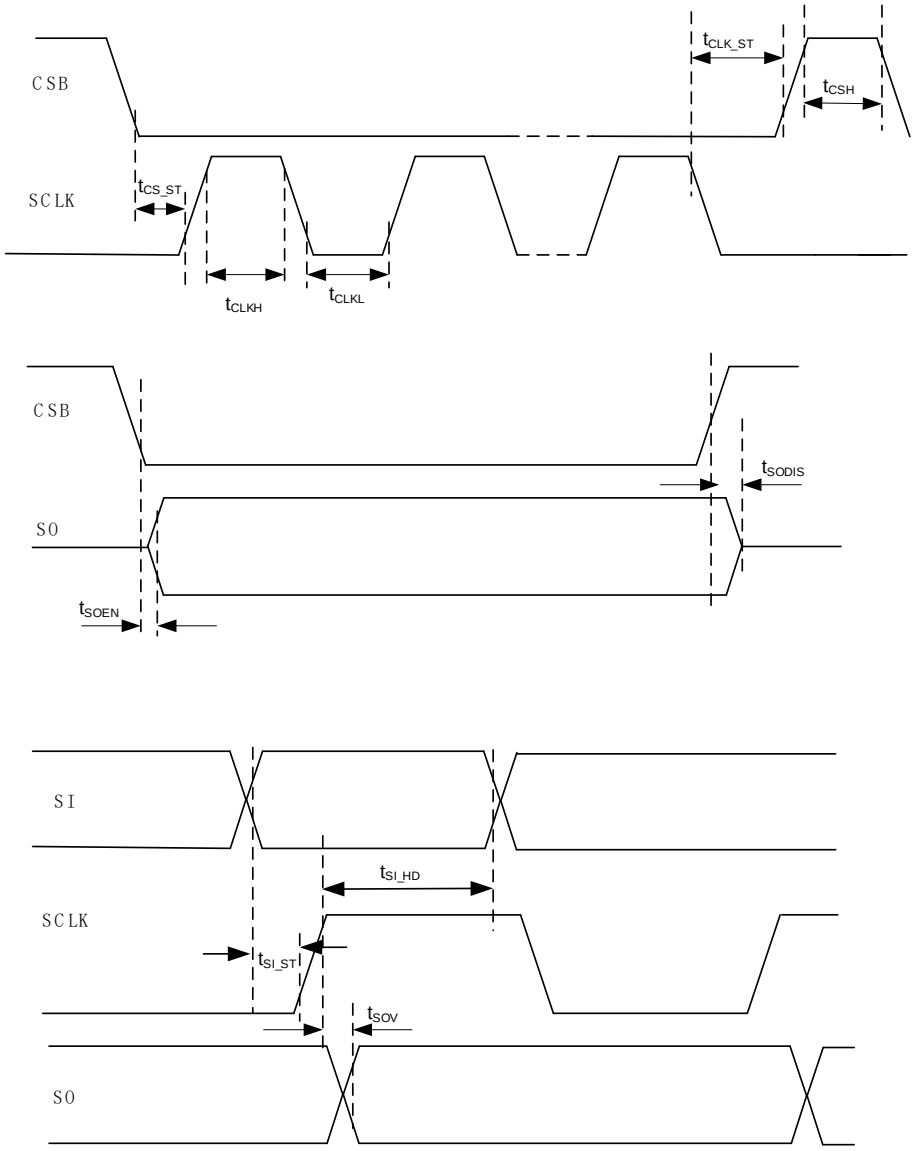


Figure5. SPI Time Sequence

Functional Description

The SA52106 is a six half-bridge motor driver solution for automotive, industrial and other mechatronic applications. It can be configured as 3 independent H-bridge. Each of the output is characterized for a max 550mA DC load. Internal thermal shutdown is provided to protect the IC. All the control logic and fault report is handled via SPI. An internal pull down circuit is designed to ensure the IC is off if the enable signal is lost. In addition, the enable signal can make the IC enter sleep mode in which no data is stored and all the registers are cleared.

Power Supply

VS powers the MOSFETs, and VDD powers the logic circuits. A rising edge on VDD crossing V_{POR_ON} triggers an internal Power-On Reset (POR) to initialize the IC at power-on. All the internal registers are cleared on VDD POR.

Reset Behavior

VDD Undervoltage Reset:

The SPI interface shall not function if VDD is below the voltage, V_{POR_OFF}. The digital block will be deactivated, the logic contents are cleared and the output stages are switched off. The digital block is initialized once VDD is above the undervoltage threshold, V_{POR_ON}. Then the NPOR bit is reset (NPOR=0 in SYS_DIAG1 and Global Status Register).

Reset on EN pin:

If the EN pin is pulled down, the logic content is reset and the device enters sleep mode. The reset event is reported by the NPOR bit (NPOR=0) once the SA52106 is in normal mode (EN=High; VDD>V_{POR_ON})

Driving Control

The output is controlled via SPI. The device can be configured as H-bridge, high-side or low-side driver. The half-bridge outputs of the device are intended to drive motor loads. These outputs can either be driven continuously or PWM enabled via SPI. For example, HS1 and LS2 used to drive a motor in a continuously driven way, the SPI commands shall be sent as follows:

- Active HS1: Bit HB1_HS_EN in HB_ACT_1_CTRL register
- Active LS2: Bit HB2_LS_EN in HB_ACT_1_CTRL register

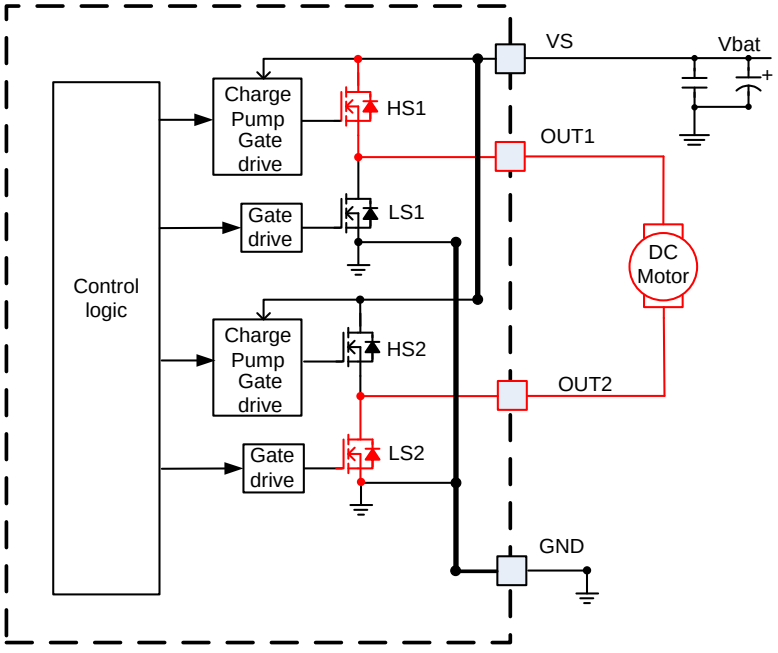


Figure 6. Be Driven Continuously

Half-bridge operation with PWM enabled

Each half-bridge can be configured into PWM mode to drive an inductive load (e.g. DC brush motor). and has been allocated a maximum of three PWM channels with individual duty cycle settings with 8-bit resolution. Different control profiles can result in flexible PWM operation while driving loads.

PWM frequency and duty cycle can be changed on demand during PWM operation of the desired half-bridge output. If driving motor loads, active or passive free-wheeling configuration is available via SPI to select the speed at which the inductive current can decay over the full-bridge circuit. The default setting is passive free-wheeling.

Table PWM capability and frequency selection per half-bridge output

Control Register: HBx_MODEn(n=0,1)	**PWM Frequency 80Hz (Control Register: PWM_CH_FREQ_CTRL)**	**PWM Frequency 100Hz (Control Register: PWM_CH_FREQ_CTRL)**	**PWM Frequency 200Hz (Control Register: PWM_CH_FREQ_CTRL)**
PWM Channel 1	PWM_CH1_FREQ_n(n=0, 1) Bit'01_B'	PWM_CH1_FREQ_n(n=0,1) Bit'10_B'	PWM_CH1_FREQ_n(n=0, 1) Bit'11_B'
PWM Channel 2	PWM_CH2_FREQ_n(n=0, 1) Bit'01_B'	PWM_CH2_FREQ_n(n=0,1) Bit'10_B'	PWM_CH2_FREQ_n(n=0, 1) Bit'11_B'
PWM Channel 3	PWM_CH3_FREQ_n(n=0, 1) Bit'01_B'	PWM_CH3_FREQ_n(n=0,1) Bit'10_B'	PWM_CH3_FREQ_n(n=0, 1) Bit'11_B'

An illustration is shown in Figure7 with OUT1 and OUT2 driving a DC brush motor. With this configuration, HS1 is permanently driven while LS2 is driven in PWM operation. HS2 serves to active free-wheeling (FW) the motor current load, reducing the power dissipation of the device.

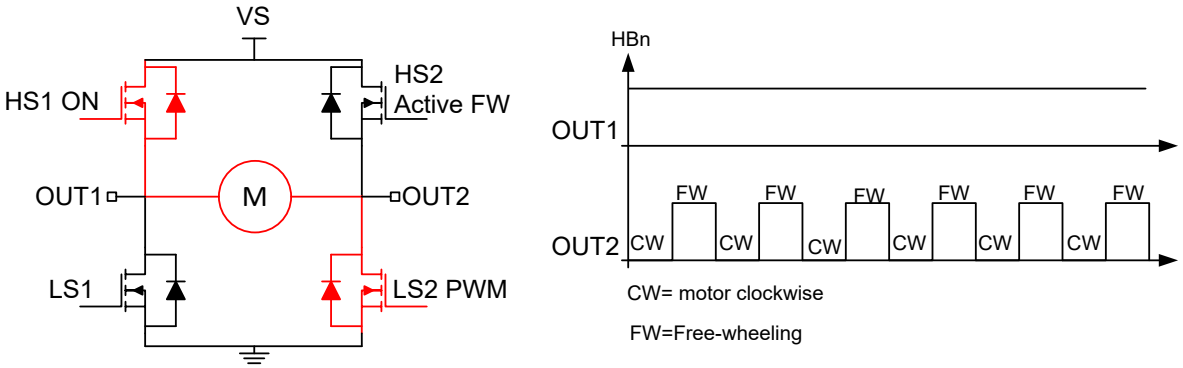


Figure7. PWM Operation on OUT2

Assuming HBx_MODE = 00 and both HSx and LSx are considered off (tri-state). The suggested SPI control commands for proper PWM operation are:

Option 1: The consider outputs are not put in parallel with another one

- Configure the frequency to 00 (PWM is stopped and off) for selected PWM channel
- Configure active or passive free-wheeling of the inductive decay current in FW_OL_CTRL register
- Assign an appropriate PWM channel for selected half-bridge output in HB_MODE_CTRL register
- Configure the duty cycle of the selected half-bridge output in PWM_DC_CTRL register
- Select the PWM frequency in PWM_CH_FREQ_CTRL register to begin the PWM period
- Active the channel to be driven in PWM operation: HSn or LSn in the HB_ACT_CTRL register

Option 2: Outputs controlled by different control registers are put paralleled. This sequence ensures that corresponding HS or LS are activated simultaneously

- Configure the frequency to 00 (PWM is stopped and off) for selected PWM channel
- Configure active or passive free-wheeling of the inductive decay current in FW_OL_CTRL register

- Assign an appropriate PWM channel for selected half-bridge output in HB_MODE_CTRL register
- Configure the duty cycle of the selected half-bridge output in PWM_DC_CTRL register
- Active the channel to be driven in PWM operation: HSn or LSn in the HB_ACT_CTRL register
- Select the PWM frequency in PWM_CH_FREQ_CTRL register to begin the PWM period

Careful attention should be paid to the free-wheeling configuration of the half-bridge required to be driven in PWM operation. For example, in the event a high-side channel is activated and assigned a PWM channel, and active free-wheeling is selected, and a frequency mode of '00' (PWM is stopped an off) is configured in the PWM_CH_FREQ_CTRL register, then the respective high-side channel will be configured low and the adjacent low-side channel within the half-bridge will be enabled. This is a result of enabling active free-wheeling.

SPI Communication

The device supports nonstandard 16-bit SPI to be controlled. The commutation is performed by LSB clocked in first. SCLK must be Low during CSB falling edge (Clock Polarity = 0). The SPI interface is a synchronous serial interface for address and data transfer at bit rates of up to 5MHz. It is configured in 8-bit bytes designed to interface with a SPI bus. Four pins are used to communicate on the SPI: SCLK (synchronous clock), CSB (chip select, active low), SI (data input to the device for write operations,), and SO (data output from the device for read operations). As shown in Figure 8.

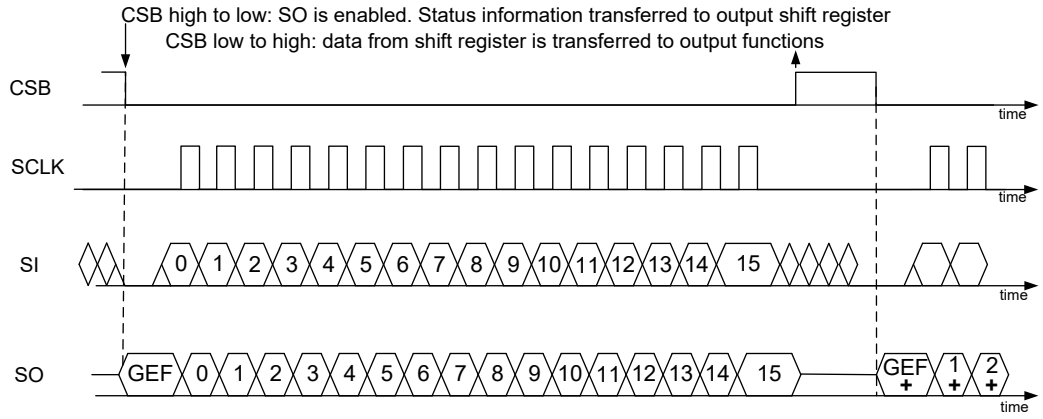


Figure 8. SPI Timing

The state of SI is sampled with every rising edge on SCLK and shifted into the input register with every falling edge on SCLK. As shown in Figure 9.

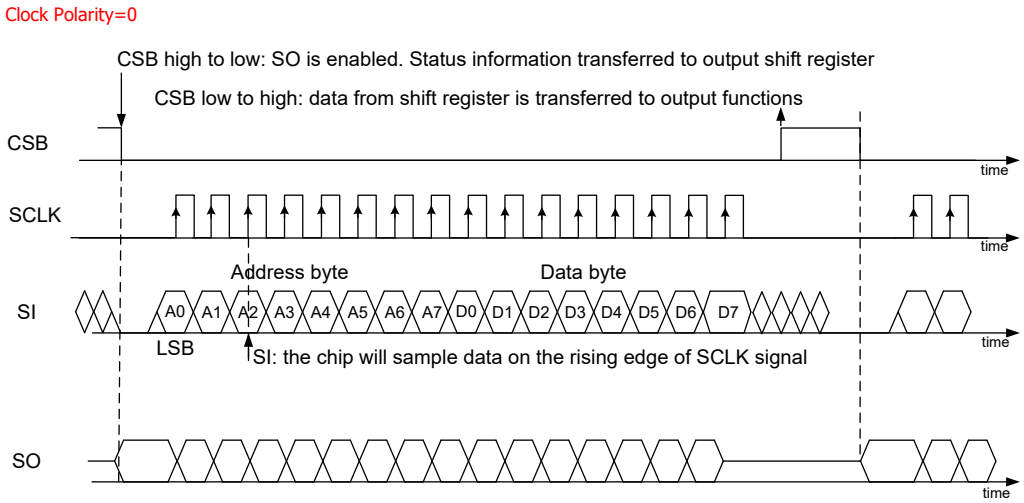


Figure 9. SI Data Transfer Timing

The state of SO is shifted out of the output register at every rising edge on SCLK and need to be sampled by MCU to decode at every falling edge on SCLK. As shown in Figure 10.

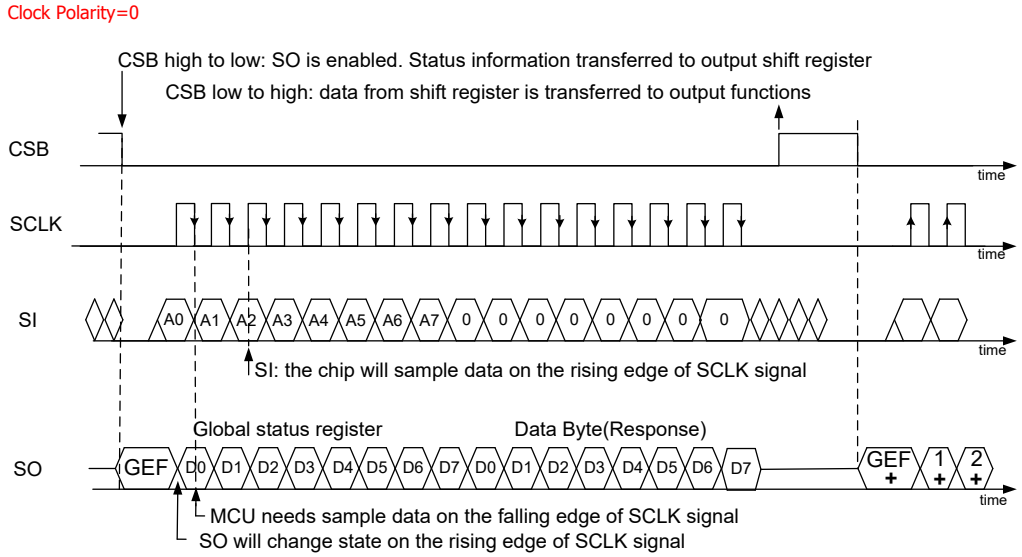


Figure 10. SO Data Transfer Timing

SPI messages are only recognized if a minimum set time, t_{enh_SPIV}, is observed upon rising edge of the EN pin.

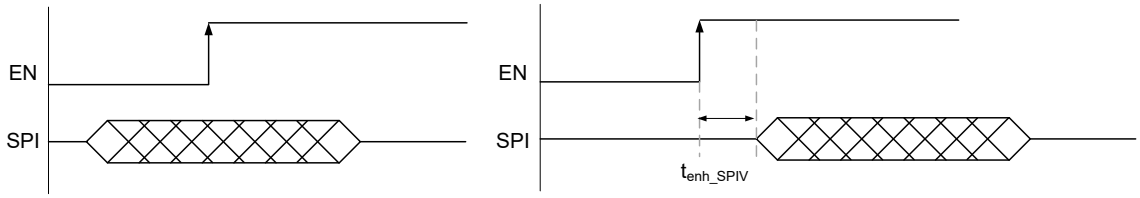


Figure 11. Setup Time from EN Rising Edge to First SPI Communication

Global Error Flag

A logic OR combination between Global Error Flag (GEF) and the signal present on SI is reported on SO between CSB falling edge and the first SCLK rising edge. GEF is set if the device comes from a Power On Reset (POR) or a fault condition is detected.

It is possible to check if the device has detected a fault by reading the GEF without SPI clock pulse.

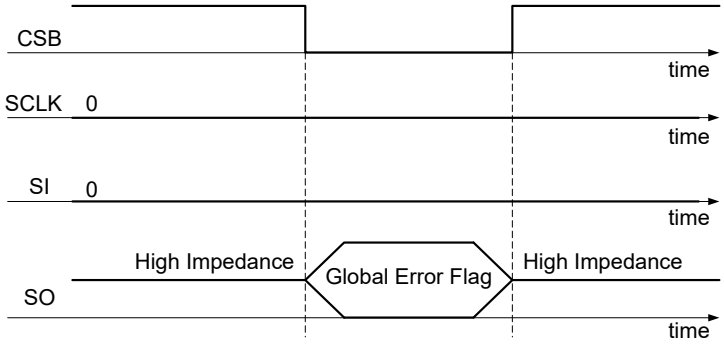


Figure12. SO Behavior with 0-clock Cycle

Global Status Register

The SO shifts out the Global Status Register during the first eight SCLK cycles. This register provides an overview of the device status. Different bits represent different error conditions:

- SPI protocol error (SPI_ERR bit)
- Load Error (LE bit): logical OR between Open load(OL) and Overcurrent(OC) failures
- VS Undervoltage (VS_UV bit)
- VS Overvoltage (VS_OV bit)
- Negated Power On Reset (NPOR bit)
- Temperature Shutdown (TSD bit)
- Temperature Pre-warning (TPW bit)

Note: The Global Error Flag is a logic OR combination of every bit of the Global Status Register with the exception of NPOR: GEF= (SPI_ERR) OR(LE) OR(VS_UV) OR(VS_OV) OR (NOT(NPOR)) OR(TSD) OR(TPW)

Table Failure reported in the Global Status Register and Global Error Flag

Type of Error	Failure reported in the Global Status Register	Global Error Flag
SPI protocol error	SPI_ERR=1	1
Load Error	LE=1	1
VS Undervoltage	VS_UV=1	1
VS Overvoltage	VS_OV=1	1
Negated Power On Reset	NPOR=0	1
Temperature Shutdown	TSD=1	1
Temperature Pre-warning	TPW=1	1
No error and no Power On Reset	SPI_ERR=0 LE=0 VS_UV=0 VS_OV=0 **NPOR=1** TSD=0 TPW=0	0

Note: The default value (after Power On Reset) of NPOR is 0, therefore the default value of GEF is 1.

SPI protocol error detection

The SPI incorporates an error flag in the Global Status Register (SPI_ERR, Bit 7) to supervise and preserve the data integrity. If an SPI protocol error is detected during a given frame, the SPI_ERR bit is set in the next SPI communication.

The SPI_ERR bit is set in the following error conditions:

- After CSB is Low, the number of SCLK clock pulses received is not a multiple of 16
- The microcontroller sends an SPI command to an unused address. In particular, SI stuck to High is reported in the SPI_ERR bit
- The LSB of an address byte is not set to 1. In particular, SI stuck to Low is reported in the SPI_ERR bit
- A clock polarity error is detected: the incoming clock signal was High during CSB rising or falling edges.

For a correct SPI communication:

- SCLK must be Low for a minimum t_{CLK_ST} before CSB falling edge and t_{CS_ST} after CSB rising edge
- SCLK must be Low for a minimum t_{CLK_ST} before CSB rising edge and t_{CS_ST} after CSB falling edge

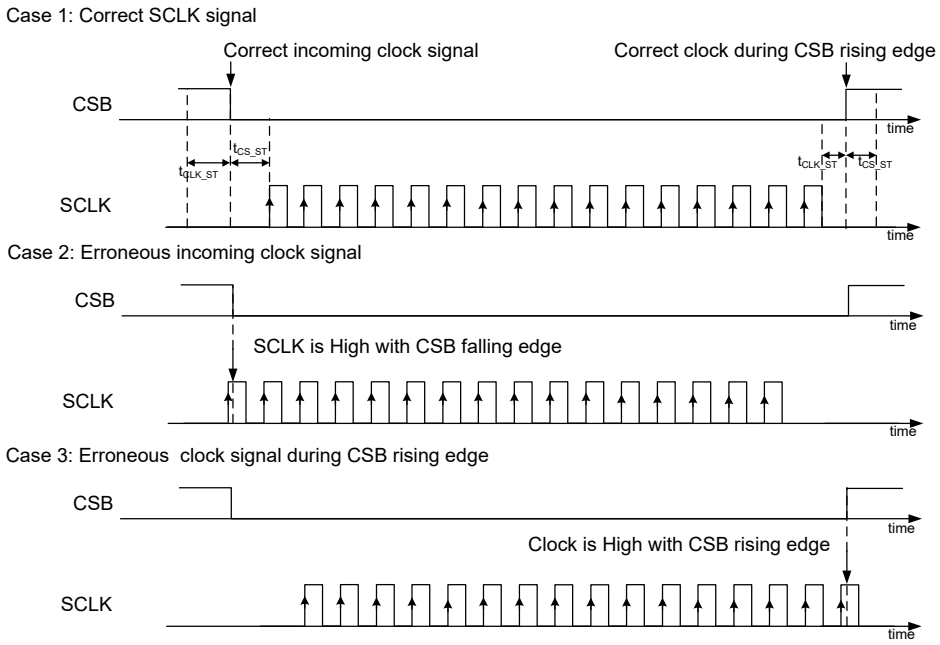


Figure13. Clock Polarity Error

SPI configuration

Each SPI communication starts with one address byte followed by one data byte. The LSB of the address byte must be set to '1'. The address bytes specifics:

- The type of operation: READ (OP bit=0) or WRITE (OP bit=1) of the configuration bits, and READ (OP bit=0) or CLEAR (OP bit=1) of the status bits.
- The target register address (A[6:2])

While the microcontroller sends the address byte on SI, SO shifts out GEF and the Global Status Register. A further data byte (Bit15...8) is allocated to either configure the half-bridges or retrieve status information of the device.

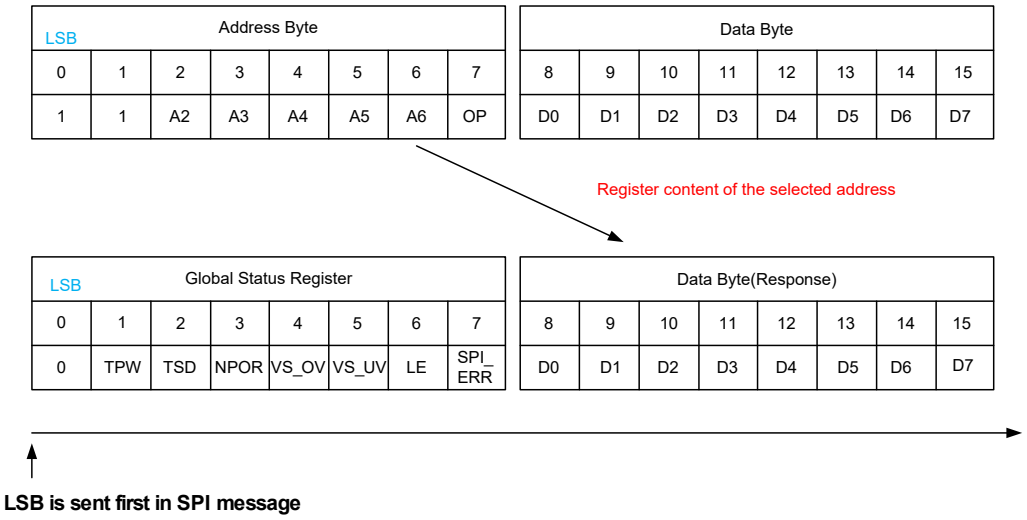


Figure14. SPI Operation Mode

The in-frame response characteristic enables the microcontroller to read the contents of the addressed register within the SPI command.

Status register is changed during SPI communication

If a new failure occurs after the transfer of the data byte(s), i.e. between the end of the last address byte and the CSB rising edge, this failure will be reported in the next SPI frame.

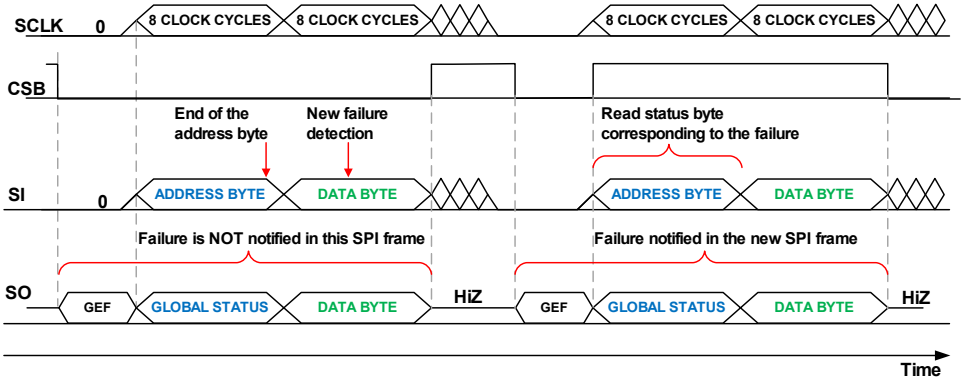


Figure15. Status register is changed during transfer of data byte

No information is lost, even if a status register is changed during a SPI frame, in particular during a Read and Clear command. For example:

- The microcontroller sends a Read and Clear command to a status register.
- The device detects during the transfer the data byte(s) a new fault condition, which is normally reported in the target status register

The incoming Clear command will be ignored, so that the microcontroller can read the new failure in the subsequent SPI frames.

Data inconsistency between the Global Status Register and the data byte (status register) within the same SPI frame is possible if:

- An open load or overcurrent error is detected during the transfer of the data byte
- The target status register corresponds to the new detected failure

In this case the new failure:

- Is not reported in the Global Status Register of the current SPI frame but in the next one
- Is reported in the data byte of the current SPI frame.

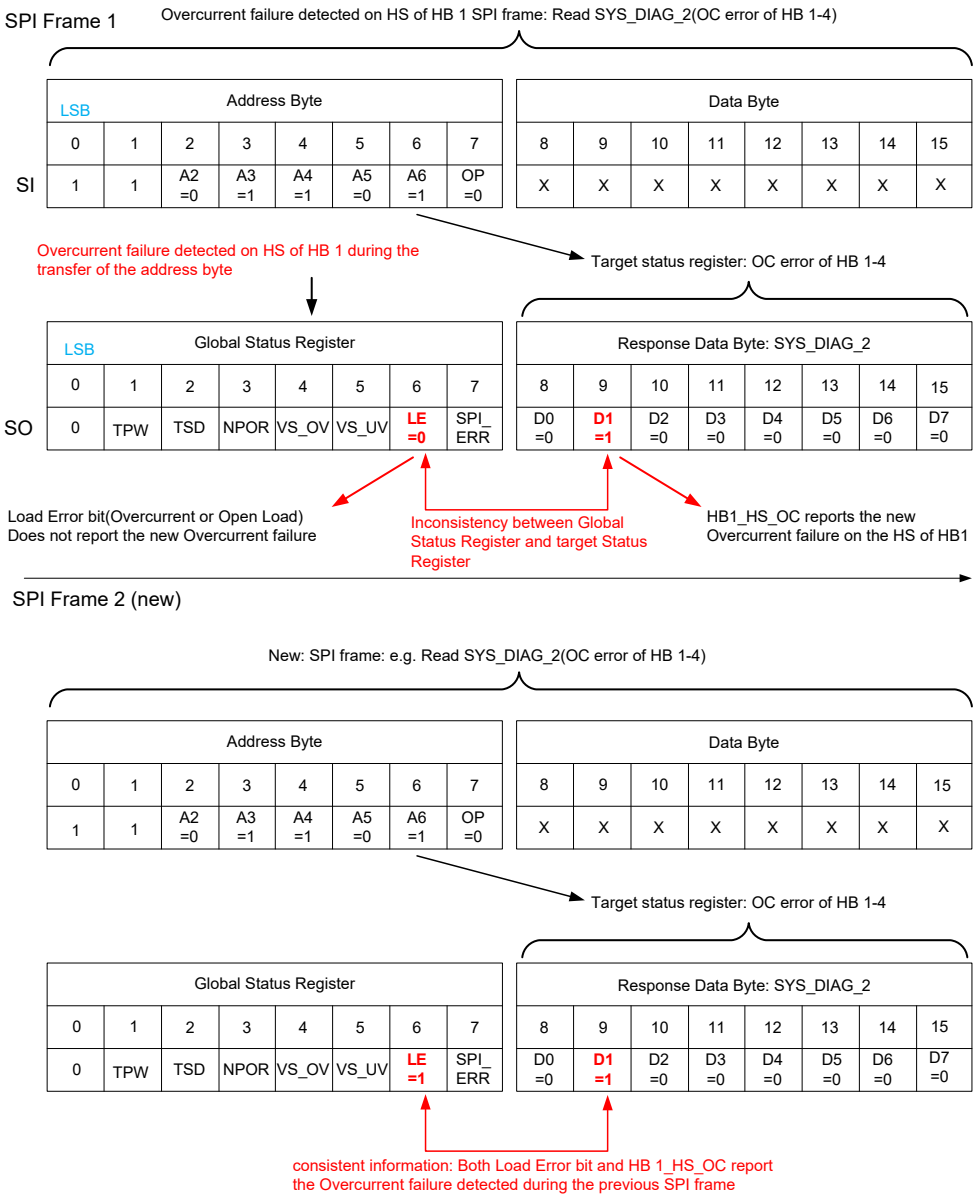


Figure16. Example of Inconsistency between Global Error Flag and Status Register when a Status Bit is Changed during the Transfer of an Address Byte

Device Protection

The half-bridge drivers of device can be controlled and diagnosed with SPI interface. This device has embedded protective functions such as undervoltage, overvoltage, overcurrent, short circuit, thermal warning and thermal shutdown. The following table provides a summary of fault conditions, protection mechanisms and recovery states embedded in the device.

Fault condition	Error Flag (EF) behavior	Error bit: Status Register	Output Protection mechanism	Output error state	Output and error Flag (EF) recovery
Overcurrent	Latch	1. Load Error bit, LE (bit 6) in SYS_DIAG 1: Global Status 1 Register 2. Localized error for each HS and LS channel of half-bridge, HBn_HS_OC and HBn_LS_OC bits in SYS_DIAG_2, SYS_DIAG_3 status registers.	Error output shutdown and latched	High-Z	Half_bridge control Bits remain set despite error, However, the Output state is shutdown. Clear EF to Reactive output stage
Open load	Latch	1. Load Error bit, LE (bit 6) in SYS_DIAG 1: Global Status 1 Register 2. Localized error for each HS and LS channel of half-bridge, HBn_HS_OL and HBn_LS_OL bits in SYS_DIAG_5, SYS_DIAG_6 status registers.	None	No State change	An open load detection does not change the state of the output. EF to be cleared.
Temperature pre-warning	Latch	Global error bit 1, TPW in SYS_DIAG_1: Global Status 1 register	None	No State change	Not applicable
Temperature shutdown	Latch	Global error bit 2, TSD in SYS_DIAG_1: Global Status 1 register	All outputs shutdown and latched	High-Z	Half_bridge control bits remain set despite error, however, the output stage is shutdown. Clear EF to reactivate output stage.
Power supply failure due to undervoltage	Latch	Global error bit 5, VS_UV in SYS_DIAG_1: Global Status 1 register	All outputs shutdown and automatically recover.	All outputs shutdown and automatically recover.	Half-bridge control bits remain set despite error; however, the output stage is shutdown. They will automatically be reactivated once the power supply recovers. EF to be cleared.
Power supply failure due to overvoltage	Latch	Global error bit 4, VS_OV in SYS_DIAG_1: Global Status 1 register	All outputs shutdown and automatically recover.	All outputs shutdown and automatically recover.	Half-bridge control bits remain set despite error, however the output stage is shutdown. They will automatically be reactivated once the power supply recovers. EF to be cleared.

Overcurrent Protection (OCP)

The device offers over current protection. Monitoring the current on the high side and low side drivers at any time, once the current exceeds the overcurrent shutdown detection threshold, the corresponding HS or LS driver is latched off and the corresponding error bit, HBn_HS_OC or HBn_LS_OC is set and latched after the specified shutdown time, t_{oc}. See the figure for more detail. A global load error bit, LE, contained in the global status register, SYS_DIAG_1, is also set for ease of error scanning by the application software. The power switch remains deactivated as long as the error bit is set. To resume normal functionality of the power switch (in the event the overcurrent condition disappears or to verify if the failure still exists) the microcontroller shall clear the error bit in the respective status register to reactivate the desired power switch.

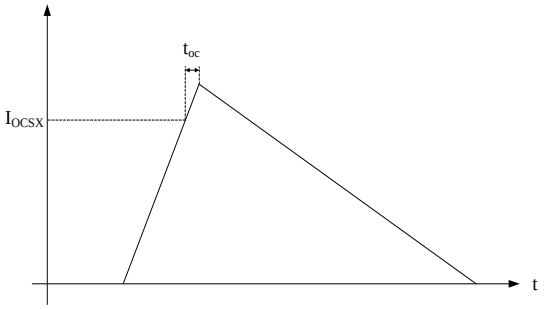


Figure17. Over Current Timing Diagram

Short Circuit Protection (SCP)

When short circuit conditions are on both high and low side devices, that is, a short to ground, or to power supply, or across the motor winding all result in a short circuit protection. That is, the short current would decrease to the current regulation point and the corresponding HS and LS driver is latched off after the specified current regulation time, t_{oc}. Meanwhile, the corresponding error bit, HBn_HS_OC or HBn_LS_OC is set and latched.

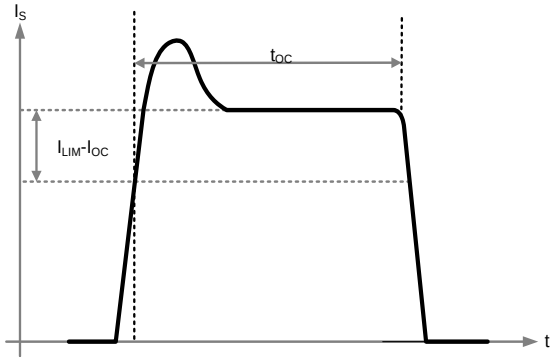


Figure 18. Short Current Waveform

Undervoltage Lockout (UVLO)

In the event the supply voltage VS drops below the switch off voltage V_{UVLO_FALL}, all output stages are switched off, however, the logic information remains intact and uncorrupted. The VS under-voltage error bit, VS_UV, located in SYS_DIAG_1: Global Status 1 status register, will be set and latched. If VS rises again and reaches the switch on voltage threshold, the power stages will automatically be activated. The VS_UV error bit should be cleared to verify if the supply disruption is still present.

In the event the VDD logic supply decreases below the undervoltage threshold, V_{POR_OFF}, the SPI interfaces shall no longer be functional and the SA52106 will enter reset. The digital block will be initialized and the output stages are switched off to high impedance. The undervoltage reset is released once VDD voltage levels are above the undervotage threshold, V_{POR_ON}. The reset event is reported in SYS_DIAG_1 by the NPOR bit (NPOR=0) once the SA52106 is in normal mode.

Overvoltage Protection (OVP)

In the event the supply voltage VS rises above the switch off voltage V_{OVP_RISE}, all output stages are switched off. The VS over-voltage error bit, VS_OV, located in SYS_DIAG_1: Global Status 1 status register, will be set and latched. If VS falls again and reaches the switch on voltage threshold, the power stages will automatically be activated. The VS_OV error bit should be cleared to verify if the overvoltage condition is still present.

Open Load Detection

Both HS and LS drivers are capable of detecting an open load in their activated state. If a load current lower than the open load detection threshold, I_{UL} for at least t_{UL} is detected at the activated switch, the corresponding error bit, HBn_HS_OL or HBn_LS_OL is set and latched. A global load error bit, LE, in the global status register, SYS_DIG_1: Global Status 1, is also set. However, the half-bridge output remains activated. The microcontroller must clear the error bit in the respective status register to determine if the open load is still present or disappeared.

Thermal Shutdown (TSD)

The device offers temperature warning and shutdown protection. If one or more temperature sensors reach the warning temperature, the temperature pre-warning bit, TPW is set. This bit is latched and can only be cleared via SPI, but the outputs stages remain activated. If one or more temperature sensors reach the temperature shutdown threshold, all outputs are switched off. The TSD bit in SYS_DIAG_1: Global Status 1 is set. All outputs will be activated when the TSD bit is cleared. To resume normal functionality of the power switch (in the event the over temperature condition disappears, or to verify if the failure still exists) the microcontroller shall clear the TSD bit in the status register to reactivate the respective power switch.

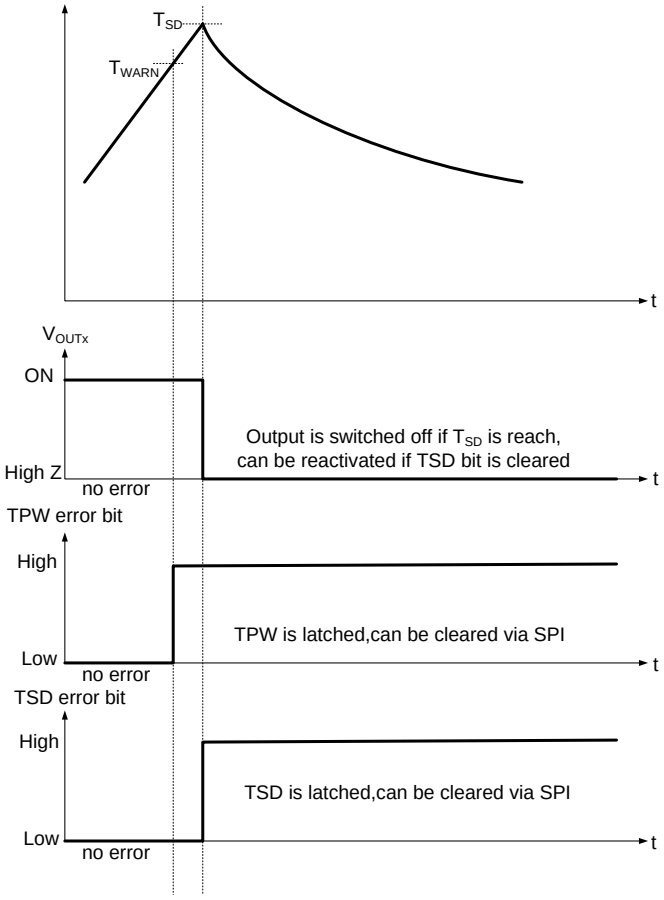


Figure 19. Over-temperature Behavior

SPI Bit Mapping

The SPI registers have been mapped as shown in Figure 20 and Figure 21 respectively. The control registers are READ/WRITE registers. To set the control register to READ, bit 7 of the address byte (OP bit) must be programmed to '0', otherwise '1' for WRITE. The status registers are READ/CLEAR registers. To CLEAR any status register, bit 7 of address byte must be set to '1', otherwise '0' for READ.

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	8 Data Bits [D7...D0] for Configuration & Status Information								8 Address Bits[A7...0]							
									Access type							
Control Registers	HB_ACT_1_CTRL								read/write	0	0	0	0	0	1	1
	HB_ACT_2_CTRL								read/write	1	0	0	0	0	1	1
	HB_MODE_1_CTRL								read/write	1	1	0	0	0	1	1
	HB_MODE_2_CTRL								read/write	0	0	1	0	0	1	1
	PWM_CH_FREQ_CTRL								read/write	0	1	1	0	0	1	1
	PWM1_DC_CTRL								read/write	1	1	1	0	0	1	1
	PWM2_DC_CTRL								read/write	0	0	0	1	0	1	1
	PWM3_DC_CTRL								read/write	1	0	0	1	0	1	1
	FW_OL_CTRL								read/write	0	1	0	1	0	1	1
Status Registers	SYS_DIAG_1: Global status 1								read/clear	0	0	1	1	0	1	1
	SYS_DIAG_2: OP ERROR_1_STAT								read/clear	1	0	1	1	0	1	1
	SYS_DIAG_3: OP ERROR_2_STAT								read/clear	0	1	1	1	0	1	1
	SYS_DIAG_5: OP ERROR_4_STAT								read/clear	0	0	0	0	1	1	1
	SYS_DIAG_6: OP ERROR_5_STAT								read/clear	1	0	0	0	1	1	1

Figure 20. SA52106 SPI Register mapping

	Registers	15	14	13	12	11	10
		Data Bits D7-D0					
		D7	D6	D5	D4	D3	D2
Control Registers	**Control Registers**						
	HB_ACT_1_CTRL	HB4_HS_EN	HB4_LS_EN	HB3_HS_EN	HB3_LS_EN	HB2_HS_EN	HB2_LS_EN
	HB_ACT_2_CTRL	reserved	reserved	reserved	reserved	HB6_HS_EN	HB6_LS_EN
	HB_MODE_1_CTRL	HB4_MODE1	HB4_MODE0	HB3_MODE1	HB3_MODE0	HB2_MODE1	HB2_MODE0
	HB_MODE_2_CTRL	reserved	reserved	reserved	reserved	HB6_MODE1	HB6_MODE0
	PWM_CH_FREQ_CTRL	reserved	reserved	PWM_CH3_FREQ_1	PWM_CH3_FREQ_0	PWM_CH2_FREQ_1	PWM_CH2_FREQ_0
	PWM1_DC_CTRL	PWM1_DC_CTRL_7	PWM1_DC_CTRL_6	PWM1_DC_CTRL_5	PWM1_DC_CTRL_4	PWM1_DC_CTRL_3	PWM1_DC_CTRL_2
	PWM2_DC_CTRL	PWM2_DC_CTRL_7	PWM2_DC_CTRL_6	PWM2_DC_CTRL_5	PWM2_DC_CTRL_4	PWM2_DC_CTRL_3	PWM2_DC_CTRL_2
	PWM3_DC_CTRL	PWM3_DC_CTRL_7	PWM3_DC_CTRL_6	PWM3_DC_CTRL_5	PWM3_DC_CTRL_4	PWM3_DC_CTRL_3	PWM3_DC_CTRL_2
	FW_OL_CTRL	FW_HB6	FW_HB5	FW_HB4	FW_HB3	FW_HB2	FW_HB1
Status Registers	**Status Registers**						
	SYS_DIAG_1:Global status 1	SPI_ERROR	LE	VS_UV	VS_OV	NPOR	TSD
	SYS_DIAG_2:OP ERROR_1_STAT	HB4_HS_OC	HB4_LS_OC	HB3_HS_OC	HB3_LS_OC	HB2_HS_OC	HB2_LS_OC
	SYS_DIAG_3:OP ERROR_2_STAT	reserved	reserved	reserved	reserved	HB6_HS_OC	HB6_LS_OC
	SYS_DIAG_5:OP ERROR_4_STAT	HB4_HS_OL	HB4_LS_OL	HB3_HS_OL	HB3_LS_OL	HB2_HS_OL	HB2_LS_OL
	SYS_DIAG_6:OP ERROR_5_STAT	reserved	reserved	reserved	reserved	HB6_HS_OL	HB6_LS_OL

	Registers	9	8	7	6	5	4	3	2	1	0
		Data Bits D7-D0		Address Bits A7...A0							
		D1	D0	Access Type							
Control Registers	**Control Registers**										
	HB_ACT_1_CTRL	HB1_HS_EN	HB1_LS_EN	read/write	0	0	0	0	0	1	1
	HB_ACT_2_CTRL	HB5_HS_EN	HB5_LS_EN	read/write	1	0	0	0	0	1	1
	HB_MODE_1_CTRL	HB1_MODE1	HB1_MODE0	read/write	1	1	0	0	0	1	1
	HB_MODE_2_CTRL	HB5_MODE1	HB5_MODE0	read/write	0	0	1	0	0	1	1
	PWM_CH_FREQ_CTRL	PWM_CH1_FREQ_1	PWM_CH1_FREQ_0	read/write	0	1	1	0	0	1	1
	PWM1_DC_CTRL	PWM1_DC_CTRL_1	PWM1_DC_CTRL_0	read/write	1	1	1	0	0	1	1
	PWM2_DC_CTRL	PWM2_DC_CTRL_1	PWM2_DC_CTRL_0	read/write	0	0	0	1	0	1	1
	PWM3_DC_CTRL	PWM3_DC_CTRL_1	PWM3_DC_CTRL_0	read/write	1	0	0	1	0	1	1
	FW_OL_CTRL	reserved	reserved	read/write	0	1	0	1	0	1	1
Status Registers	**Status Registers**										
	SYS_DIAG_1:Global status 1	TPW	0	read/write	0	0	1	1	0	1	1
	SYS_DIAG_2:OP ERROR_1_STAT	HB1_HS_OC	HB1_LS_OC	read/write	1	0	1	1	0	1	1
	SYS_DIAG_3:OP ERROR_2_STAT	HB5_HS_OC	HB5_LS_OC	read/write	0	1	1	1	0	1	1
	SYS_DIAG_5:OP ERROR_4_STAT	HB1_HS_OL	HB1_LS_OL	read/write	0	0	0	0	1	1	1
	SYS_DIAG_6:OP ERROR_5_STAT	HB5_HS_OL	HB5_LS_OL	read/write	1	0	0	0	1	1	1

Figure 21. SA52106 Bit mapping

SPI Control Registers

- The 'POR' value is defined by the register content after a POR or device reset
- One 16-bit SPI command consists of two bytes
  - an address byte
  - followed by a data byte
- The control bits are not cleared or changed automatically by the device. This must be done by the microcontroller via SPI programming.
- Reading a register is done byte wise by setting the SPI bit 7 to "0" (=READ ONLY).
- Writing a register is done byte wise by setting the SPI bit 7 to "1".

Control Register Definition

HB_ACT_1_CTRL

Half-bridge output control 1(Address Byte [OP] 000 0011$_B$)

D7	D6	D5	D4	D3	D2	D1	D0
HB4_HS_EN	**HB4_LS_EN**	**HB3_HS_EN**	**HB3_LS_EN**	**HB2_HS_EN**	**HB2_LS_EN**	**HB1_HS_EN**	**HB1_LS_EN**
rw	rw	rw	rw	rw	rw	rw	rw

Field	Bits	Type	Description
HB4_HS_EN	D7	rw	Half-bridge output 4 high side switch enable 0_B HS4 OFF (default value) 1_B HS4 ON
HB4_LS_EN	D6	rw	Half-bridge output 4 low side switch enable 0_B LS4 OFF (default value) 1_B LS4 ON
HB3_HS_EN	D5	rw	Half-bridge output 3 high side switch enable 0_B HS3 OFF (default value) 1_B HS3 ON
HB3_LS_EN	D4	rw	Half-bridge output 3 low side switch enable 0_B LS3 OFF (default value) 1_B LS3 ON
HB2_HS_EN	D3	rw	Half-bridge output 2 high side switch enable 0_B HS2 OFF (default value) 1_B HS2 ON
HB2_LS_EN	D2	rw	Half-bridge output 2 low side switch enable 0_B LS2 OFF (default value) 1_B LS2 ON
HB1_HS_EN	D1	rw	Half-bridge output 1 high side switch enable 0_B HS1 OFF (default value) 1_B HS1 ON
HB1_LS_EN	D0	rw	Half-bridge output 1 low side switch enable 0_B LS1 OFF (default value) 1_B LS1 ON

Note: The simultaneous activation of both HS and LS switch within a half-bridge is prevented by the digital block to avoid cross current. If both LS_EN and HS_EN bits of a given half-bridge are set, the logic turns off this half-bridge.

HB_ACT_2_CTRL

Half-bridge output control 2(Address Byte [OP] 100 0011B)

D7	D6	D5	D4	D3	D2	D1	D0
reserved	**reserved**	**reserved**	**reserved**	**HB6_HS_EN**	**HB6_LS_EN**	**HB5_HS_EN**	**HB5_LS_EN**
rw	rw	rw	rw	rw	rw	rw	rw

Field	Bits	Type	Description
reserved	D7	rw	Reserved. Always reads as '0'
reserved	D6	rw	Reserved. Always reads as '0'
reserved	D5	rw	Reserved. Always reads as '0'
reserved	D4	rw	Reserved. Always reads as '0'
HB6_HS_EN	D3	rw	Half-bridge output 6 high side switch enable 0_B HS6 OFF (default value) 1_B HS6 ON
HB6_LS_EN	D2	rw	Half-bridge output 6 low side switch enable 0_B LS6 OFF (default value) 1_B LS6 ON
HB5_HS_EN	D1	rw	Half-bridge output 5 high side switch enable 0_B HS5 OFF (default value) 1_B HS5 ON
HB5_LS_EN	D0	rw	Half-bridge output 5 low side switch enable 0_B LS5 OFF (default value) 1_B LS5 ON

Note: The simultaneous activation of both HS and LS switch within a half-bridge is prevented by the digital block to avoid cross current. If both LS_EN and HS_EN bits of a given half-bridge are set, the logic turns off this half-bridge.

HB_MODE_1__CTRL

Half-bridge output mode control 1(Address Byte [OP] 110 0011B)

D7	D6	D5	D4	D3	D2	D1	D0
HB4_MODE1	**HB4_MODE0**	**HB3_MODE1**	**HB3_MODE0**	**HB2_MODE1**	**HB2_MODE0**	**HB1_MODE1**	**HB1_MODE0**
rw	rw	rw	rw	rw	rw	rw	rw

Field	Bits	Type	Description
HB4_MODEn (n=0,1)	D7:D6	rw	Half-bridge output 4 mode select 00_B No PWM (default value) 01_B PWM control with PWM Channel 1 10_B PWM control with PWM Channel 2 11_B PWM control with PWM Channel 3
HB3_MODEn (n=0,1)	D5:D4	rw	Half-bridge output 3 mode select 00_B No PWM (default value) 01_B PWM control with PWM Channel 1 10_B PWM control with PWM Channel 2 11_B PWM control with PWM Channel 3
HB2_MODEn (n=0,1)	D3:D2	rw	Half-bridge output 2 mode select 00_B No PWM (default value) 01_B PWM control with PWM Channel 1 10_B PWM control with PWM Channel 2 11_B PWM control with PWM Channel 3
HB1_MODEn (n=0,1)	D1:D0	rw	Half-bridge output 1 mode select 00_B No PWM (default value) 01_B PWM control with PWM Channel 1 10_B PWM control with PWM Channel 2 11_B PWM control with PWM Channel 3

HB_MODE_2_CTRL

Half-bridge output mode control 2(Address Byte [OP] 001 0011$_B$)

D7	D6	D5	D4	D3	D2	D1	D0
reserved	**reserved**	**reserved**	**reserved**	**HB6_MODE1**	**HB6_MODE0**	**HB5_MODE1**	**HB5_MODE0**
rw	rw	rw	rw	rw	rw	rw	rw

Field	Bits	Type	Description
reserved	D7:D6	rw	Reserved. Always reads as '0'
reserved	D5:D4	rw	Reserved. Always reads as '0'
HB6_MODEn (n=0,1)	D3:D2	rw	Half-bridge output 6 mode select 00_B No PWM (default value) 01_B PWM control with PWM Channel 1 10_B PWM control with PWM Channel 2 11_B PWM control with PWM Channel 3
HB5_MODEn (n=0,1)	D1:D0	rw	Half-bridge output 5 mode select 00_B No PWM (default value) 01_B PWM control with PWM Channel 1 10_B PWM control with PWM Channel 2 11_B PWM control with PWM Channel 3

PWM_CH_FREQ_CTRL

PWM channel frequency select (Address Byte [OP] 011 0011$_B$)

D7	D6	D5	D4	D3	D2	D1	D0
reserved	**reserved**	**PWM_CH3_ FREQ_1**	**PWM_CH3_ FREQ_0**	**PWM_CH2_ FREQ_1**	**PWM_CH2_ FREQ_0**	**PWM_CH1_ FREQ_1**	**PWM_CH1_ FREQ_0**
rw	rw	rw	rw	rw	rw	rw	rw

Field	Bits	Type	Description
reserved	D7:D6	**rw**	Bit reserved. Always reads '0'.
PWM_CH3_FREQ_n (n=0,1)	D5:D4	rw	PWM Channel 3 frequency select 00_B PWM is stopped and off (default value) 01_B PWM frequency 1: 80Hz 10_B PWM frequency 2: 100Hz 11_B PWM frequency 3: 200Hz
PWM_CH2_FREQ_n (n=0,1)	D3:D2	rw	PWM Channel 2 frequency select 00_B PWM is stopped and off (default value) 01_B PWM frequency 1: 80Hz 10_B PWM frequency 2: 100Hz 11_B PWM frequency 3: 200Hz
PWM_CH1_FREQ_n (n=0,1)	D1:D0	rw	PWM Channel 1 frequency select 00_B PWM is stopped and off (default value) 01_B PWM frequency 1: 80Hz 10_B PWM frequency 2: 100Hz 11_B PWM frequency 3: 200Hz

PWM1_DC_CTRL

PWM channel 1 duty cycle configuration (Address Byte [OP] 111 0011_B)

D7	D6	D5	D4	D3	D2	D1	D0
PWM1_DC_CTRL_7	**PWM1_DC_CTRL_6**	**PWM1_DC_CTRL_5**	**PWM1_DC_CTRL_4**	**PWM1_DC_CTRL_3**	**PWM1_DC_CTRL_2**	**PWM1_DC_CTRL_1**	**PWM1_DC_CTRL_0**
rw	rw	rw	rw	rw	rw	rw	rw

Field	Bits	Type	Description
PWM1_DC_CTRLn	D7:D0	rw	PWM Channel 1 Duty Cycle configuration (bit7=MSB) 0000 0000_B 100%OFF (default value) xxxx $xxxx_B$ parts of 255 ON 1111 1111_B 100% ON

PWM2_DC_CTRL

PWM channel 2 duty cycle configuration (Address Byte [OP] 000 1011_B)

D7	D6	D5	D4	D3	D2	D1	D0
PWM2_DC_CTRL_7	**PWM2_DC_CTRL_6**	**PWM2_DC_CTRL_5**	**PWM2_DC_CTRL_4**	**PWM2_DC_CTRL_3**	**PWM2_DC_CTRL_2**	**PWM2_DC_CTRL_1**	**PWM2_DC_CTRL_0**
rw	rw	rw	rw	rw	rw	rw	rw

Field	Bits	Type	Description
PWM2_DC_CTRLn	D7:D0	rw	PWM Channel 2 Duty Cycle configuration (bit7=MSB) 0000 0000_B 100%OFF (default value) xxxx $xxxx_B$ parts of 255 ON 1111 1111_B 100% ON

PWM3_DC_CTRL

PWM channel 3 duty cycle configuration (Address Byte [OP] 100 1011_B)

D7	D6	D5	D4	D3	D2	D1	D0
PWM3_DC_CTRL_7	**PWM3_DC_CTRL_6**	**PWM3_DC_CTRL_5**	**PWM3_DC_CTRL_4**	**PWM3_DC_CTRL_3**	**PWM3_DC_CTRL_2**	**PWM3_DC_CTRL_1**	**PWM3_DC_CTRL_0**
rw	rw	rw	rw	rw	rw	rw	rw

Field	Bits	Type	Description
PWM3_DC_CTRLn	D7:D0	rw	PWM Channel 3 Duty Cycle configuration (bit7=MSB) 0000 0000_B 100%OFF (default value) xxxx $xxxx_B$ parts of 255 ON 1111 1111_B 100% ON

FW_OL_CTRL

Free-wheeling configuration (Address Byte [OP] 010 1011$_B$)

D7	D6	D5	D4	D3	D2	D1	D0
FW_HB6	**FW_HB5**	**FW_HB4**	**FW_HB3**	**FW_HB2**	**FW_HB1**	**reserved**	**reserved**
rw	rw	rw	rw	rw	rw	rw	rw

Field	Bits	Type	Description
FW_HB6	D7	rw	HB6 free-wheeling configuration 0_B Passive free-wheeling(default value) 1_B Active free-wheeling
FW_HB5	D6	rw	HB5 free-wheeling configuration 0_B Passive free-wheeling(default value) 1_B Active free-wheeling
FW_HB4	D5	rw	HB4 free-wheeling configuration 0_B Passive free-wheeling(default value) 1_B Active free-wheeling
FW_HB3	D4	rw	HB3 free-wheeling configuration 0_B Passive free-wheeling(default value) 1_B Active free-wheeling
FW_HB2	D3	rw	HB2 free-wheeling configuration 0_B Passive free-wheeling(default value) 1_B Active free-wheeling
FW_HB1	D2	rw	HB1 free-wheeling configuration 0_B Passive free-wheeling(default value) 1_B Active free-wheeling
reserved	D1	rw	Bit reserved. Always reads ‘0’.
reserved	D0	rw	Bit reserved. Always reads ‘0’.

SPI Status Registers

The status register has a READ/CLEAR access

- The ‘POR’ value of the status registers (content after a POR or device reset) is 0000 0000$_B$
- One 16-bit SPI command consists of two bytes
  - an address byte
  - followed by a data byte
- Reading a register is done byte wise by setting the SPI bit 7 of the address byte to “0” (=READ ONLY).
- Clearing a register is done byte wise by setting the SPI bit 7 of the address byte to “1”.
- SPI status registers are not cleared automatically by the device. This must be done by the microcontroller via SPI command.

Status Register Definition

SYS_DIAG_1
Global status 1 (Address Byte [OP] 001 1011$_B$)

D7	D6	D5	D4	D3	D2	D1	D0
SPI_ERR	**LE**	**VS_UV**	**VS_OV**	**NPOR**	**TSD**	**TPW**	**reserved**
rc	r	rc	rc	rc	rc	rc	r

Field	Bits	Type	Description
SPI_ERR	D7	rc	SPI error detection 0_B No SPI protocol error is detected (default value) 1_B An SPI protocol error is detected
LE	D6	r	Load error detection (logic OR combination of Open Load and Overcurrent) 0_B No Open Load and no Overcurrent detected (default value) 1_B Open load or Overcurrent detected in at least one of the power outputs. Error latched
VS_UV	D5	rc	VS Undervoltage error detection 0_B No undervoltage on VS detected (default value) 1_B Undervoltage on VS detected. Error latched and all outputs disabled
VS_OV	D4	rc	VS Overvoltage error detection 0_B No overvoltage on VS detected (default value) 1_B Overvoltage on VS detected. Error latched and all outputs disabled
NPOR	D3	rc	Not Power On Reset(NPOR) detection 0_B POR on EN or VDD supply rail (default value) 1_B No POR
TSD	D2	rc	Temperature shutdown error detection 0_B Junction temperature below temperature shutdown threshold (default value) 1_B Junction temperature has reached temperature shutdown threshold. Error latched and all outputs disabled.
TPW	D1	rc	Temperature pre-warning error detection 0_B Junction temperature below temperature pre-warning threshold (default value) 1_B Junction temperature has reached temperature pre-warning threshold.
reserved	D0	r	Bit reserved. Always reads ‘0’.

Note: The LE bit in the Global Status register is read only. It reflects an OR combination of the respective open load and overcurrent errors of the half bridge channels. If all OC/OL bits of the respective high-side and low-side channels are cleared to '0', the LE bit will be automatically updated to '0'.

SYS_DIAG_2:OP_ERROR_1_STAT

Overcurrent error status of half-bridge outputs 1-4 (Address Byte [OP] 101 1011$_B$)

D7	D6	D5	D4	D3	D2	D1	D0
HB4_HS_OC	**HB4_LS_OC**	**HB3_HS_OC**	**HB3_LS_OC**	**HB2_HS_OC**	**HB2_LS_OC**	**HB1_HS_OC**	**HB1_LS_OC**
rc	rc	rc	rc	rc	rc	rc	rc

Field	Bits	Type	Description
HB4_HS_OC	D7	rc	High-side(HS) switch of half-bridge 4 overcurrent detection 0_B No error on HS4 switch (default value) 1_B Overcurrent detected on HS4 switch. Error latched and HS4 disabled.
HB4_LS_OC	D6	rc	Low-side(LS) switch of half-bridge 4 overcurrent detection 0_B No error on LS4 switch (default value) 1_B Overcurrent detected on LS4 switch. Error latched and LS4 disabled.
HB3_HS_OC	D5	rc	High-side(HS) switch of half-bridge 3 overcurrent detection 0_B No error on HS3 switch (default value) 1_B Overcurrent detected on HS3 switch. Error latched and HS3 disabled.
HB3_LS_OC	D4	rc	Low-side(LS) switch of half-bridge 3 overcurrent detection 0_B No error on LS3 switch (default value) 1_B Overcurrent detected on LS3 switch. Error latched and LS3 disabled.
HB2_HS_OC	D3	rc	High-side(HS) switch of half-bridge 2 overcurrent detection 0_B No error on HS2 switch (default value) 1_B Overcurrent detected on HS2 switch. Error latched and HS2 disabled.
HB2_LS_OC	D2	rc	Low-side(LS) switch of half-bridge 2 overcurrent detection 0_B No error on LS2 switch (default value) 1_B Overcurrent detected on LS2 switch. Error latched and LS2 disabled.
HB1_HS_OC	D1	rc	High-side(HS) switch of half-bridge 1overcurrent detection 0_B No error on HS1 switch (default value) 1_B Overcurrent detected on HS1 switch. Error latched and HS1 disabled.
HB1_LS_OC	D0	rc	Low-side(LS) switch of half-bridge 1 overcurrent detection 0_B No error on LS1 switch (default value) 1_B Overcurrent detected on LS1 switch. Error latched and LS1 disabled.

SYS_DIAG_3:OP_ERROR_2_STAT

Overcurrent error status of half-bridge outputs 5-6 (Address Byte [OP] 011 1011$_B$)

D7	D6	D5	D4	D3	D2	D1	D0
reserved	**reserved**	**reserved**	**reserved**	**HB6_HS_OC**	**HB6_LS_OC**	**HB5_HS_OC**	**HB5_LS_OC**
r	r	r	r	rc	rc	rc	rc

Field	Bits	Type	Description
reserved	D7	r	Bit reserved. Always reads ‘1’.
reserved	D6	r	Bit reserved. Always reads ‘0’.
reserved	D5	r	Bit reserved. Always reads ‘0’.
reserved	D4	r	Bit reserved. Always reads ‘0’.
HB6_HS_OC	D3	rc	High-side(HS) switch of half-bridge 6 overcurrent detection 0_B No error on HS6 switch (default value) 1_B Overcurrent detected on HS6 switch. Error latched and HS6 disabled.
HB6_LS_OC	D2	rc	Low-side(LS) switch of half-bridge 6 overcurrent detection 0_B No error on LS6 switch (default value) 1_B Overcurrent detected on LS6 switch. Error latched and LS6 disabled.
HB5_HS_OC	D1	rc	High-side(HS) switch of half-bridge 5 overcurrent detection 0_B No error on HS5 switch (default value) 1_B Overcurrent detected on HS5 switch. Error latched and HS5 disabled.
HB5_LS_OC	D0	rc	Low-side(LS) switch of half-bridge 5 overcurrent detection 0_B No error on LS5 switch (default value) 1_B Overcurrent detected on LS5 switch. Error latched and LS5 disabled.

SYS_DIAG_5:OP_ERROR_4_STAT

Open load error status of half-bridge outputs 1-4 (Address Byte [OP] 000 0111$_B$)

D7	D6	D5	D4	D3	D2	D1	D0
HB4_HS_OL	**HB4_LS_OL**	**HB3_HS_OL**	**HB3_LS_OL**	**HB2_HS_OL**	**HB2_LS_OL**	**HB1_HS_OL**	**HB1_LS_OL**
rc	rc	rc	rc	rc	rc	rc	rc

Field	Bits	Type	Description
HB4_HS_OL	D7	rc	High-side(HS) switch of half-bridge 4 open load detection 0_B No error on HS4 switch (default value) 1_B Open load detected on HS4 switch. Error latched.
HB4_LS_OL	D6	rc	Low-side(LS) switch of half-bridge 4 open load detection 0_B No error on LS4 switch (default value) 1_B Open load detected on LS4 switch. Error latched.
HB3_HS_OL	D5	rc	High-side(HS) switch of half-bridge 3 open load detection 0_B No error on HS3 switch (default value) 1_B Open load detected on HS3 switch. Error latched.
HB3_LS_OL	D4	rc	Low-side(LS) switch of half-bridge 3 open load detection 0_B No error on LS3 switch (default value) 1_B Open load detected on LS3 switch. Error latched.
HB2_HS_OL	D3	rc	High-side(HS) switch of half-bridge 2 open load detection 0_B No error on HS2 switch (default value) 1_B Open load detected on HS2 switch. Error latched.
HB2_LS_OL	D2	rc	Low-side(LS) switch of half-bridge 2 open load detection 0_B No error on LS2 switch (default value) 1_B Open load detected on LS2 switch. Error latched.
HB1_HS_OL	D1	rc	High-side(HS) switch of half-bridge 1 open load detection 0_B No error on HS1 switch (default value) 1_B Open load detected on HS1 switch. Error latched.
HB1_LS_OL	D0	rc	Low-side(LS) switch of half-bridge 1 open load detection 0_B No error on LS1 switch (default value) 1_B Open load detected on LS1 switch. Error latched.

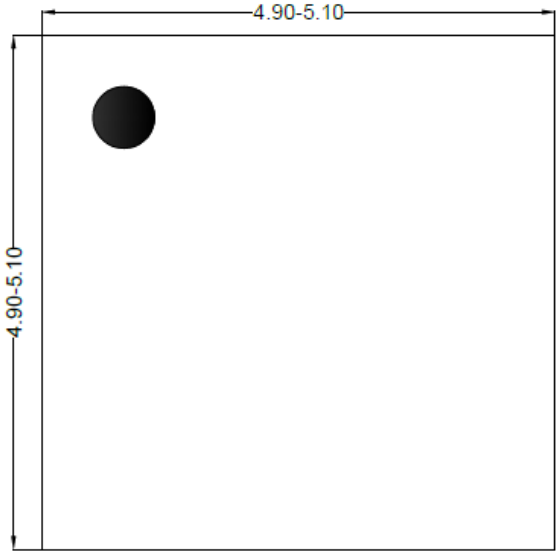
SYS_DIAG_6:OP_ERROR_5_STAT

Open load error status of half-bridge outputs 5-6 (Address Byte [OP] 100 0111$_B$)

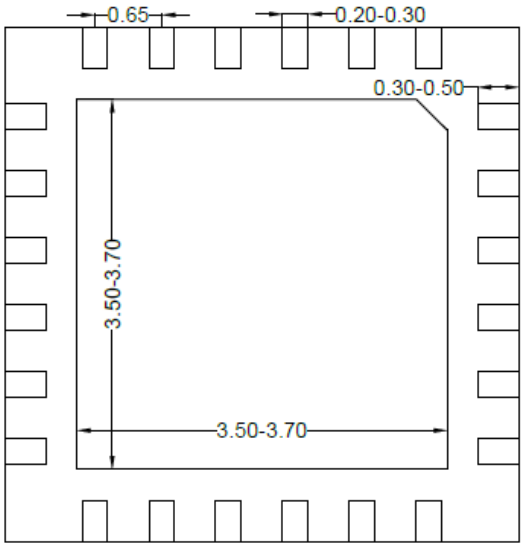
D7	D6	D5	D4	D3	D2	D1	D0
reserved	**reserved**	**reserved**	**reserved**	**HB6_HS_OL**	**HB6_LS_OL**	**HB5_HS_OL**	**HB5_LS_OL**
r	r	r	r	rc	rc	rc	rc

Field	Bits	Type	Description
reserved	D7	r	Bit reserved. Always reads ‘0’.
reserved	D6	r	Bit reserved. Always reads ‘0’.
reserved	D5	r	Bit reserved. Always reads ‘0’.
reserved	D4	r	Bit reserved. Always reads ‘0’.
HB6_HS_OL	D3	rc	High-side(HS) switch of half-bridge 6 open load detection 0_B No error on HS6 switch (default value) 1_B Open load detected on HS6 switch. Error latched.
HB6_LS_OL	D2	rc	Low-side(LS) switch of half-bridge 6 open load detection 0_B No error on LS6 switch (default value) 1_B Open load detected on LS6 switch. Error latched.
HB5_HS_OL	D1	rc	High-side(HS) switch of half-bridge 5 open load detection 0_B No error on HS5 switch (default value) 1_B Open load detected on HS5 switch. Error latched.
HB5_LS_OL	D0	rc	Low-side(LS) switch of half-bridge 5 open load detection 0_B No error on LS5 switch (default value) 1_B Open load detected on LS5 switch. Error latched.

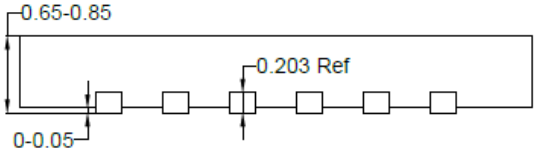
QFN5x5-24 Package Outline Drawing



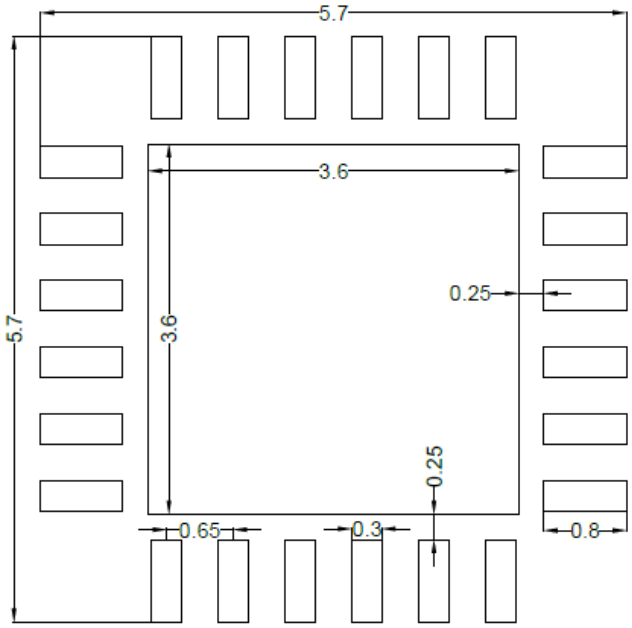
Top View



Bottom View



Front View



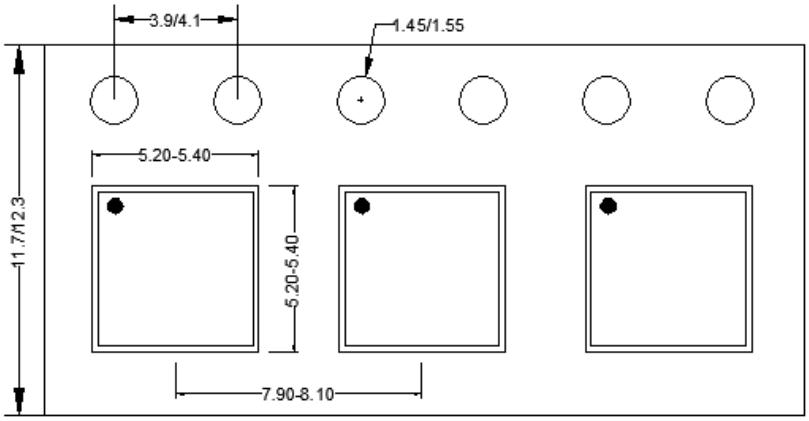
Recommended PCB layout
(Reference only)

Notes: 1, All dimension in millimeter and exclude mold flash & metal burr

Taping & Reel Specification

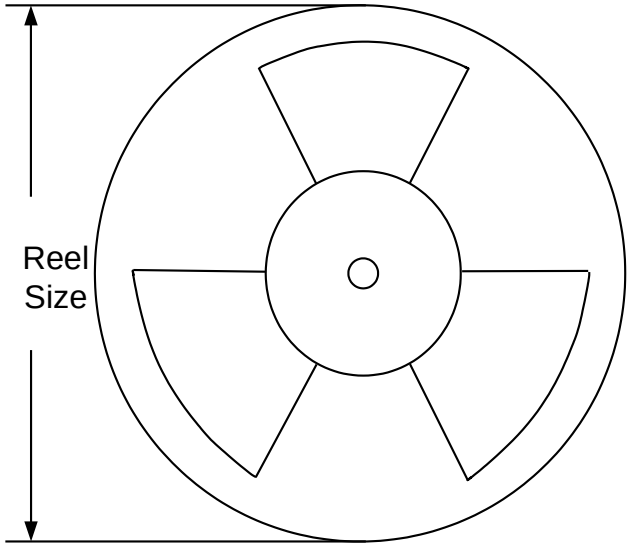
1. Taping orientation

QFN5×5



Feeding direction

2. Carrier Tape & Reel specification for packages



Package types	Tape width (mm)	Pocket pitch(mm)	Reel size (Inch)	Trailer length(mm)	Leader length (mm)	Qty per reel
QFN5×5	12	8	13"	400	400	5000

3. Others: NA

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