SA52631

40V High-side and Low-Side Gate Driver

General Description

SA52631 is a high voltage floating driver for direct driving high side and low side channels. The floating channel can be used to drive 40V N-channel MOSFET in high side configuration. Input logic is compatible with standard CMOS or TTL. Compact DFN3X3-8 package is utilized to minimize the peripheral circuit design and the difficulty of PCB mounting.

Features

- High Voltage Range up to 40 V
- 0.75A Source and 1.25A Sink Current
- VCC Operation Range from 4.4V to 14V
- CMOS/TTL Compatible
- Fast Propagation Delay Time
- DFN3x3-8 Package
- AEC-Q100 Qualified

Ordering Information

SA52631 □(□□□)

Package Code

Optional Spec Code

Ordering Number	Package type	Note
SA52631DAD	DFN3x3-8	

Applications

- Wireless Charger
- Half-bridge Gate Driver

Typical Application

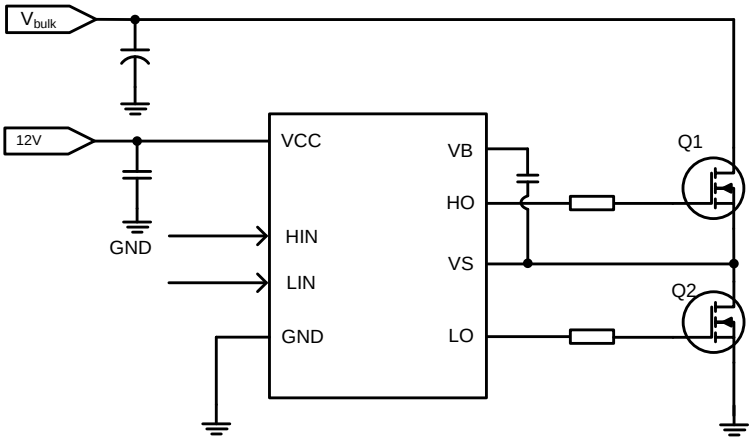
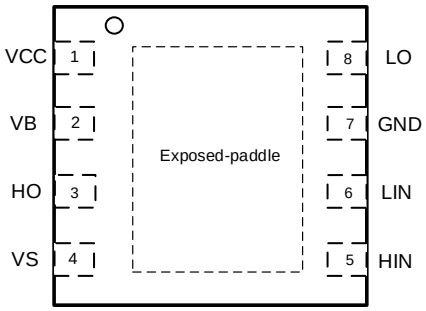


Figure 1. SA52631 Application Schematic

Pinout (Top View)



(DFN3x3-8)

Top Mark: DQN*xyz* (device code: **DQN**, ***x=year code, y=week code, z= lot number code)***

Pin Name	Pin No.	Pin Description
VCC	1	Logic power supply pin. Decouple with MLCC to ground for high frequency noise elimination.
VB	2	High-side bias voltage supply pin.
HO	3	High-side driver output pin.
VS	4	High-side bias voltage floating ground.
HIN	5	High-side control signal input pin.
LIN	6	Low-side control signal input pin.
GND	7	Logic ground.
LO	8	Low-side driver output pin.

Function Block

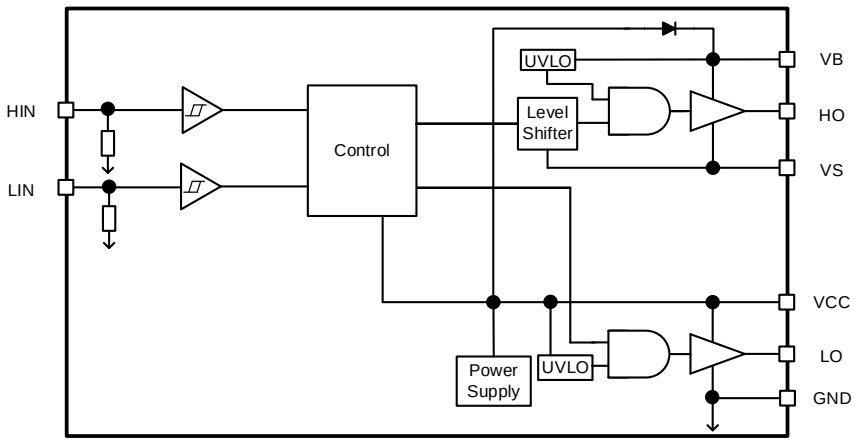


Figure 2. Block Diagram

Absolute Maximum Ratings (Note 1)

V_{CC} ---------- -0.3 - 20V
V_{VB} ---------- -0.3 - 44V
V_{VS} ---------- -1V - V_{VB} +0.3V
V_{HIN}, V_{LIN} ---------- -0.3 - 20V
V_{HO} ---------- V_{VS}-0.3V - V_{VB}+0.3V
V_{LO} ---------- -0.3V - VCC+0.3V
Power Dissipation, P_D @ T_A = 25°C, ---------- 0.21 W
Package Thermal Resistance (Note 2)
θ_{JA} ---------- 35 °C/W
θ_{JC} ---------- 33 °C/W
Junction Temperature Range ---------- -40°C to 150°C
Storage Temperature Range ---------- -65°C to 150°C

Recommended Operating Conditions

V_{CC} ---------- 4.4V to 14V
V_{VB} ---------- V_{VS}+4.4V to V_{VS}+14V
V_{VS} (Note 3) ---------- -1V to 40V
V_{HIN}, V_{LIN} ---------- 0V to 5V
dV_S/dt ---------- less than 50V/ns
Operation Junction Temperature Range ---------- -40°C to 125°C

Electrical Characteristics

T_A=T_J=-40°C to 125°C, V_{CC}=V_{VB}=12V, no load on LO and HO, unless otherwise specified.

Parameter	Symbol	Test conditions	Min.	Typ.	Max.	Units
Supply Current						
Quiescent V_{CC} Supply Current	I_{QVCC}	V_{HIN}=V_{LIN}=0V		70	110	uA
Operation V_{CC} Supply Current	I_{OPVCC}	f=200kHz, C_{LOAD}=1000pF		3		mA
Quiescent V_{BS} Supply Current (Note 4)	I_{QVBS}	V_{HIN}=V_{LIN}=0V		65	100	uA
Operation V_{BS} Supply Current	I_{OPVBS}	f =200kHz, C_{LOAD}=1000pF		3		mA
Input Signal						
Logic “1” Input Voltage	V_{IH}		2.4			V
Logic “0” Input Voltage	V_{IL}				0.8	V
Input Hysteresis	V_{IHYS}			680		mV
Logic “1” Input Bias Current	I_{IH}	V_{IN}=5V			50	uA
Logic “0” Input Bias Current	I_{IL}	V_{IN}=0V			5	uA
Under Voltage Lock Out						
V_{CC} under Voltage Rising Threshold	V_{CCUV+}		3.6	4	4.4	V
V_{CC} under Voltage Falling Threshold	V_{CCUV-}		3.1	3.5	3.9	V
V_{BS} under Voltage Rising Threshold	V_{BSUV+}		3.6	4	4.4	V
V_{BS} under Voltage Falling Threshold	V_{BSUV-}		3.1	3.5	3.9	V
Boot Strap Diode						
Low Current forward Voltage	V_{F1}	I_{VCC-VB}=100uA		0.65		V
High Current forward Voltage	V_{F2}	I_{VCC-VB}=100mA		0.9		V
Gate Driver						
High-side High Level Output Voltage	V_{HOH}	I_O= -100mA, V_{HOH} = V_{VB}-V_{HO}		0.71		V
High-side Low Level Output Voltage	V_{HOL}	I_O=100mA		0.21		V
Low-side High Level Output Voltage	V_{LOH}	I_O= -100mA, V_{LOH} = V_{CC}-V_{LO}		0.71		V
Low-side Low Level Output Voltage	V_{LOL}	I_O=100mA		0.21		V
Gate Driver Output						
Peak Pull-up Current	I_{O-}	V_O=0V, (Note 5)		0.75		A
Peak Pull-down Current	I_{O+}	V_O=12V, (Note 5)		1.25		A

Note 1: Stresses listed as the above “Absolute Maximum Ratings” may cause permanent damage to the device. These are for stress ratings. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may remain possibility to affect device reliability.

Note 2: θ_{JA} is measured in the natural convection at T_A = 25°C on a high effective 4-layer thermal conductivity test board with four thermals via.

Note 3: Make sure V_{VB} does not exceed ABS 44V.

Note 4: V_{BS}=V_{VB}-V_{VS}

Note 5: This spec is guaranteed by design.

Propagation Delays

V_{CC}=V_{BS}=12V, VS=GND=0V, C_L=1000pF, T_A=25℃, unless otherwise specified.

Parameter	Symbol	Test conditions	Min.	Typ.	Max.	Units
Turn on Propagation Delay	T_{DLTON}			32		ns
Turn off Propagation Delay	T_{DLTOFF}			27		ns

Delay Matching

V_{CC}=V_{BS}=12V, VS=GND=0V, C_L=1000pF, T_A=25℃, unless otherwise specified.

Parameter	Symbol	Test conditions	Min.	Typ.	Max.	Units
Delay Matching, HO&LO Turn-on	T_{MON}				10	ns
Delay Matching, HO&LO Turn-off	T_{MOFF}				10	ns

Output Rising and Falling Time

V_{CC}=V_{BS}=12V, VS=GND=0V, T_A=25℃, unless otherwise specified.

Parameter	Symbol	Test conditions	Min.	Typ.	Max.	Units
Turn on Rise Time	t_R	C_{LOAD} = 1000pF, from 10% to 90%		20		ns
Turn off Fall Time	t_F			10		ns

Switching Timing

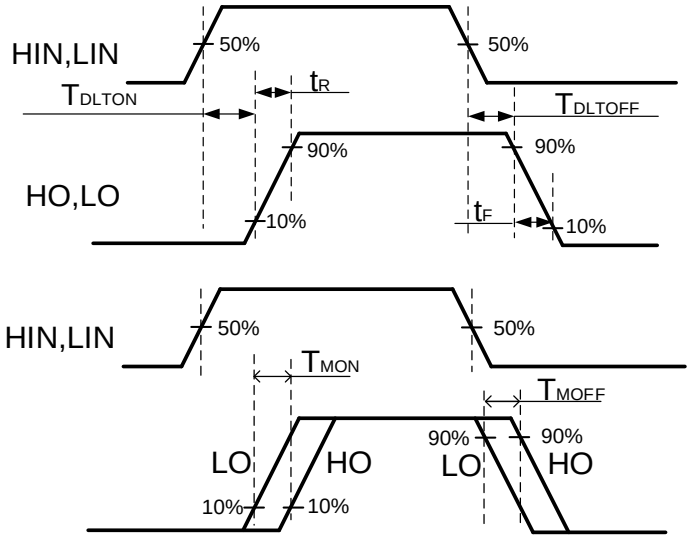
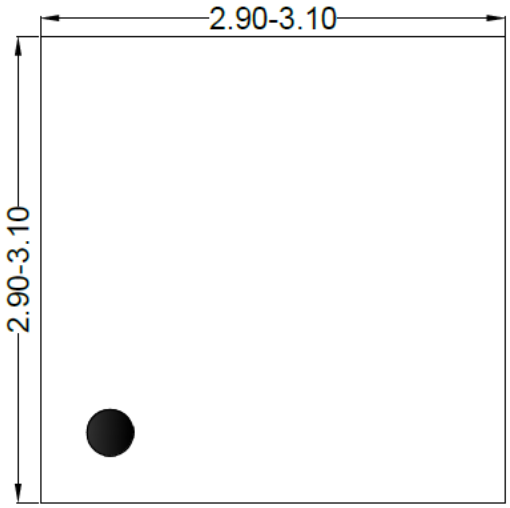
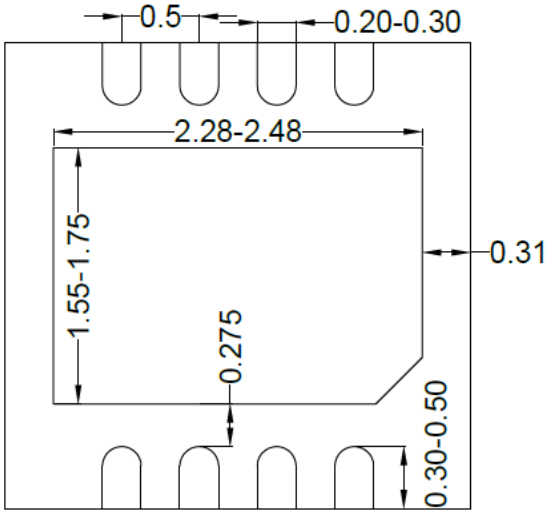


Figure 3. Timing Diagram

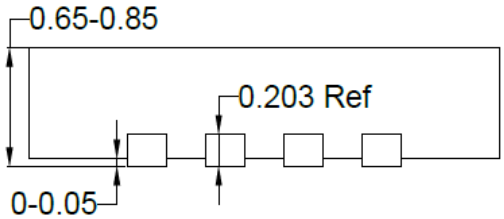
DFN3×3-8 Package Outline Drawing



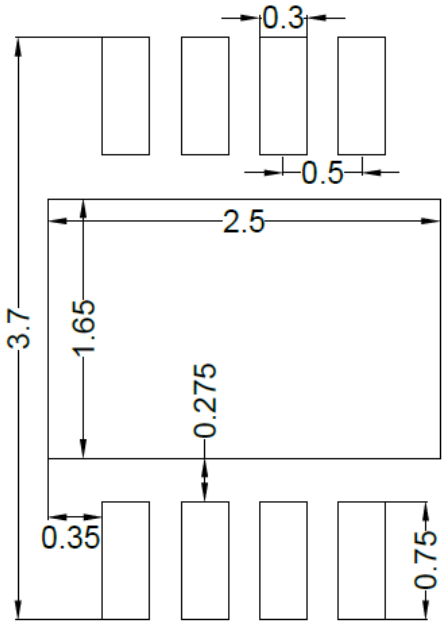
Top view



Bottom view



Front view

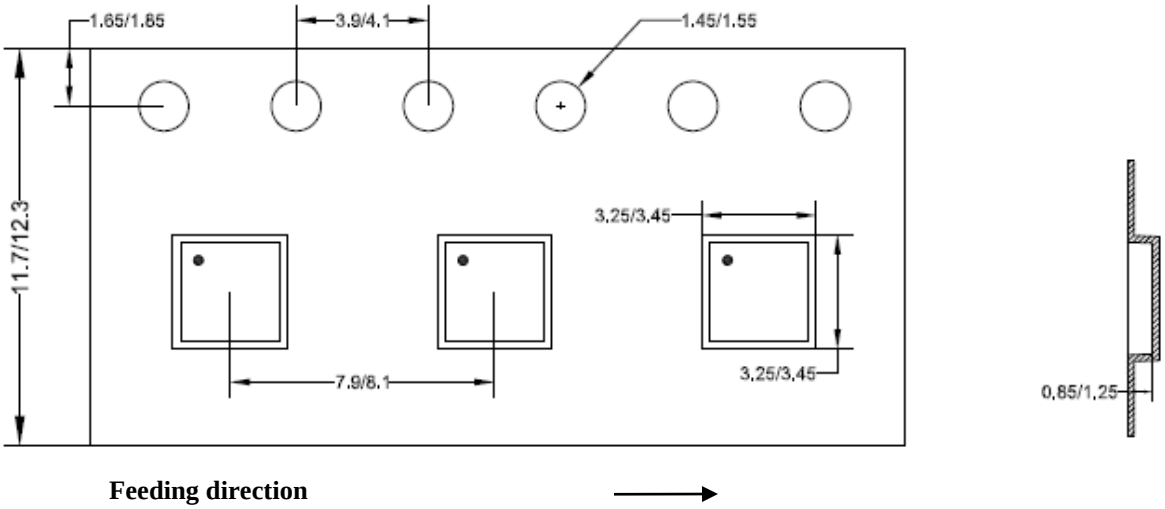


Recommended PCB layout
(Reference only)

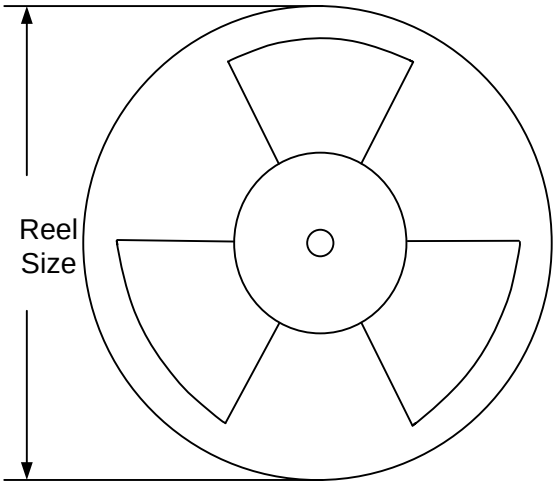
Notes: **All dimensions in millimeter and exclude mold flash & metal burr.**

Taping & Reel Specification

1. DFN3x3 taping orientation



2. Carrier Tape & Reel specification for packages



Package type	Tape width (mm)	Pocket pitch(mm)	Reel size (Inch)	Trailer length(mm)	Leader length (mm)	Qty per reel (pcs)
DFN3x3	12	8	13"	400	400	5000

3. Others: NA