SYT21S05DXD

Ultra-Low Capacitance TVS Protection

General Description

The SYT21S05DXD is an ultra-low capacitance bi-directional transient voltage suppressor (TVS) designed to provide electrostatic discharge (ESD) protection for high-speed data interfaces.

With a typical capacitance of 0.5pF, the device is designed to protect parasitic-sensitive systems against overvoltage and overcurrent transient events. It complies with IEC61000-4-2 (ESD) (±30kV air, ±30kV contact discharge), and IEC61000-4-5 (surge) (4.5A, 8/20μs) standards.

Each SYT21S05DXD device can protect one data line. It is available in a compact DFN0.6×0.3-2 package.

Features

- Operating Voltage: 5V and Below
- Transient Protection for High-Speed Data Lines
  - IEC61000-4-2 (ESD) ±30kV (Air) ±30kV (Contact)
  - IEC61000-4-5 (Surge) 4.5 (8/20μs)
- Protects One Data, Control or Power Line
- Low Capacitance: 0.5pF (Typical)
- Low Leakage Current: 0.01μA at V_{RWM} (Typical)
- Low Clamping Voltage

Applications

- Serial ATA
- PCI Express
- Desktops, Servers, and Notebooks
- MDDI Ports
- USB2.0, 3.0 and 3.1
- Display Ports
- HDMI 1.3, 1.4, 2.0 and 2.1
- Digital Visual Interfaces (DVI)

Mechanical Characteristics

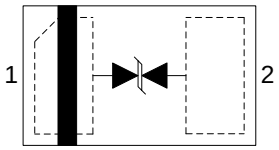
- DFN0.6×0.3-2 Package
- Marking: Device Code, Date Code
- Packaging: Tape and Reel

Circuit Diagram

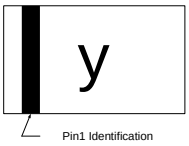
Ordering Information

Part Number	Package Type	Top Mark
SYT21S05DXD	DFN0.6×0.3-2	y

Pinout (Top View)



Marking Codes



Notes: "y" is device code, fixed.

Pin Descriptions

Device Pins	Name	Description
1	Input/Output	IO
2	Input/Output	IO

Absolute Maximum Ratings (Note 1)				
Parameter	**Symbol**	**Min**	**Max**	**Unit**
ESD per IEC 61000-4-2 (Air) ESD per IEC 61000-4-2 (Contact)	V_{ESD}	-30 -30	30 30	kV
Maximum Peak Pulse Current (8/20μs)	I_{PP}		4.5	A
Junction Temperature	T_J	-40	+125	°C
Storage Temperature	T_{STG}	-55	+150	°C

Electrical Characteristics (IO referenced to IO, T_A = 25°C, Note 4)						
Parameter	**Symbol**	**Test Condition**	**Min**	**Typ**	**Max**	**Unit**
Nominal Reverse Working Voltage	V_{RWM}				5.0	V
Reverse Leakage Current at V_{RWM}	I_R	V_{RWM} = 5V, T_A = 25°C		0.01	0.1	μA
Reverse Triggering Voltage at I_{t1} (Note 5)	V_{tl}	I_{tl}=1μA	5.5		10	V
Holding Voltage at I_h	V_h	I_h =10mA	5.5		9.0	V
Clamping Voltage at I_{PP} (Note 5)	V_C	I_{PP} = 16A, t_p = 10/100ns		11		V
Clamping Voltage at I_{PP} (Note 5)	V_C	I_{PP} = 4.5A, t_p = 8/20μs		10	12	V
Dynamic Resistance (Note 2, 5)	R_{DYN}	t_p = 10/100ns		0.25		Ω
Parasitic Capacitance (Note 5)	C_{ESD}	V_R = 2.5V, f = 1MHz		0.50	0.65	pF

Note 1: Stresses beyond the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: R_{DYN} calculated based on I_{PP}=8A to I_{PP}=16A, t_p = 10/100ns.

Note 3: The device is not guaranteed to function outside its operating conditions.

Note 4: Unless otherwise stated, limits are 100% production tested under pulsed load conditions such that $T_A \cong T_J$ = 25°C. Limits over the operating temperature range (see recommended operating conditions) and relevant voltage range(s) are guaranteed by design, test, or statistical correlation.

Note 5: Guaranteed by design or statistical correlation and not production tested.

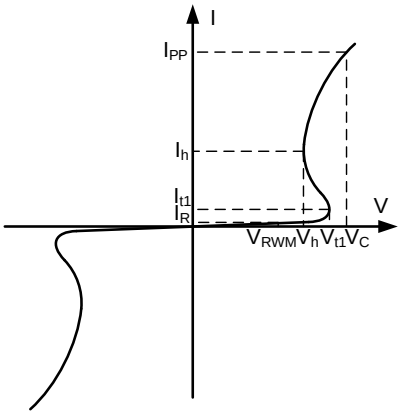
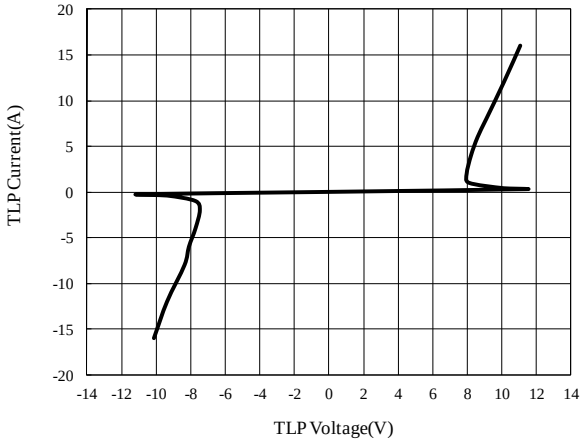


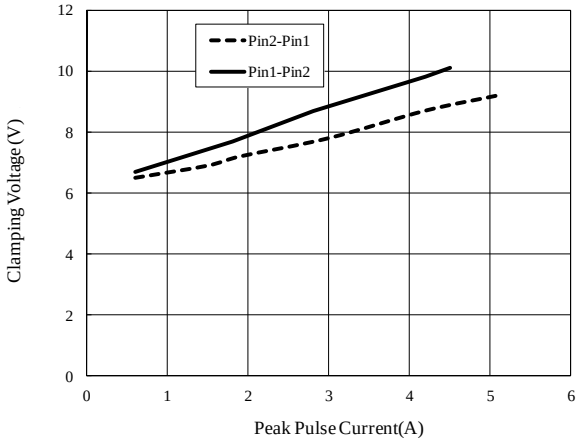
Figure 1. Bi-Directional TVS

Typical Performance Characteristics, IO referenced to IO

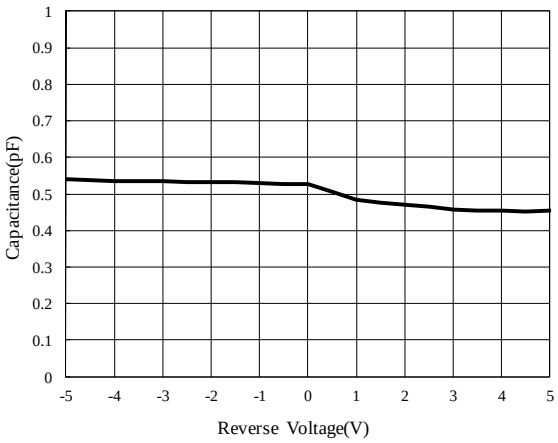
TLP Testing



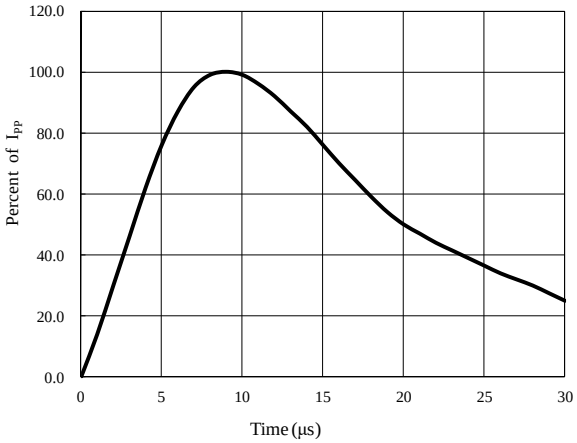
Clamping Voltage vs. Peak Pulse Current (8/20μs)



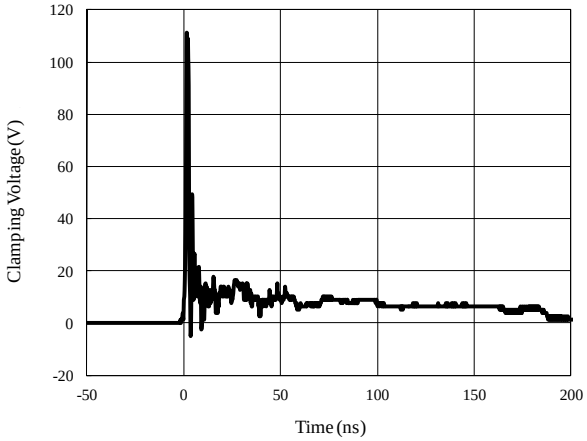
Capacitance vs. Voltage



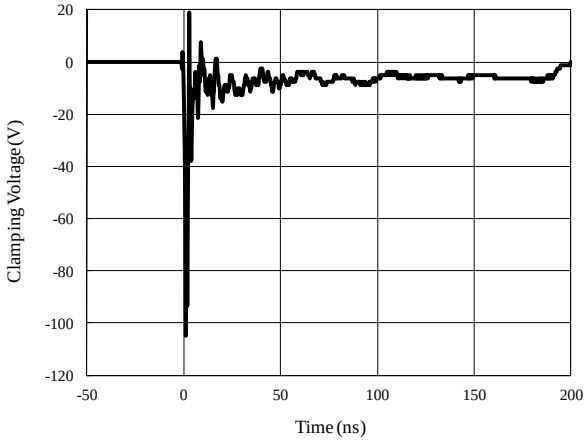
Pulse Waveform



ESD Clamping
(+8kV Contact per IEC 61000-4-2)



ESD Clamping
(-8kV Contact per IEC 61000-4-2)



Application Information

PCB Pin Connections

The SYT21S05DXD protects one bi-directional data line against overvoltage and overcurrent transient events by clamping it to an acceptable reference.

The SYT21S05DXD pin connections are shown in Figure 1. The protected line is connected to one of the pins, while the other is connected to the GND, which should connect to a ground plane on the board. All path lengths connected to pins of the SYT21S05DXD should be as short as possible to minimize the parasitic inductance.

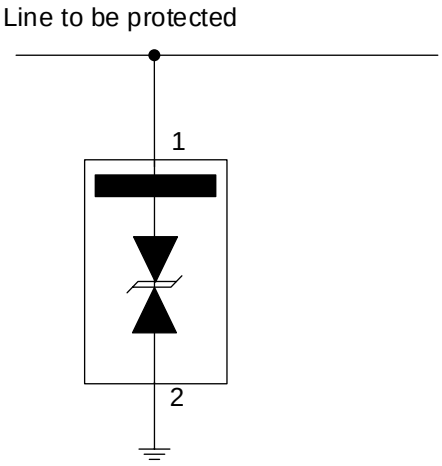


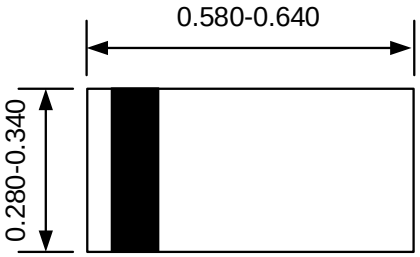
Figure 2. ESD/Surge Protection

PCB Layout Guidelines

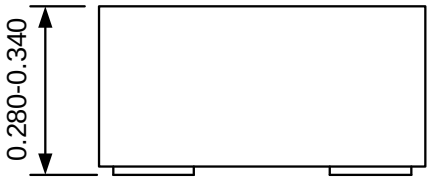
For optimum ESD protection and circuit performance, the following PCB layout guidelines are recommended:

- Place SYT21S05DXD as close to the connector or terminal ports as possible.
- Use a large via to connect the SYT21S05DXD pin to the ground.
- Avoid running signals near board edges.
- The SYT21S05DXD should be placed near the protected line.
- The distance between the SYT21S05DXD ground pin and the GND reference path should be as short as possible.

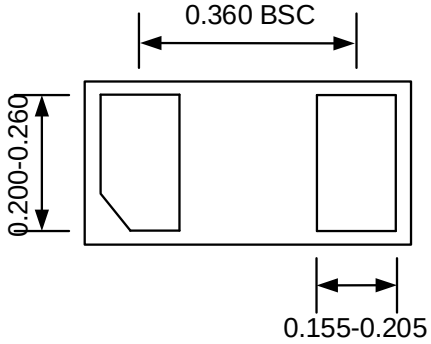
DFN0.6×0.3-2 Package Outline



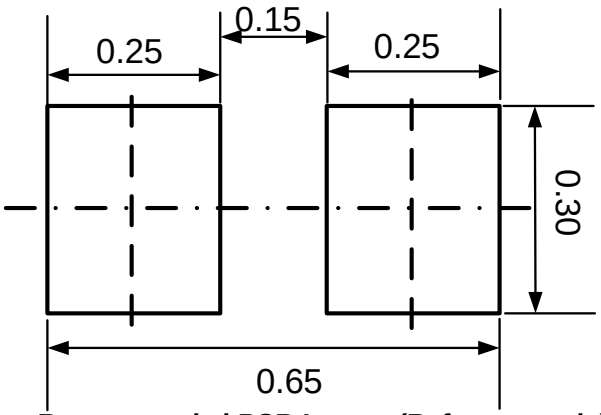
Top View



Side View



Bottom View

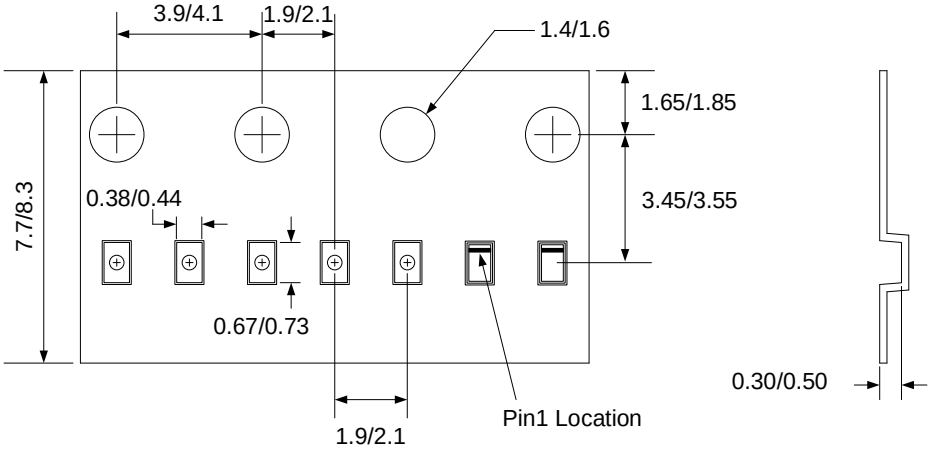


Recommended PCB Layout (Reference only)

Note: All dimensions are in millimeters and exclude mold flash and metal burr.

Tape and Reel Information

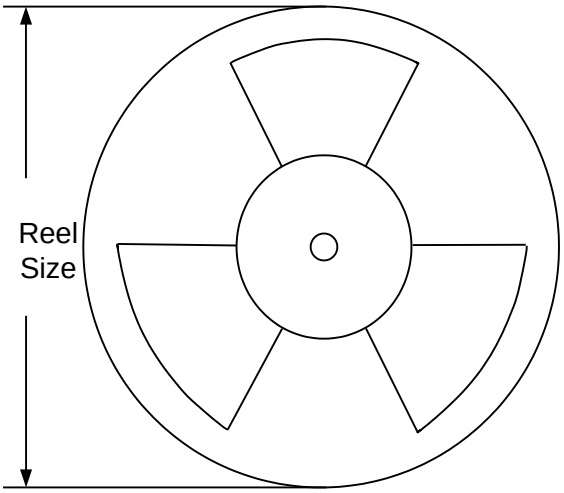
Tape Dimensions and Pin 1 Orientation



Dimensions In mm

Feeding direction ⟶

Reel Dimensions



Package Type	Tape Width (mm)	Pocket Pitch(mm)	Reel Size (Inch)	Qty per Reel (pcs)
DFN0.6×0.3-2	8	2	7"	10000

Revision History

The revision history provided is for informational purposes only and is believed to be accurate; however, not warrantied. Please make sure that you have the latest revision.

Revision Number	Revision Date	Description	Pages changed
1.0	Aug.05, 2024	Initial Release	

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