SQ33020

High Frequency QR Flyback Controller with Valley Lockout, Accuracy Output OCP, and X Capacitor Discharge

General Description

The SQ33020 is a high frequency quasi-resonant (QR) flyback controller designed for power delivery (PD) adaptors and quick battery chargers. It can deliver 240W output power with 25kHz–500kHz switching frequency.

The SQ33020 operates using peak current control. It provides a QR mode in which the MOSFET can be turned on at a valley point to reduce switching loss, especially under high input voltages.

In conventional QR flyback solutions, the valley number always varies between 1 and 2 or between 3 and 5, which increases V_O ripple and creates audible noise. The SQ33020 uses a proprietary circuit to lock the valley number between 1 and 6, which provides more stability than conventional QR solutions.

If load decreases, the SQ33020 will enter discontinuous conduction mode (DCM) to reduce the switching frequency for higher efficiency. Under very light loads, the SQ33020 enters burst mode to reduce power loss.

The SQ33020 provides multiple mechanisms to ensure reliable operation: HV startup, X capacitor discharge, brown-out protection, output and VCC overvoltage protection (OVP), output undervoltage protection (UVP), internal and external overtemperature protection (OTP), and open-loop protection (OLP).

For higher efficiency, use the SQ33239 as a secondary side synchronous rectifier controller in conjunction with the SQ33020 to achieve zero voltage switching (ZVS).

The SQ33020 is available in an SSOP9 package.

Features

- DCM+QR Combined Operating Mode
- Programmable Gate Driver Current
- Switching Frequency Range: 25kHz–500kHz
- Automatic Valley Lockout from 1 to 6 cycles
- Accurate Output OCP
- Adaptive OCP (Limited Power Source)
- Low Frequency Burst Operation (1kHz)
- Switching Frequency Modulation to Reduce EMI Noise
- Internal Soft-Start
- Integrated 700V HV Startup
- Brown-In/Brown-Out Protections
- X Capacitor Discharge Protection (Optional)
- Programmable Output OVP and UVP
- Current Sense Resistor Short Protection
- Internal and External OTP
- Compact Package: SSOP9

Applications

- AC/DC Adapters
- PD Adapters
- Quick Battery Chargers

Typical Application

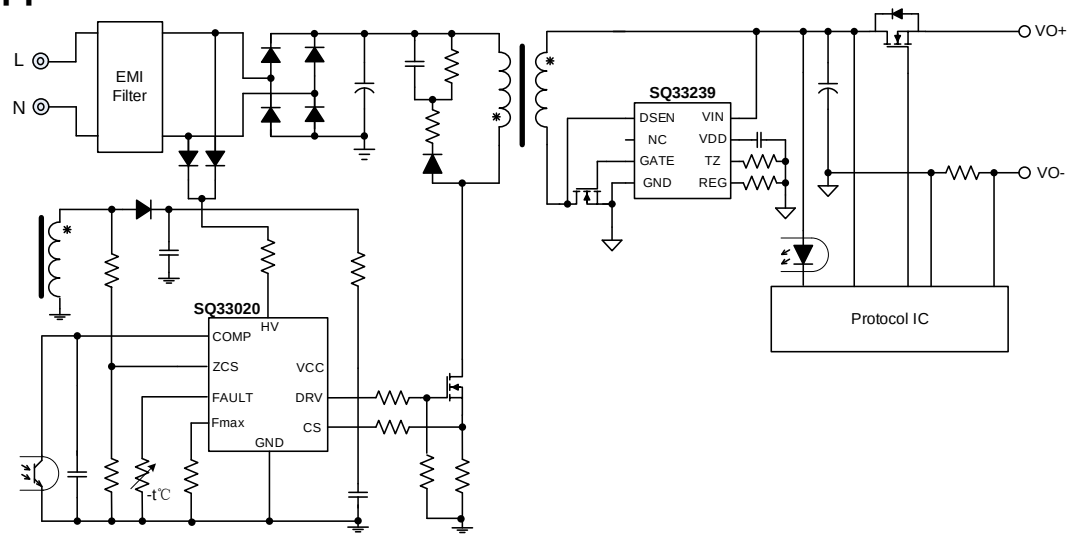


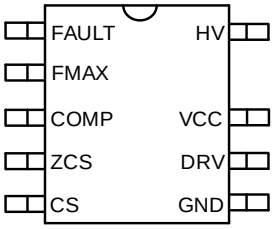
Figure 1. Typical Application Circuit using Synchronous Rectification (SR)

Ordering Information

Ordering Part Number	Package type	Top Mark
SQ33020FVP	SSOP9 RoHS-Compliant and Halogen-Free	**FDExyz**

x = year code, y = week code, z = lot number code

Pinout (top view)



Pin Description

Pin No	Pin Name	Pin Description
1	FAULT	External OTP and V_{OUT} OVP pin
2	FMAX	Maximum frequency (f_{MAX}) set pin with an external resistor to GND
3	COMP	Compensation voltage of secondary side, connected to an optocoupler
4	ZCS	Output voltage, input voltage, and QR valley detection pin
5	CS	Transformer current sensing pin
6	GND	Ground pin
7	DRV	Programmable MOSFET gate drive pin
8	VCC	Power supply pin
9	HV	HV startup, brown-in/out, X capacitor discharge detection pin

Block Diagram

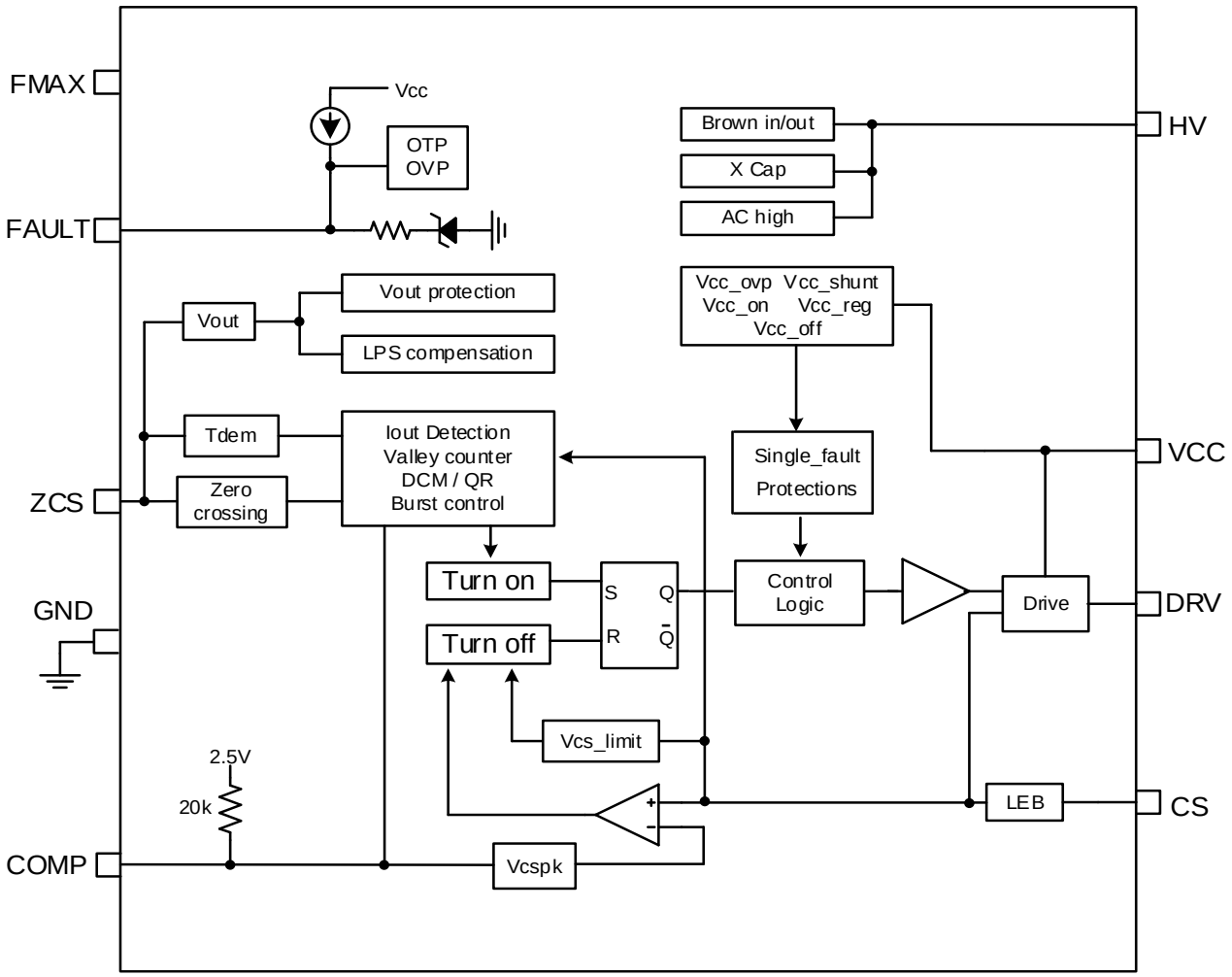


Figure 2. Block Diagram

Absolute Maximum Ratings

Parameter (Note 1)	Min	Max	Unit
HV	-0.3	700	V
VCC	-0.3	30	
DRV	-0.3	16	
CS, COMP, FAULT, FMAX	-0.3	4	
ZCS	-1 (Note 1)	7	
Junction Temperature, Operating	-40	150	°C
Lead Temperature (Soldering, 10s)		260	
Storage Temperature Range	-60	150	
Note1, Dynamic ZCS Negative Voltage in 50μs Duration		-1	V
Note1, Dynamic ZCS Negative Current in 50μs Duration		-2	mA
Human Body Model ESD (HV Pin and VCCH Pin) per ESDA/JEDEC JS-001-2017 (Note 6)		±1	kV
Human Body Model ESD (All Pins Except HV Pin and VCCH Pin) per ESDA/JEDEC JS-001-2017 (Note 6)		±2	kV
Charged Device Model ESD per JS-002-2018 (Note 6)		±500	V
Latch-Up Test per JEDEC78E (Note 6)		±100	mA
MSL Rating		3	

Thermal Information

Parameter (Note 2)	Min	Max	Unit
θ_{JA} Junction-to-Ambient Thermal Resistance		158	°C/W
θ_{JC} Junction-to-Case Thermal Resistance		30	
PD Power Dissipation TA = 25°C		0.79	W

Recommended Operating Conditions

Parameter	Min	Max	Unit
HV	-0.3	700	V
VCC	9	25	
DRV	7	15	
CS	-0.3	0.5	
ZCS	-0.3	3.0	
COMP	-0.3	2.5	
FMAX	-0.3	2.5	
FAULT	-0.3	3.0	
Junction Temperature Range	-40	125	°C
Ambient Temperature Range	-40	85	°C

Electrical Characteristics

(V_{VCC} = 13V (Note 7), T_A = 25°C unless otherwise specified)

Parameter (Note 4)		Symbol	Test Conditions	Min	Typ	Max	Unit
HV	HV Current to Charge VCC	$I_{HV\_CHARGE1}$	V_{HV} = 100V_{DC}, VCC = 0V	0.15	0.3	0.55	mA
			V_{HV} = 100V_{DC}, VCC = 3V	2.6	4.0	5.4	mA
	Current to Discharge X Capacitor	I_{HV_XCAP}			2.0		mA
	High or Low Voltage Detection	$HV_{TH\_AC\_HIGH}$		200	218	236	V
	AC Low Debounce Time	$t_{AC\_LOW\_DBC}$			20		ms
	Debounce Time to Detect AC Unplug	t_{UNPLUG_DBC}			100		ms
	BO Threshold	HV_{TH_BO}		65	72	79	V
	BI Threshold	HV_{TH_BI}			105		V
	BO Debounce Time	t_{BO_DBC}			90		ms
	Restart Time after BO	t_{ERROR_BO}			0.25		s
	BI Debounce Time	t_{BI_DBC}			200		µs
VCC	VCC Turn-On Threshold	V_{CC_ON}	V_{CC} rising	18	20	22	V
	VCC Turn-Off Threshold	V_{CC_OFF}	V_{CC} falling	7.5	8.0	8.5	V
	VCC Short Threshold	$V_{CC\_SHORT\_TH}$		0.5	0.7	0.8	V
	VCC Regulation Threshold	V_{CC_REG}		10	11	12	V
	VCC Regulation Hysteresis	V_{CC_REGHYS}			1.0		V
	Protection Timer after Error Trigger	t_{ERROR}			1.0		s
	VCC OVP Threshold	V_{CC_OVP}	V_{VCC} rising	26.4	28.0	29.6	V
	VCC OVP Debounce Cycles	N_{VCCOVP_DBC}			4		
	VCC Shunt Threshold	V_{CC_SHUNT}		25	27	29	V
	VCC Shunt Current Capability	I_{VCC_SHUNT}	VCC > $V_{CC,\ SHUNT}$		10		mA
	Normal Operation Current Consumption	$I_{CC\_OPERATING}$	C_L = open, f_{SW} = 50kHz		1.2		mA
	Standby Current Consumption	$I_{CC\_STANDBY}$	V_{COMP} < $V_{TH\_SLEEP\_IN}$	180	400	520	µA
FMAX	Frequency Set	f_{MAX}	R > 260kΩ R = 100kΩ R < 52kΩ or Floating	450	100 260 500	540	kHz
CS	Maximum Peak Current threshold	V_{CS_MAX}	Secondary Side Diode or SR Short	685	720	755	mV
	Leading Edge Blanking for V_{CS_MAX}	t_{CS_LEB1}			150		ns
	Delay Time from V_{CS_MAX} to PWM Off	t_{CSMAX_DELAY}			30		ns

Parameter (Note 4)		Symbol	Test Conditions	Min	Typ	Max	Unit
CS	V_{CS_MAX} Cycles	N_{VCSMAX_DBC}			4		
	V_{CS} Limit	V_{CS_LIMIT}		475	500	525	mV
	Leading Edge Blanking for V_{PK} and V_{CS_LIMIT}	t_{CS_LEB2}			250		ns
	OCP Threshold Normal	$V_{REF\_OCPNORMAL}$		805	850	895	mV
	OCP Threshold LPS High	$V_{REF\_OCPLPSH}$	$V_{ZCS} < V_{ZCSLPS\_LOW}$	805	850	895	mV
	OCP Threshold LPS Low	$V_{REF\_OCPLPSL}$	$V_{ZCS} > V_{ZCSLPS\_HIGH}$	470	495	520	mV
	OCP Debounce Time	$t_{IOUTOCP\_DBC}$			200		ms
	Delay Time from V_{CS_LIMIT} to DRV Falling	t_{CS_DELAY2}			30		ns
	Delay Time from V_{PK} Control to DRV Falling	t_{CS_DELAY3}			30		ns
	V_{CS} Minimum in DCM	V_{CSMIN_DCM}		65	80	95	mV
	Soft-Start Time	t_{SST}			10		ms
	QR Mode Frequency of Modulation	$f_{MODULATION\_QR}$			4		kHz
	V_{CSPK} Modulation Amplitude in QR Mode	$V_{QR\_MODULATION1}$	Valley = 1–3		20		mV
			Valley = 4–6		30		mV
	CS Short-Circuit Protection	V_{CS_SHORT}	t_{ON} = 6.2μs		60		mV
	Restart Time after CS Short Circuit	$t_{ERROR\_CSSHORT}$			0.25		s
	Current Mirror In t_{ON}	V_{CS_MIRROR}	I_{ZCS}:I_{CS}		12:1		/
ZCS	OVP Threshold	V_{ZCS_OVP}		2.36	2.50	2.64	V
	OVP Threshold Debounce Cycles	N_{ZCSOVP_DBC}			4		
	UVP Threshold	V_{ZCS_UVP}			150		mV
	UVP Threshold Debounce Time	$t_{VOUTUVP\_DBC}$			20		ms
	Maximum Value of Off Blanking Time	t_{ZCSLEB_MAX}		1.6	2.3	3.0	μs
	Minimum Value of Off Blanking Time	t_{ZCSLEB_MIN}		0.65	0.9	1.3	μs
	Maximum Off-Time	t_{OFF_MAX}		90	120	150	μs
	Zero-Cross Point	V_{ZCS_ZERO}			0		mV
	QR Turn-On Delay	$t_{ZCS\_ONDELAY}$			100		ns
	LPS High Point	V_{ZCSLPS_HIGH}		1.74	1.90	1.98	V
	LPS Low Point	V_{ZCSLPS_LOW}		1.06	1.12	1.24	V
Fault	Current Source for OTP Detection	I_{OTP}		46.5	49.0	51.5	μA
	OTP Threshold	V_{OTP_TH}		0.37	0.40	0.43	V
	OTP Exit Threshold	$V_{OTPEXIT\_TH}$			0.45		V
	Clamp Diode for OVP	$V_{OVPDIODE}$		1.1	1.3	1.5	V
	Capability of Clamp Diode for OVP	I_{FAULT_OVP}			1		mA
	OVP Threshold	V_{OVP_TH}			2.5		V

Parameter (Note 4)		Symbol	Test Conditions	Min	Typ	Max	Unit
	Debounce Time to Trigger OTP/OVP	$t_{FAULTOTP/OVP\_DBC}$	$V_{FAULT} < V_{OTP\_TH}$ $V_{FAULT} > V_{OVP\_TH}$		100		μs
COMP	Internal Pullup Voltage	V_{COMP_PULLUP}		2.2	2.5	2.8	V
	Internal Pullup Resistor	R_{COMP_PULLUP}			20		kΩ
	V_{CS_LIMIT} Point	V_{COMP_LIMIT}			1.9		V
	QR Mode to DCM Change Threshold	V_{COMPTH_DCM}			1.0		V
	Hysteresis of QR Mode to DCM	V_{COMPTH_DCMHYS}			0.1		V
	Minimum Switching Frequency Threshold	V_{COMP_FMIN}		0.55	0.7	0.85	V
	Enter Burst Mode Threshold	$V_{COMP\_BURSTIN}$	V_{COMP} falling	0.19	0.25	0.31	V
COMP	Exit Burst Mode Threshold	$V_{COMP\_BURSTOUT}$	V_{COMP} increasing		0.45		V
	Start PWM Threshold in Burst Mode	$V_{COMP\_BURSTSTART}$	V_{COMP} increasing		0.35		V
	Burst Frequency	$V_{COMP\_BURSTFREQ}$			1		kHz
	OLP Threshold	V_{COMP_OLP}	V_{COMP} rising	1.95	2.2	2.45	V
	OLP Debounce Time	t_{OLP_DBC}	$V_{COMP} > V_{COMP\_OLP}$		50		ms
DRV	High Voltage Clamp	V_{DRV-CS_CLAMP}		12.0	13.5	15.0	V
	Programmable Driver Current	I_{DRV}	DVR-GND: 43kΩ		10		mA
			DVR-GND: 22kΩ		20		mA
			DVR-GND: 10kΩ		40		mA
			DVR-GND: < 2kΩ		Not supported		
	Sink Current	I_{DRV_SINK}			800		mA
	Maximum t_{ON}	t_{ON_MAX}		14	20	26	μs
	Frequency Limit in DCM Mode	f_{LIMIT_DCM}			75		kHz
	Frequency Minimum in DCM Mode	f_{MIN_DCM}		20	25	32	kHz
	DCM Mode Modulation Frequency	$f_{MODULATION\_DCM}$			250		Hz
	Minimum Valley Number in QR Mode	$VALLEY_{NUMBER}$	HV < 218V	1		6	
			HV > 218V	1		6	
Internal OTP	OTP Threshold (Note 5)	$T_{OVP\_SHUNTDOWN}$			150		°C
	Recovery Threshold (Note5)	$T_{OVP\_RECOVERY}$			130		°C

Note 1: Stresses beyond the “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: θ_{JA} is measured in the natural convection at TA = 25°C on a low effective single layer thermal conductivity test board of JEDEC 51-3 thermal measurement standard. Test condition: Device mounted on “2 x 2” FR-4 substrate PCB, 2oz copper, with minimum recommended pad on top layer and thermal via to bottom layer ground plane.

Note 3: The device is not guaranteed to function outside its operating conditions.

Note 4: Unless otherwise stated, limits are 100% production tested under pulsed load conditions such that $T_A \cong T_J$ = 25C. Limits over the operating temperature range (See recommended operating conditions) and relevant voltage range(s) are guaranteed by design, test, or statistical correlation.

Note 5: Guaranteed by design or statistical correlation and not production tested.

Note 6: Meets ESDA/JEDEC JS-001-2017 and JEDEC78E.

Note 7: Increase VCC pin voltage higher than V_{CC_ON} (max) voltage, then reduce it to 13V.

Detailed Description

HV Startup and Power Supply

The HV pin charges the VCC capacitor at AC power-on. When VCC voltage rises above the startup threshold, the HV circuits will be turned off to reduce power loss.

In situations when the device enters protection mode, the PWM operation is stopped for a t_{ERROR} time. Because of the power consumption during t_{ERROR}, the VCC capacitor voltages will drop. When VCC falls to V_{CC_REG}, HV circuitry is enabled again to charge the capacitors until VCC > (V_{CC_REG} + V_{CC_REGHYS}). After t_{ERROR}, the internal logic will be reset, and a restart sequence is initiated.

QR Mode (Automatically Selected Valley Number between 1 and 6)

In QR mode, PWM turns on at the valley point of the MOS FET drain voltage. This improves EMI and efficiency. V_{CSPK} is controlled by V_{COMP}, and the valley number is controlled by the output load. When V_{COMP} is higher than (V_{COMP_THDCM} + V_{COMPTH_DCMHYS}), QR mode is enabled and starts on the 6th valley number. As the load increases, the valley number decreases in one-step increments until it reaches the minimum value.

Valley Detect

The waveform in Figure 3 shows the valley detection method. When the falling edge of the zero-crossing voltage appears at the ZCS pin, the SQ33020 will turn on the MOS FET after a delay.

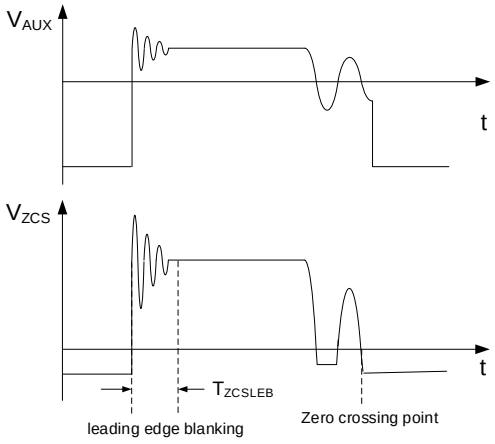


Figure 3. Valley Detection

Noise is present at the ZCS pin when the MOS FET turns off, which may affect valley detection. The SQ33020 uses a blanking time to avoid noise interference, which is described in the *Output OVP and UVP* section.

DCM Mode

When V_{COMP} is lower than V_{COMPTH_DCM}, DCM mode is enabled. In DCM mode, V_{CSPK} and the switching frequency are controlled by V_{COMP}. PWM turns on instantly at f_{SW} and does not wait for the valley point. As load decreases, the frequency first decreases from $f_{LIMIT,DCM}$ to $f_{MIN,DCM}$, and the device switches operation to PFM mode to maintain high efficiency. When the frequency has decreased to $f_{MIN,DCM}$ and the load continues decreasing, V_{CSPK} begins decreasing to maintain constant output voltage.

Burst Mode

When frequency and V_{CSPK} have decreased to their respective minimum values, if the output load continues decreasing, V_{COMP} becomes lower than $V_{COMP\_BURSTIN}$. In this case the device starts operating in Burst mode. PWM will start when V_{COMP} is higher than $V_{COMP\_BURSTSTART}$. The PWM number of switching cycles is controlled by t_{BURST} in order to keep burst frequency lower than the set value. PWM operation will continue until the set number of cycles are completed. PWM then stops and waits for the next rising edge of $V_{COMP\_BURSTSTART}$. With this method, the burst frequency is low, and audible noise is reduced.

When V_{COMP} is higher than $V_{COMP\_BURSTOUT}$, the SQ33020 will enter DCM mode.

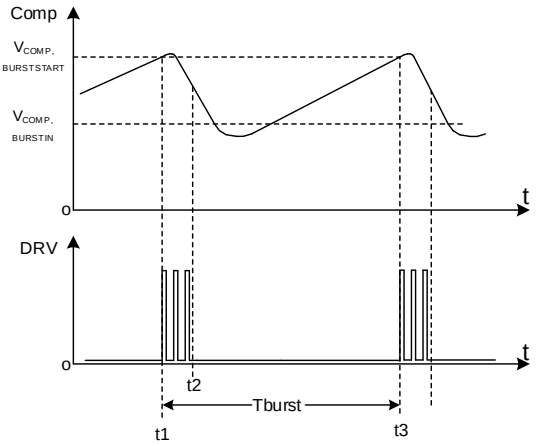


Figure 4. Quiet Burst

VCC Power Supply

Figure 5 shows a typical VCC supply circuit. During the X capacitor discharge process, C11 voltage will be charged to V_{CC_SHUNT}. In this case, a 35V capacitor voltage rating is recommended.

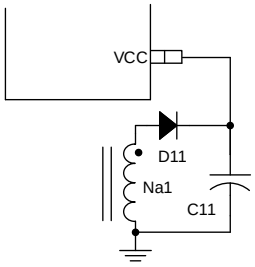


Figure 5. Typical Circuit for One-Winding Application

Accurate Output Overcurrent Protection (OCP)

The SQ33020 detects output current at the primary side. The CS pin samples voltage across R_{CS} before PWM turn-off. When Ns winding current falls to zero, the ZCS pin records the demagnetization time. The SQ33020 calculates output current using these two signals, and the result is compared with V_{REF_OCP} (internal threshold). When the result is higher than V_{REF_OCP} for a period of $t_{IOUTOCP\_DBC}$, PWM stops and a timer begins. After time t_{ERROR} elapses, logic will be reset and HV will charge V_{CC} to V_{CC_ON} for restart.

I_{OUT_OCP} can be set by R_{CS} with following formula.

$$I_{OUT\_OCP} = \frac{0.93 \times V_{RER\_OCP} \times N_{PS}}{6 \times R_{CS}}$$

where V_{REF_OCP} is the internal voltage of SQ33020; N_{PS} is the transformer N_P/N_S; R_{CS} is R5 shown in Figure 6.

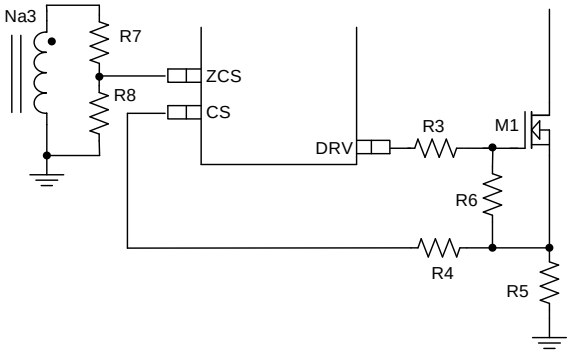


Figure 6. Typical Circuit for R_{CS} Calculation

The SQ33020 uses R4 to compensate the system error. If I_{OUT_OCP} becomes higher with an input voltage increase, R4 should be increased. If I_{OUT_OCP} falls with an input voltage increase, which indicates excess compensation, R4 should be reduced.

For applications where M1 is a super junction MOS, the R4 recommended value is between 1kΩ to 3kΩ. When M1 is a GaN FET, such as NV611x and NV612x, the R4 recommended value is between 200Ω to 1kΩ.

Output OCP Modes

In quick charge applications, V_{OUT} range is usually very wide (3.3V to 21V, for example). I_{OUT} range is also very wide. The SQ33020 provides two OCP options to accommodate different applications.

The first option is Normal OCP mode. This mode is suitable when the current limit doesn't change for different output voltages. Output voltage and current selections include the following: 5V/3A, 9V/3A, 12V/3A, 15V/3A, 20V/3.25A, 3.3V–21V/3A.

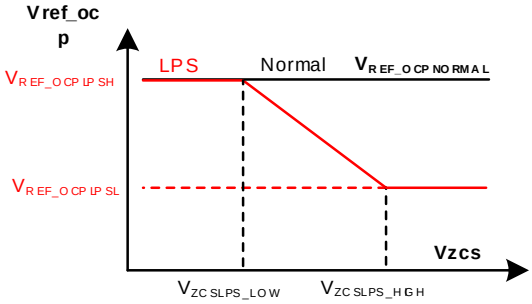


Figure 7. Two Output OCP Modes

The second option is limited power source (LPS) OCP mode. This mode of operation is suitable for applications where the overall power delivered is used to determine the OCP threshold, according to the programmed output voltage. If Normal OCP option would be used, in some cases the OCP threshold could expose the part to unsafe power levels. For example, assuming that I_{OUT_OCP} is set to 7.0A, when V_{OUT} is changed to 20V, maximum output power will be 140W. This is prohibited in UL60950 or later safety standards.

The SQ33020's LPS OCP option is suitable for operating the part reliably across all operating conditions. V_{REF_OCPLPS} is related to V_{OUT}, and I_{OUT_OCP} can be set by R_{CS} when V_{OUT} is highest. When V_{OUT} is lower, V_{REF_OCPLPS} becomes higher. At V_{OUT} = 10V, I_{OUT_OCP} is higher than 6.5A and a 10V/6.5A load won't trigger output OCP.

Typical output voltage and current selections include the following: 5V/3A, 9V/3A, 10V/6.5A, 12V/5A, 15V/4A, 20V/3.25A, and 5V-12V/5A.

X Capacitor Discharge and Output OCP using the ZCS Resistor

The X capacitor discharge and Output OCP functions can be selected using the ZCS resistor. When the X capacitor is enabled, HV should be connected to the AC line via two diodes. When the X capacitor is disabled, HV can be connected to V_{BUS} to eliminate the diodes and reduce solution cost.

Table 1. ZCS Resistors Configuration

ZCS Pulldown (R8)	X Capacitor Function	Output OCP
25–27kΩ ±1%	Disabled	Normal
13kΩ ±1%	Enabled	Normal
7.5kΩ ±1%	Disabled	LPS
3.0–3.6kΩ ±1%	Enabled	LPS

The ZCS_OVP threshold is 2.50V. With R8 selected, R7 can be calculated according to V_{OUT_OVP} and Na/Ns. Resistor R4, in series with CS, should be adjusted as well. If I_{OUT_OCP} (user selected) increases according to V_{AC}

rising, the value of R4 should be increased for more compensation.

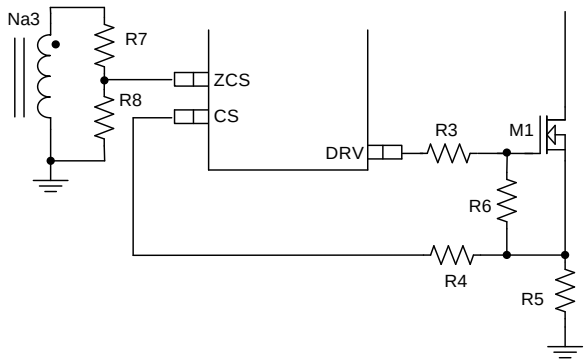


Figure 8. X Capacitor and Output OCP using ZCS Resistor

Programmable Drive Current

During turn-on, the SQ33020 uses constant current to charge the input M1 capacitance, Cgs, and improve EMI performance. During turn-off, the DRV pin will be pulled down quickly to reduce turn-off loss. Traditional drive resistors and diodes are not required. R3 is used to make slight adjustments to the turn-off speed. The recommended value of R3 is 10Ω–30Ω.

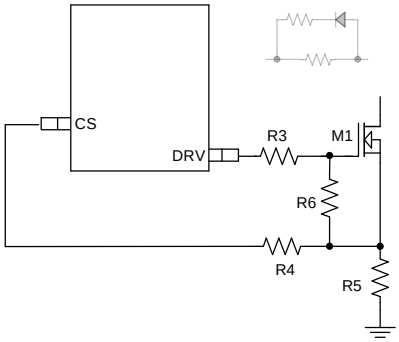


Figure 9. MOSFET Drive Circuit

At turn-on, the constant current value can be selected using R6 based on Table 2:

Table2. R6 and Constant Current Value

R6	Constant Current
10kΩ	40mA
22kΩ	20mA
43kΩ	10mA
<2kΩ	Not Supported

The device enters protection mode for R6 values below 2kΩ where PWM switching is disabled.

Using a lower current, the MOS turn-on speed will be slower and EMI performance will be better. The R6 value is measured during startup, and the current value is fixed until the next startup.

Frequency Limit Curve

For QR mode operation, when load decreases, switching frequency will increase. This will also increase switching loss, so the FMAX pin can be used to limit the maximum frequency. The relationship between frequency limit and the FMAX pin resistor is shown in Figure 10.

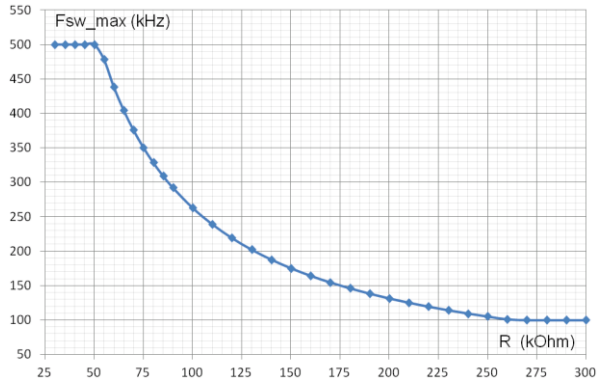


Figure 10. Frequency Limitation Curve

When the FMAX pin is floating, or if the resistor is lower than 30kΩ, the frequency limit is 500kHz. When frequency limit is triggered, PWM will turn on at the next valley.

Frequency Modulation

In QR mode, the SQ33020 adds a triangle voltage on V_{CS} for frequency modulation. If the valley number is between 1 and 3, the modulation amplitude is set to 20mV. If the valley number is between 4 and 6, the modulation amplitude is set to 30mV in order to obtain an effective range of frequency modulation.

Soft-Start

At startup, when V_{COMP} rises to $V_{COMP\_BURSTSTART}$, PWM operation starts and V_{CS} increases from the minimum value linearly. Under heavy load or V_{OUT} short conditions, soft-start will terminate after a period of t_{SST}. Under light load or no-load conditions, when the V_{CS} value determined by V_{COMP} is lower than the value determined by soft-start, soft-start will terminate and V_{COMP} will control V_{CS}.

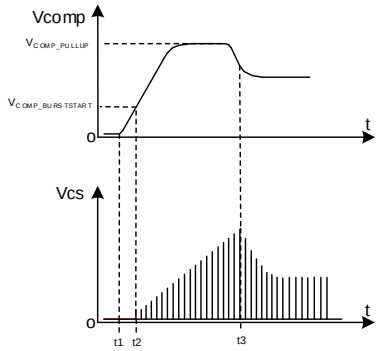


Figure 11. Soft-Start Process

Under startup or V_{OUT} short conditions, V_{OUT} and ZCS are very low. If ZCS cannot detect an effective valley signal, t_{OFF_MAX} will be enabled. This is helpful to reduce the voltage stress on the SR MOSFET V_{DS}.

V_{CS_LIMIT}

After time t_{CS_LEB2} in each cycle, when V_{CS} is higher than V_{CS_LIMIT}, PWM will turn off immediately. The decision is made cycle by cycle and will not affect the next cycle's PWM on-time.

V_{CS_MAX} Protection

Under normal operating conditions, V_{CS_LIMIT} can limit MOS peak current and provide sufficient protection. When the transformer winding or the secondary diode short circuits, the current slope is very high and the transformer will enter saturation state. In this situation, the current can rise to a much higher level during t_{CS_LEB2}. The SQ33020 can detect V_{CS} after t_{CS_LEB1}, which is shorter than t_{CS_LEB2}. If V_{CS} is higher than V_{CS_MAX} for four consecutive cycles, PWM operation stops and the timer starts. After t_{ERROR}, the logic is reset and a restart is triggered, with HV charging V_{CC} to V_{CC_ON}.

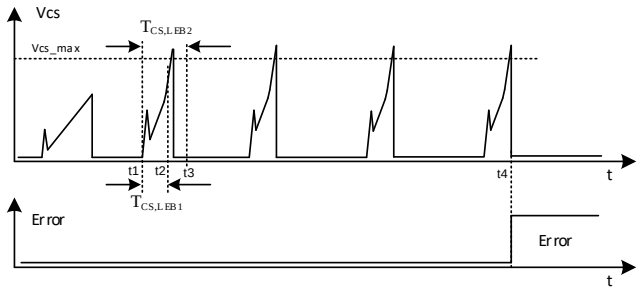


Figure 12. V_{CS_MAX} Process

Brown-In and Brown-Out

When input voltage is lower than 90V AC, current and heat dissipation on the transformer and primary MOSFET are very high. The SQ33020 provides brown-in (BI) and brown-out (BO) protections to protect the power supply. Brown-in and brown-out are defined as follows:

- BI: HV voltage is higher than $HV_{TH,BI}$ and lasts for $t_{BI,DBC}$
- BO: HV voltage is lower than $HV_{TH,BO}$ and lasts for $t_{BO,DBC}$

After a BO event, PWM stops. Then, after a t_{ERROR_BO} delay, the logic is reset and a startup sequence is initiated, with the HV input charging VCC to V_{CC_ON}.

X Capacitor Discharge

Under light load, when the charger is unplugged from the AC source, there may be remaining high voltage on the input terminals, which can present a safety concern.

The SQ33020 uses the HV pin to discharge the X capacitor. HV is connected to the AC side through R1, D1, and D3. The recommended R1 value is 1kΩ–10kΩ, which protects against surge voltages on the AC line.

If there is no HV rising edge for continuous time t_{UNPLUG_DBC}, an AC unplug condition is detected and PWM stops. HV sources an I_{HV_XCAP} current to the VCC pin. As a result, VCC rises to V_{CC_SHUNT} and HV falls linearly. When VCC becomes lower than V_{CC_OFF}, the discharge stops.

The voltage rating of the VCC capacitor should be higher than V_{CC_SHUNT}. A 35V voltage rating is recommended.

During X capacitor discharge, when a rising edge on HV (indicating AC re-plug) is detected, the discharge is terminated immediately. The t_{ERROR} timer continues. During t_{ERROR}, HV keeps VCC between V_{CC_REG} and (V_{CC_REG} + V_{CC_REGHYS}). After a t_{ERROR} delay, the logic will be reset and a startup sequence is initiated, with the HV input charging V_{CC} to V_{CC_ON}.

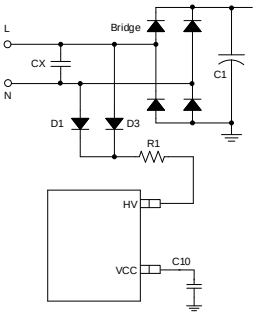


Figure 13. X Capacitor Discharge Circuit

Figure 14 shows the discharge waveforms:

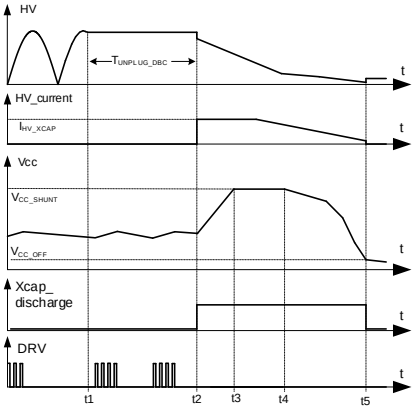


Figure 14. X Capacitor Discharge Waveforms

- At t1, AC unplug occurs.
- At t2, AC unplug is confirmed. PWM stops and HV sources current to V_{CC}.
- At t3, V_{CC} rises to V_{CC_SHUNT}.
- At t4, X capacitor discharge current is lower than V_{CC} dissipation and V_{CC} begins falling.
- At t5, V_{CC} is lower than V_{CC_OFF} and the discharge stops.

Output Overvoltage and Undervoltage Protection

The SQ33020 detects the output voltage through the ZCS pin and provides output overvoltage protection (OVP) and undervoltage protection (UVP). There is parasitic resonance on the AUX winding when the primary MOSFET turns off, so the SQ33020 uses blanking time to avoid false triggering. Blanking time is adaptive according to V_{CSPK}. When V_{CSPK} is below 200mV, primary current is low and energy stored in leakage inductance is also low. Parasitic resonance on auxiliary winding will be shorter, so blanking time is also shorter. Blanking time increases to the maximum value as V_{CSPK} rises to 500mV.

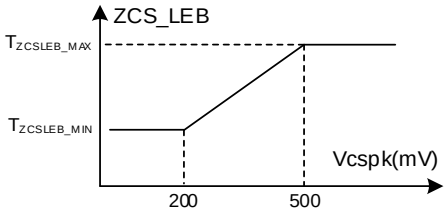


Figure 15. ZCS Blanking Time

When ZCS voltage is higher than V_{ZCS_OVP} for N_{ZCSOVP_DBC} cycles, ZCS_OVP is triggered and PWM stops. After a t_{ERROR} delay, the logic is reset and a startup sequence is initiated, with the HV input charging V_{CC} to V_{CC_ON}.

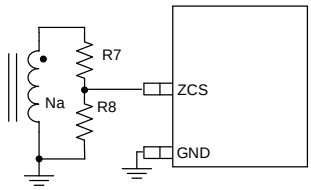


Figure 16. ZCS OVP Setting

The output OVP threshold is calculated as follows:

$$V_{OUT\_OVP} = V_{ZCS\_OVP} \times \frac{R7 + R8}{R8} \times \frac{Ns}{Na}$$

When ZCS voltage is lower than V_{ZCS_UVP} continuously for a period of $t_{VOUTUVP\_DBC}$, ZCS_UVP is triggered and PWM stops. After a t_{ERROR} delay, the logic is reset and a startup sequence is initiated, with the HV input charging V_{CC} to V_{CC_ON}.

Note: The pulldown resistor R8 value should be selected first, based on use of the X capacitor and output OCP settings. Then, R7 should be calculated according to the above equation. UVP is used to avoid continuous operation under V_{OUT} short-circuit conditions and is not mandatory for the design.

VCC Overvoltage Protection

The SQ33020 provides V_{CC} overvoltage protection (OVP) to protect the IC from abnormal high voltage caused by an open feedback loop or improper N_A winding. When V_{CC} rises to V_{CC_SHUNT} and external power current capability is higher than the shunt ability, V_{CC} can continue rising.

V_{CC} is continuously monitored. If V_{CC} is higher than V_{CC_OVP} for four continuous cycles, V_{CC} OVP is triggered and PWM stops. After a t_{ERROR} delay, the logic is reset and a startup sequence is initiated, with the HV input charging V_{CC} to V_{CC_ON}.

If the error condition still exists after restart, the IC will operate in hiccup mode.

Open-Loop Protection

If the output is short-circuited, the optocoupler circuit is open, or the load increases too much, V_{COMP} will increase. When V_{COMP} is higher than V_{COMP_OLP} and lasts for t_{OLP_DBC}, open-loop protection (OLP) is triggered and PWM stops. After a t_{ERROR} delay, the logic is reset and a startup sequence is initiated, with the HV input charging V_{CC} to V_{CC_ON}.

FAULT Overtemperature and Overvoltage Protection

The FAULT pin can be used for detecting overvoltage (OVP) and overtemperature (OTP) protection conditions. During normal operation, the current of I_{OTP} is clamped by D12. D12 clamp voltage is selected to be between the OTP threshold and the OVP threshold. Therefore, neither protection is triggered.

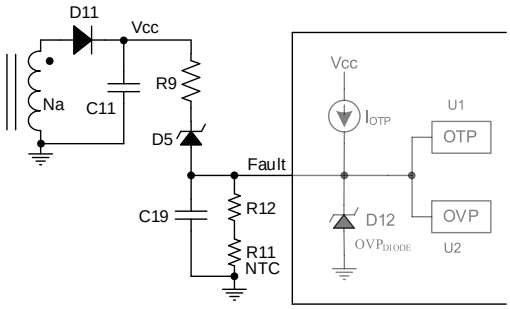


Figure 17. Fault OTP and OVP

Under error conditions, V_{CC} will rise. In this case, if D5 also fails, the pullup current might exceed D12 clamp capability and the FAULT pin voltage will be pulled up. When the FAULT pin is higher than V_{OVP_TH} and lasts for a period of $t_{FAULTOTP/OVP\_DBC}$, FAULT OVP is triggered and PWM stops. After a t_{ERROR} delay, the logic is reset and a startup sequence is initiated, with the HV input charging V_{CC} to V_{CC_ON}.

R11 is a negative temperature coefficient (NTC) resistor. As temperature rises, R11 resistance falls. When R11 resistance is low enough, there will be no current flowing into D12 and the I_{OTP} current will flow into R11. As I_{OTP} does not change, FAULT voltage will fall along with R11

resistance. When FAULT voltage is lower than V_{OTP_TH}, FAULT OTP is triggered and PWM stops. After a t_{ERROR} delay, the logic is reset and a startup sequence is initiated, with the HV input charging V_{CC} to V_{CC_ON}. After restart, the FAULT pin is monitored, and PWM will not begin until FAULT voltage is higher than $V_{OTPEXIT\_TH}$.
R9 is used to limit the current flowing into the FAULT pin. The OVP threshold is primarily decided by D5 breakdown voltage. R12 is used to adjust the OTP threshold slightly. C19 is used to filter noise, with a recommended value of 100pF.

CS Pin Short Circuit

During t_{ON} of every PWM cycle, V_{CS} is sampled every 6.2μs and compared with V_{CS_SHORT}. If $V_{CS} < V_{CS\_SHORT}$, short-circuit protection is triggered and PWM stops. After a $t_{ERROR\_CSSHORT}$ delay, the logic is reset and a startup sequence is initiated, with the HV input charging V_{CC} to V_{CC_ON}.

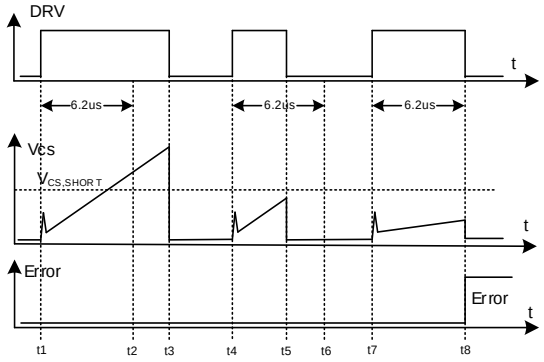


Figure 18. CS Short Protection

Figure 18 shows the short-circuit protection logic:

- At t2, V_{CS} is higher than V_{CS_SHORT}. No protection.
- At t5, the 6.2μs timer has not expired. No comparison is needed. No protection.
- At t8, V_{CS} is lower than V_{CS_SHORT} at 6.2μs mark. Protection is triggered.

Internal OTP

The SQ33020 continuously monitors the die temperature during normal operation. When the die temperature rises above the OTP threshold, PWM stops. After a t_{ERROR} delay, the logic is reset and a startup sequence is initiated, with the HV input charging V_{CC} to V_{CC_ON}.

Design Guide

BUS Capacitor Calculation

Generally, bulk capacitor CBUS is selected according to the following rules:

- No PFC: 1.5–1.8μF per watt (output power)
- With PFC: 0.5–0.8μF per watt (output power)

Minimum BUS Voltage Calculation

Minimum BUS voltage occurs when input voltage V_{AC} is lowest and output current reaches its rated value. When there is no power factor correction (PFC) circuit before the flyback, minimum BUS voltage is calculated as follows:

$$V_{BUS\_MIN} = \sqrt{2V_{IN\_MIN}^2 - \frac{P_O(1-K_{CH})}{\eta C_{BUS} f_o}}$$

where K_{CH} is the BUS capacitor charge coefficient (generally K_{CH} is set to 0.2–0.3); η is conversion efficiency; f_O is the AC input frequency.

When selecting the necessary capacitors, the following aspects must be considered:

- The actual capacitance for aluminum capacitors is only 85-90% of nominal value
- Component tolerance

The following examples are helpful for fast selection and can be used as a reference.

- 30W solution, with no boost PFC circuit. Bus nominal capacitance is 27 + 27μF. V_{BUS_MIN} is as follows:

Output Power	30W	35W	40W	45W
AC90V 50Hz	86V	80V	75V	68V
AC90V 60Hz	93V	87V	83V	78V

For optimal performance, V_{BUS_MIN} should be higher than 80V.

- 66W solution, no boost PFC circuit. Under full load 20V, 3.3A, V_{BUS_MIN} is as follows:

Bus Nominal Capacitance	82+22μF	82+10μF	82μF	68μF
AC90V 50Hz	82V	78V	72V	60V

For optimal performance, V_{BUS_MIN} should be higher than 80V.

- 140W solution, boost + flyback topology. Output is 28V, 5A. Bus nominal capacitance is 39+39μF.
  - At AC90V 50Hz, boost PFC outputs DC240V. V_{BUS} is 222V(min) to 253V(max). Ripple is 31V.
  - At AC176V 50Hz, boost PFC outputs DC350V. V_{BUS} is 338V(min) to 362V(max). Ripple is 24V.

Transformer Parameters Calculation

1. **Primary/secondary turns ratio: N_{PS}**

   N_{PS} is limited by voltage stress on the primary MOSFET

$$N_{PS} \le \frac{V_{MOS\_BR}K_{DR} - \sqrt{2}V_{IN\_MAX} - \Delta V_{SN}}{V_O + V_{D\_F}}$$

   where V_{MOS_BR} is the breakdown voltage of the primary MOSFET; K_{DR} is the V_{DS} de-rating factor of the power MOS; $V_{IN,MAX}$ is always AC264V; V_{D_F} is

the forward voltage of the secondary rectification diode (If SR is used on the secondary side, use V_{D_F} = 0); ΔV_{SN} is the voltage spike at primary MOS turn-off. A starting value of 50V can be used for the calculation.

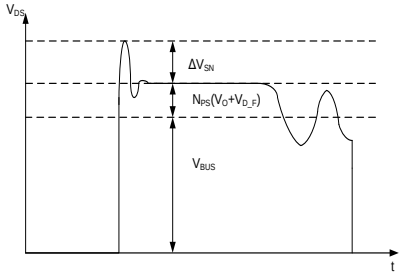


Figure 19. Primary V_{DS} Waveform

After N_{PS} is determined, the reflected voltage can be calculated as follows:

$$V_{OR} = N_{PS} \times (V_O + V_{D\_F})$$

2. Primary Inductance: LP

The SQ33020 provides operates in QR and DCM modes (CCM is not available). The transformer primary inductance is mainly related to switching frequency. With V_{BUS} being at its minimum value, L_P can be calculated as follows:

$$L_P = \frac{1}{2 \times F_{SW\_MIN} \times V_O \times I_O \times} \times \left(\frac{V_{BUS\_MIN} \times V_{OR}}{V_{BUS\_MIN} + V_{OR}}\right)^2$$

where V_O is the output voltage and the unit is V; N_{PS} is the primary/secondary turns ratio; V_{BUS_MIN} is the minimum voltage after the bridge (V); f_{SW_MIN} is the frequency at V_{BUS_MIN} (kHz); I_O is the output current (A); L_P is the primary inductance (mH).

The parameters V_O, N_{PS}, V_{BUS_MIN} and I_O have been determined. Only F_{SW_MIN} needs to be selected. When f_{SW_MIN} is higher, L_P will be lower. The frequency for AC230V designs will also be higher.

For a typical application, f_{SW_MIN} is approximately 100kHz-130kHz, at V_{BUS_MIN} (usually 80V-90V). Then, frequency at V_{BUS_MAX} (370V) is approximately 160kHz-220kHz.

3. Turns of primary winding: N_P

(a) Select the magnetic core and confirm the effective core area (AE)

(b) Select B_{MAX} for the magnetic core (0.32T–0.36T)

(c) Calculate primary R_{CS} (preliminary):

$$R_{CS} = \frac{0.93 \times V_{REF\_OCP} \times N_{PS}}{6 \times I_{OUT\_OCP}}$$

where V_{REF_OCP} is the internal threshold, I_{OUT_OCP} is the OCP threshold, which is selected based on the maximum output current. For example, if the maximum current required is 3A, then 3.3A can be used for I_{OUT_OCP}.

(d) Calculate maximum primary peak current

$$I_{PPK\_MAX} = \frac{V_{CS\_LIMIT}}{R_{CS}}$$

where V_{CS_LIMIT} is 0.5V.

(e) Calculate primary turns: N_P

$$N_P = \frac{L_P \times I_{PPK\_MAX}}{B_{MAX} \times A_E}$$

4. Turns of secondary winding: NS

$$N_S = \frac{N_P}{N_{PS}}$$

In the actual design, however, f_{SW_MIN} is difficult to determine. If a random value is selected, later calculations may be difficult and this may be unsuitable to the transformer bobbin. The following flow is suggested for a reduced number of iterations and predictable results:

1. Select transformer and AE
2. Determine winding width of the bobbin
3. Select N_S wire gauge
4. Determine N_S
5. Determine V_{OR} and N_{PS}
6. Calculate N_P
7. Select N_P wire gauge
8. Calculate R_{CS}
9. Calculate I_{PPK_MAX}
10. Determine B_{MAX}
11. Calculate L_P

With this procedure, f_{SW_MIN} is not an input parameter. When L_P is calculated, the switching frequency f_{SW} is determined as well. This will always lead to a satisfactory design, and efficiency will always be close to optimal for a given transformer.

5. Turns of auxiliary winding: N_A

For fast-charge applications, V_{OUT} range is wide. Turns of AUX winding should take V_{OUT_MAX} and V_{OUT_MIN} into consideration.

Efficiency can be increased by using two AUX windings, if a slight increase in BOM cost is acceptable.

- AUXL can supply V_{CC} at V_{OUT_MAX}.
- $18V < \frac{V_{OUT\_MAX}}{N_S} \times N_{AUXL} < 22V$
- AUXH can supply V_{CC} at V_{OUT_MIN}.
- $10V < \frac{V_{OUT\_MIN}}{N_S} \times N_{AUXH} < 14V$

In low-cost applications, one winding (AUXH) is sufficient. The number of turns for the AUXH winding is the same as N_{AUXH} in the above formula.

Secondary Rectifier MOSFET Selection

Under the conditions of V_{BUS_MAX} and V_{OUT_OVP}, the reverse voltage of the secondary rectification MOSFET will reach its maximum level. The maximum voltage (ignoring the voltage spike when the primary MOSFET is turned on) is calculated as follows:

$$V_{D\_R\_MAX} = \frac{\sqrt{2}V_{IN\_MAX}}{N_{PS}} + V_{O\_OVP}$$

Maximum instantaneous forward current is calculated as follows:

$$I_{SPK\_MAX} = I_{PPK\_MAX} \times N_{PS}$$

- For a 66W (20V, 3.3A) solution, BSC098N10NS5 is recommended, which has 100V, 8.2mΩ (V_{GS} = 10V) ratings.
- For a 90W (20V, 4.5A) solution, BSC0805LS is recommended, which has 100V, 6.0mΩ (V_{GS} = 10V) ratings.
- For a 120W (20V, 6.0A) solution, two MOSFETs in parallel are recommended, primarily for heat dissipation. Using two BSC098N10NS5, which has 100V, 8.2mΩ (V_{GS} = 10V) ratings.

Ensure that the selected MOSFET can dissipate the heat without exceeding the target acceptable temperature increase. Validate the design by performing temperature measurements under worst-case load and ambient temperature conditions.

Layout Considerations

Follow these PCB layout guidelines for optimal performance and EMI considerations:

- Signals are grouped into two categories:
  - Switching nodes: primary drain/AUX/core; secondary drain/AUX/core.
  - Important signal nodes (easily disturbed):
    - Primary: CS, FAULT, comp, ZCS, f_{MAX}, etc.
    - Secondary: REG, TZ (TZ pin of SQ33239), feedback loop, etc.
- To guarantee normal operation, important signal nodes should be as far as possible from switching nodes. If PCB routing is difficult, static nodes should be used as shielding between switching and signal nodes. Static nodes can be V_{BUS}, GND, VCC, VCCH, V_{OUT}, SGND, etc.
- In order to optimize EMI performance, switching nodes on the PCB layout should be as small as possible. Switching nodes should not be selected for heat sinking, such as MOS drain.
- In order to obtain good EMI performance, the following current loops should be as small as possible:
  - Current path during t_{ON}: bus capacitor → transformer → MOS → R_{CS} → GND → bus capacitor
  - Current path during t_{OFF} time: transformer → SR_MOS → C_{OUT} → GND → transformer
  - Current in leakage inductance and snubber circuit
  - Drive loop of primary and secondary MOSFETs
- Place these components near SQ33020:
  - Fault capacitor, comp capacitor, f_{MAX} resistor, CS resistor (in series), VCC capacitor.
  - ZCS pullup resistor should be placed near the AUX pin of the transformer, and pulldown resistor should be near the ZCS pin.
- The REG and TZ resistors, V_{DD} and V_{IN} capacitors should be close to SQ33239.
- GND routing is as follows:
  - SQ33020's GND should be connected to RCS_GND in order to get accurate V_{CS} signal.

- Because $V_{GS(TH)}$ of the MOS FET may be as low as 1.2V, it can easily be falsely triggered by noise.
  - Connect IC_GND to RCS_GND directly.
- Keep the drive loop as small as possible.

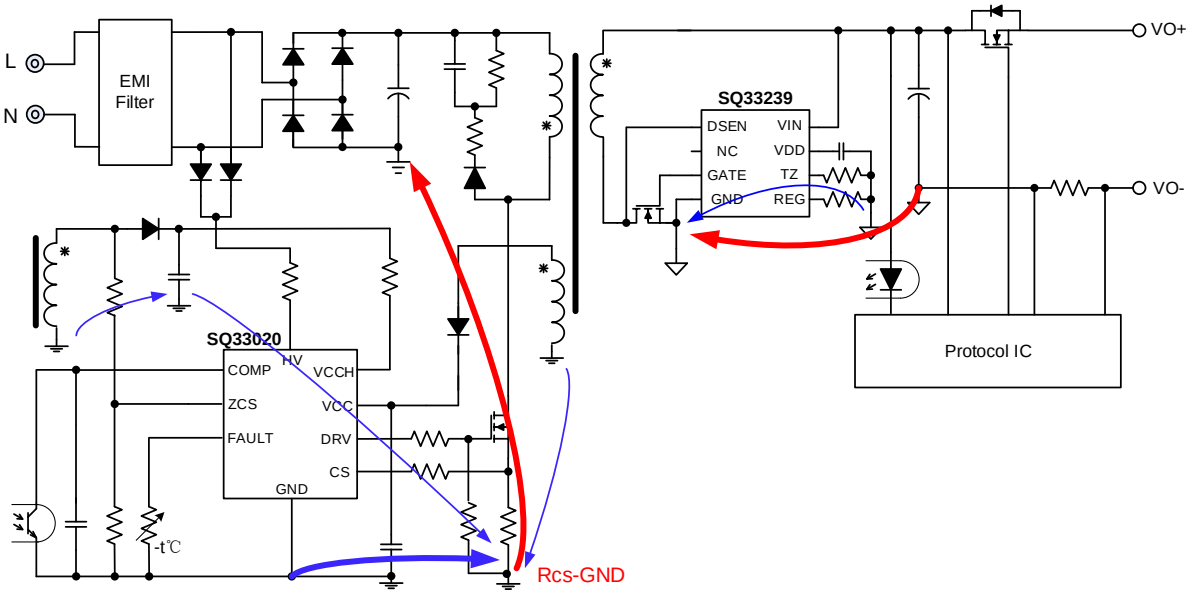


Figure 20. Recommended PCB Layout

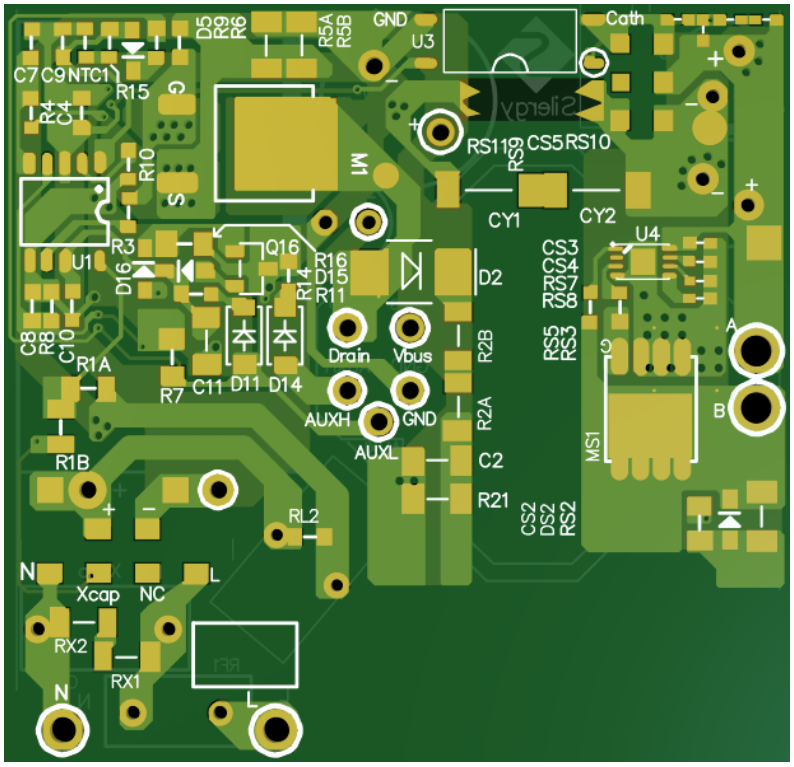


Figure 21. Recommended PCB Layout (Bottom Layer)

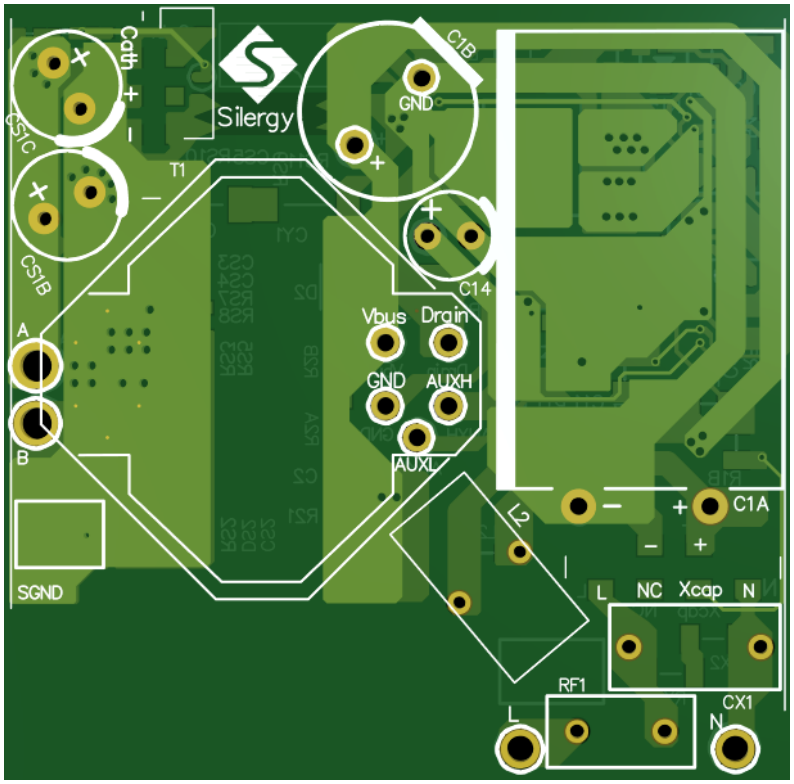


Figure 22. Recommended PCB Layout (Top Layer)

Design Example

This section provides a step-by-step design example of a typical application.

Input/Output Specifications

Parameter	Symbol	Value
Input voltage range	V_{IN}	DC200V–DC400V (with PFC)
Rated output power	P_O	66W
Rated output voltage	V_O	5V–20V
Output OVP level	V_{O_OVP}	24V
Rated output current	I_O	3.3A
Output OCP	I_{OCP}	3.7A
Efficiency	η	93%

Preset Parameters

Parameter	Symbol	Value
Breakdown voltage of power MOS	V_{MOS_BR}	700V
V_{DS} de-rating factor of power MOS	K_{DR}	90%
Spike on V_{DS} at power MOS turn-off	ΔV_{SN}	70V
BUS capacitor charge coefficient	K_{CH}	0.2
Secondary diode forward voltage drop	V_{D_R}	0V (SR)
Transformer effective Ae (RM8)	A_E	62mm^2

1. **BUS capacitor selection**
   Select BUS capacitor: C_{BUS} = 33μF (0.5uF/W with PFC)

2. **Minimum BUS voltage**
   V_{BUS_MIN} = 200V (With PFC)

3. Transformer design

(a) Transformer core: RM8, Ae = 62mm^2

(b) Winding width of bobbin: 8.1mm

(c) N_S winding wire: 0.10mm × 100

(d) N_S = 5ts

(e) N_{PS} is selected as: N_{PS} = 6.25, reflected voltage V_{OR} = 6.25 × 20V = 125V

(f) N_P is calculated as Np = N_{PS} × N_S = 31ts

(g) N_P winding wire: 8.1mm × 90%/16ts; wire should be 0.45mm–0.02mm = 0.43mm, or Litz line of 0.10mm × 20

(h) Calculate R_{CS}: in normal operation, V_{REF_OCP} = 0.85V

$$R_{CS} = \frac{0.93\times V_{REF\_OCP}\times N_{PS}}{6\times I_{OUT\_OCP}} = \frac{0.93\times 0.85V\times 6.25}{6\times 3.7A} = 0.222\Omega$$

(i) Calculate maximum primary peak current:

$$I_{PPK\_MAX} = \frac{V_{CS\_LIMIT}}{R_{CS}} = \frac{0.50V}{0.222\Omega} = 2.25A$$

(j) Determine B_{MAX} = 0.37T

(k) Calculate primary winding L_P:

$$N_P = \frac{L_P\times I_{PPK\_MAX}}{B_{MAX}\times A_E} = \frac{Lp\times 2.25A}{0.37T\times 62mm^2} = 31ts,$$ then L_P = 316μH.

(l) Calculate auxiliary winding turns N_{AUXL} = 5ts: V_{OUT_MAX} = 20V

$$18V < \frac{V_{OUT\_MAX}}{N_S}\times N_{AUXL} < 22V,\ 4.5 < NAUXL < 5.5$$

(m) Calculate auxiliary winding turns N_{AUXH} = 12ts: V_{OUT_MIN} = 5V

$$10V < \frac{V_{OUT\_MIN}}{N_S}\times N_{AUXL} < 14V,\ 10 < N_{AUXH} < 14$$

4. Secondary diode selection

(a) Maximum reverse voltage calculation:

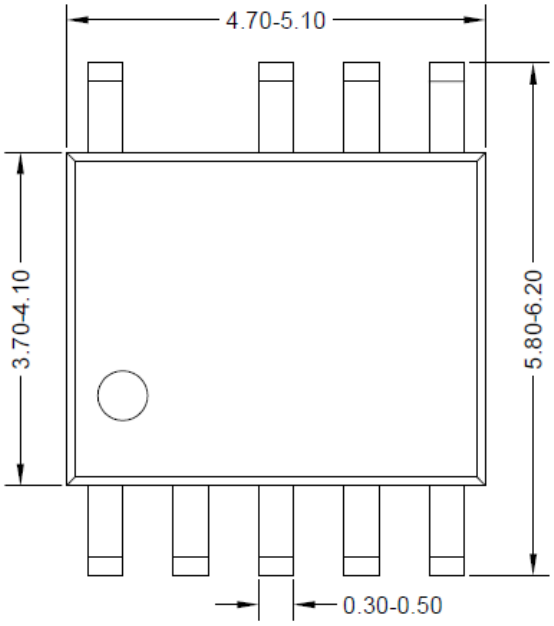
$$V_{D\_R\_MAX} = \frac{\sqrt{2}V_{IN\_MAX}}{N_{PS}} + V_{O\_OVP} = \frac{\sqrt{2}\times 264}{6.25} + 24 = 84V$$

Considering the voltage spike, reverse voltage rating is recommended to be 100V–120V.

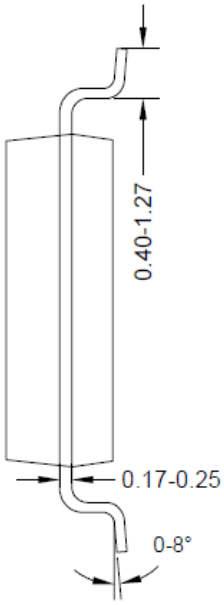
(b) Maximum instantaneous forward current:

$$I_{SPK\_MAX} = I_{PPK\_MAX}\times N_{PS} = 2.25A\times 6.25 = 14.1A$$

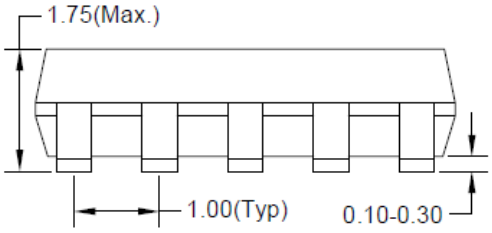
SSOP9 Package Outline Drawing



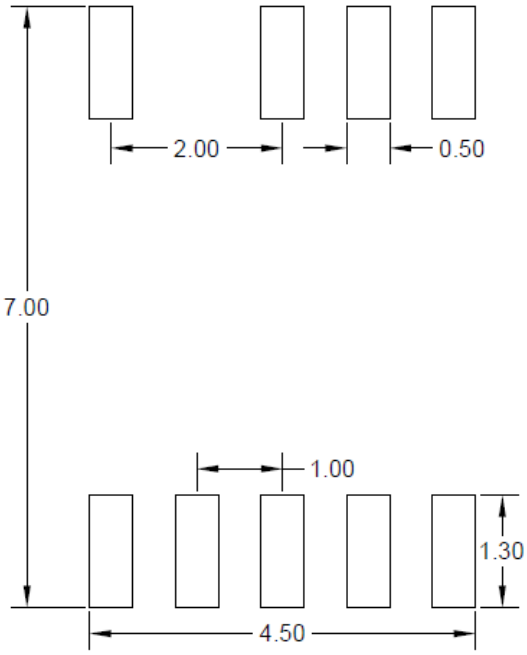
Top View



Side View



Front View

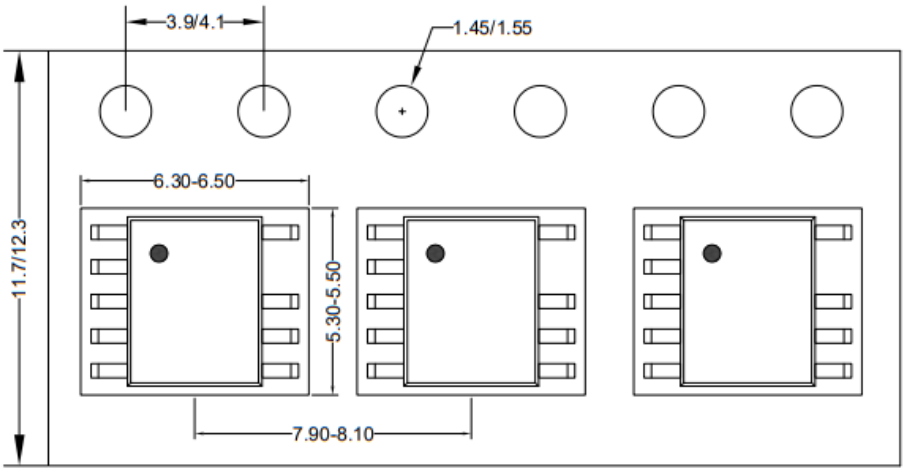


Recommended PCB Layout
(Reference Only)

Note: All dimensions are in millimeters and exclude mold flash and metal burr.

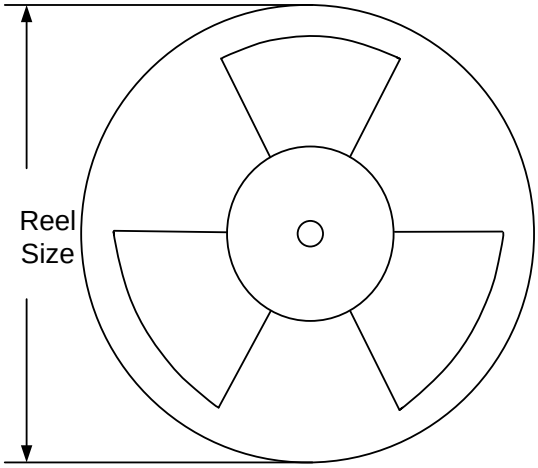
Tape and Reel Specification

Tape dimensions and pin 1 orientation



Feeding Direction ⟶

Reel dimensions



Package types	Tape width (mm)	Pocket pitch (mm)	Reel size (Inch)	Trailer * length (mm)	Leader * length (mm)	Qty per reel (pcs)
SSOP9	12	8	13"	400	400	4000

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, however, not warrantied. Please make sure that you have the latest revision.

Date	Revision	Change
June 9,2024	Revision 1.0	Initial Release

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